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Noise analysis and optimization of VCII-based SiPM interface circuit

G. Ferri[1] · L. Safari[1] · G. Barile[1] · L. Pantoli[1] · V. Stornelli[1]

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Abstract
Recently, second generation voltage conveyor (VCII)-based transimpedance amplifiers (TIAs) have begun to find their way in different applications, among which, silicon photomultipliers (SiPMs) interfacing circuitry. There are many advantages which make VCII-based TIAs attractive over conventional circuits: the intrinsic low impedance at VCII current input Y port is very helpful to mitigate the effect of high value sensor capacitance and provides fast response time; the achieved bandwidth is high and due to current mode operation; the circuits enjoy the low-voltage low-power features. As signal-to-noise ratio is a crucial parameter in SiPMs interface circuit applications, here we consider the noise specifications and optimization of VCII-based SiPM interface circuits. The noise model of VCII is introduced and equivalent noise of a VCII-based interface circuit is derived. Methods to optimize trade-offs existing between key parameters including power consumption, gain and noise performance are discussed. Simulation results are also provided showing a considerable reduction of two orders of magnitude in most of the noise performances when compared to the previous work while preserving other performance parameters.

Keywords CCII · Current mode · VCII · Current conveyor

1 Introduction

Interesting features such as high photodetection efficiency, robustness, high gain and low-cost has created a high interest in Silicon Photomultiplier detectors (SiPM), which are very promising in different fields of fast timing applications such as medical imaging (TOF-PET) and high energy physics [1–6]. On the other side, SiPMs have drawbacks related to some performance parameters for the dedicated preamplifier. For example, to avoid the reduction in response time caused by high value output capacitance of SiPM, (which exhibits values in the range of hundreds of pF [7, 8]), the preamplifier circuit must exhibit very low input impedance. In addition, SiPMs do not behave as an ideal current source and their equivalent output impedance varies by the amount of incident light. Therefore, the low input impedance of the preamplifier is mandatory to keep the nonlinear behavior caused by non-constant output impedance of SiPM, as low as possible. Another important parameter of preamplifier is the low noise performance which is crucial to avoid whole system signal-to-noise degradation. Definitively, as the amplitude of SiPM output current is low, the preamplifier should exhibit very low noise feature. Finally, in order to use the full potential of SiPM in achieving fast response time, high frequency performance is another critical parameter in the associated preamplifier. The reduction in the allowed supply voltage in advanced CMOS technologies also puts severe limitations on the preamplifier dynamic range. All these considerations reveal that the design of preamplifier circuit for SiPM is very challenging because there is a need for a careful optimization of trade-offs between input impedance, bandwidth, dynamic range, noise performance and power consumption. Therefore, novel circuit topologies should be developed to relax the downsides of SiPM and fully exploit its desired features.

Recently, with the aim of designing a very effective SiPM preamplifier circuit, a new approach based on second generation voltage conveyor (VCII) has been introduced and its effectiveness has been investigated in literature [9–14]. Especially in [13] a comparative analysis on realizing various analog functions using VCII, CCII and

✉ G. Ferri
giuseppe.ferri@univaq.it

[1] Department of Industrial and Information Engineering and Economics, University of L'Aquila, 67100 L'Aquila, Italy

operational amplifiers is given. Figure 1(a) reports the symbol of VCII, which is the dual of well-known second generation current conveyor (CCII) [12–14]. Unlike CCII, VCII Y node is a low impedance current input port. The impedance at Y node is ideally zero, so it can be used as preamplifier input. X is a high impedance current output or voltage input terminal. The input current at Y node is transferred to X node by a current gain $\pm\ \beta$ very close to unity. $VCII^{+}$ and $VCII^{-}$ are denoted by $+\ \beta$ and $-\beta$ respectively. The Z terminal is a low impedance voltage output node. The voltage produced at X terminal is transferred to Z terminal by a voltage gain α ideally close to unity:

$$\beta = \frac{\beta_0}{1+\frac{s}{P_\beta}}, \alpha = \frac{\alpha_0}{1+\frac{s}{P_\alpha}} \tag{1}$$

being β_0 and α_0 DC gain values and P_β and P_α the -3 dB bandwidths of β and α respectively. The operation of VCII based SiPM preamplifier in a transimpedance amplifier (TIA) configuration [10], shown in Fig. 1(b), can be simply explained as follows. The SiPM is connected to the low impedance Y port of VCII. The output current of SiPM entering Y port is transferred to X terminal with a gain close to unity. A gain controlling resistor R_g is connected to X terminal. Therefore, the current inside X terminal of SiPM is transferred to a proportional voltage at X node,

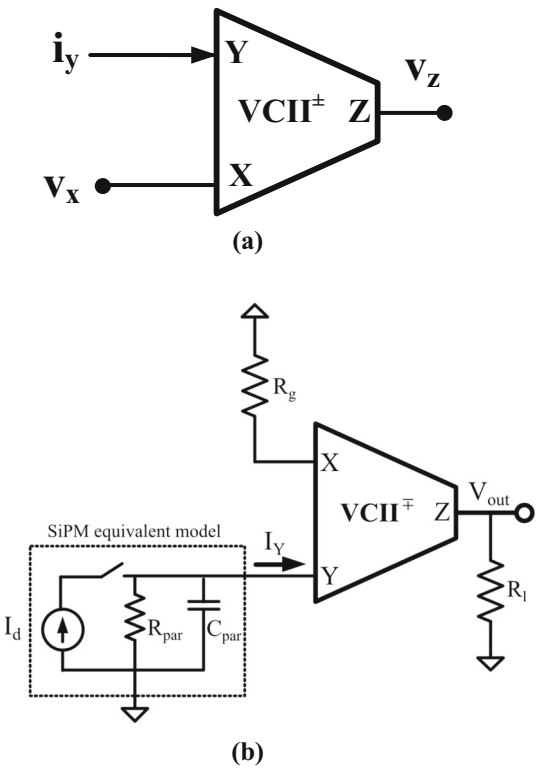

Fig. 1 VCII **a** Symbolic representation [12] and **b** SiPM preamplifier [10]

then the produced voltage is transferred to Z port. Using Eq. (1) the output voltage is found as:

$$V_{out} \approx \pm \frac{\beta_0 \alpha_0 R_g}{(1+\frac{s}{P_\beta})(1+\frac{s}{P_\alpha})(1+sR_gC_x)} I_d \tag{2}$$

being C_x the total parasitic capacitance at X terminal. By assuming $P_\beta,\ P_\alpha >> (R_gC_x)^{-1}$, Eq. (2) is simplified to:

$$V_{out} \approx \pm \frac{\beta_0 \alpha_0 R_g}{(1+sR_gC_x)} I_d \tag{3}$$

From Eq. (3), it is found that the bandwidth is determined by the gain controlling resistor R_g and parasitic capacitance at X terminal.

Using VCII based approach to implement SiPM preamplifier, the following benefits are achieved:

(1) The inherent low input impedance at Y port is very effective in mitigating the effect of SiPM parasitic impedance and capacitance effects.
(2) Thanks to the current mode operation, the bandwidth and dynamic range are high.
(3) The bandwidth is high because is mainly determined by gain setting resistor Rg and the parasitic capacitance at X terminal. Therefore, high bandwidth is simply achievable by reducing Cx through a proper circuit design.

In the previously published works [9–11], the response time and frequency performance of VCII based SiPM preamplifier have been investigated. Since the noise is also a very important parameter, in this paper we address the noise performance of a VCII based preamplifier. As VCII is the dual circuit of CCII, for noise calculations, we follow the approach for current conveyor noise analysis presented in [15]. We start by introducing noise sources in VCII block. Using this model, we derive the output equivalent noise of a general VCII based SiPM preamplifier circuit. Then the noise calculations of VCII CMOS implementation are presented. Based on the results of this study, methods to achieve lower noise performance are discussed. The formulas of the preamplifier key parameters including the VCII node impedances and bandwidth are derived. To confirm the presented theory, Spice simulate results are performed. They show that by applying the discussed optimization methods, the noise performance is significantly improved when compared to the previously designed VCII based preamplifier while preserving other parameter values (voltage and current gains, bandwidth and parasitic impedances). The organization of this paper is as follows: In section II, noise model of VCII is introduced and based on this model the output noise of VCII based SiPM preamplifier is established. In Sect. 3, the CMOS implementation of VCII and its performance parameters

are given. Then, the equivalent noises at its different ports are analyzed. The trade-offs existing between other performance parameters and noise parameter are discussed. Finally, in Sect. 4 simulation results are provided.

2 Noise analysis of a VCII based SiPM preamplifier

2.1 Noise sources of VCII block and VCII based SiPM preamplifier

Figure 2 shows the noise model of VCII block. Similar to current conveyors [16], VCII is a multiple-port device where each terminal is represented by an equivalent voltage noise and an equivalent current noise. As it will be shown, for a specific application not all but some of the noise sources play more important role compared to other noise sources. This fact simplifies the designer task to consider those critical noise sources in the circuit design. Figure 3 shows the VCII based SiPM preamplifier noise model (being Z_{par} the equivalent impedance resulted from parallel connection of C_{par} and R_{par}). In this application, Y port is connected directly to the SiPM which exhibits high output impedance; therefore, the contribution of Y port equivalent noise voltage to the overall noise performance is negligible. In other words, due to high output impedance of SiPM the current noise produced by $dv^2{}_{Yneq}$ is unimportant; therefore, its effect can be neglected. Due to current buffering action between Y and X ports and voltage buffering action between X and Z ports, any current noise source at Y port is transferred to X port and any noise voltage at X port is transferred to Z port. Assuming unity value for α and β, the output noise voltage of Fig. 3 is calculated as:

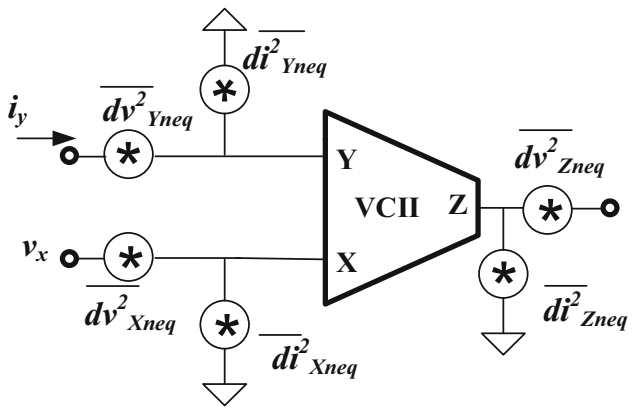

Fig. 2 Noise model of VCII

$$\overline{dv^2_{out}} = \left(\overline{di^2_{Yneq}} + \overline{di^2_{Xneq}}\right)R_g^2 + \overline{dv^2_{Xneq}} + \overline{dv^2_{Rg}} + \overline{dv^2_{Zneq}} + \overline{di^2_{Zneq}}R_L^2 + \overline{dv^2_{RL}} \quad (4)$$

The two thermal noise contributions of Rg and R_L are respectively: $\overline{dv^2_{Rg}} = 4kTR_g df$ and $\overline{dv^2_{RL}} = 4kTR_L df$, where k is Boltzmann constant, T is absolute temperature, df is frequency bandwidth. In Eq. (4), it is assumed that $R_g << R_X$ and $R_Z << R_L$.

2.2 Noise calculation of VCII circuit

For noise analysis we consider the VCII CMOS implementation of Fig. 4 which has been used in [10] to implement a SiPM preamplifier. In this circuit the negative feedback loop established by differential pair M_1-M_4 is used to reduce the impedance at Y port and to clamp V_Y at ground. The current at Y port is transferred to X port by means of simple current mirror made of M_6-M_7. The voltage produced at X port is transferred to Z port through a simple flipped voltage follower (FVF) [17] based voltage buffer made of M_9-M_{10}.

M_8 is used to set the DC offset voltage at Z port equal to zero. The small signal equivalent circuit of Fig. 4 is shown in Fig. 5 where, ro_i and gm_i denotes the output impedance and transconductance of related transistor. Also, ro_{IBi} denotes the output impedance of related current source. Using the presented small signal model, the simplified formulas of impedances at Y, X and Z ports as well as those for α_0 and β_0 are expressed as respectively:

$$r_y \approx \left[gm_2 gm_5 \bullet (ro_2 // ro_4)\right]^{-1} \quad (5)$$

$$r_x \approx ro_{IB3} // ro_7 \quad (6)$$

$$r_Z \approx \left[gm_9 gm_{10} ro_{IB4}\right]^{-1} \quad (7)$$

$$\alpha_0 \approx \frac{ro_7}{ro_7 + gm_8^{-1}} \quad (8)$$

$$\beta_0 \approx \frac{gm_7}{gm_6} \quad (9)$$

In Eq. (5), pair wise matching between differential pair transistors is assumed.

Figure 6 shows the noise model of VCII circuit of Fig. 4 where the noise produced by each MOS transistor is presented as a current source connected in parallel to it. For proper noise calculation, in Fig. 6, the implementation of current sources IB1–IB4 by means of simple current mirrors are also shown. The transistor noise includes 1/f and channel thermal noise.

The contribution of 1/f noise on the overall wide bandwidth noise is negligible, therefore the output current noise of the ith transistor is approximated as thermal noise [16]:

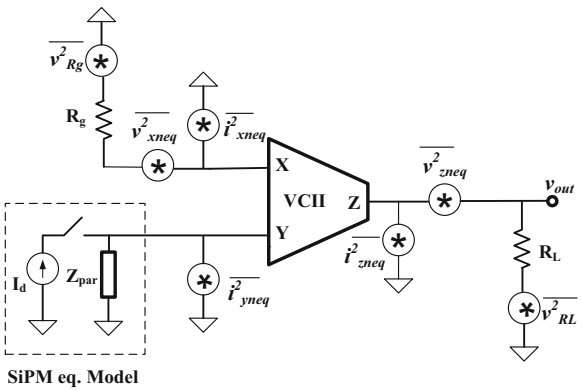

Fig. 3 Noise model of VCII based SiPM preamplifier

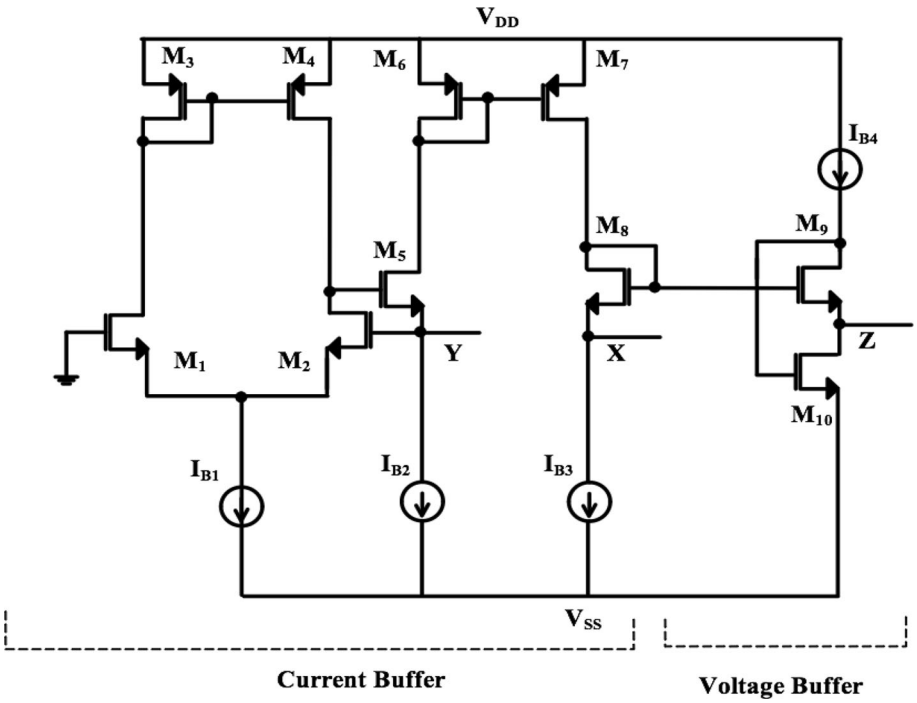

Fig. 4 CMOS implementation of VCII [10]

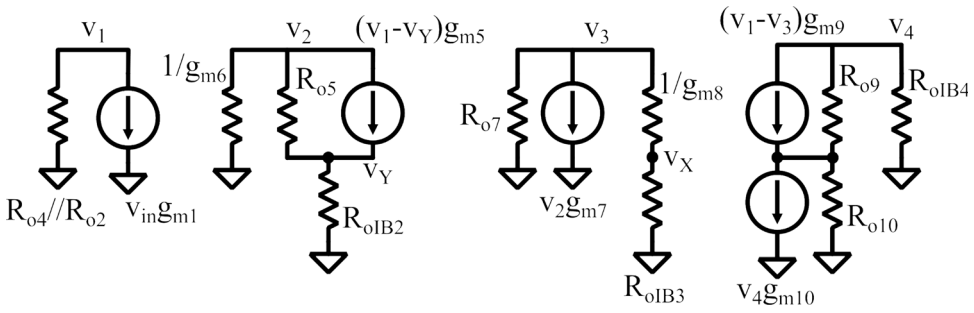

Fig. 5 Small signal equivalent circuit of Fig. 4

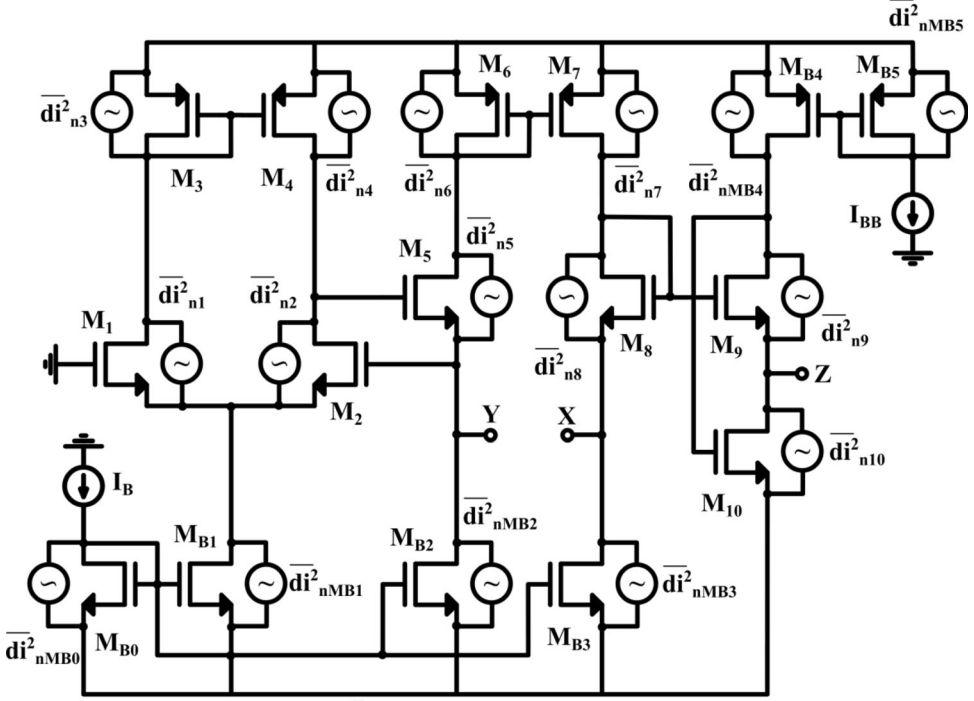

Fig. 6 VCII CMOS circuit with noise sources

$$\overline{di_{ni}^2} = 4kT\gamma gm_i df \tag{10}$$

where k is Boltzmann's constant, T is absolute temperature, df is frequency bandwidth, γ is a constant coefficient ranging from 1/3 to 2/3 and gm_i is the transconductance of the *ith* transistor.

The noise contribution of differential pair made of M_1-M_4 is a noise voltage at Y port expressed as:

$$\overline{dv_{M1-M4}^2}\Big|atY \approx 4\frac{\overline{di_{n1}^2} + \overline{di_{n2}^2} + \overline{di_{n3}^2} + \overline{di_{n4}^2}}{{g_m}^2} \tag{11}$$

being $g_{m1} = g_{m2} = g_m$.

The noise contribution of current source I_{B1} is negligible. The reason is that the output noise produced by I_{B1} is attenuated by differential pair as a common mode signal. Transistor M_5 also produces noise voltage at Y port equal to:

$$\overline{dv_{M5}^2}\Big|atY = \frac{\overline{di_{n5}^2}}{{g_{m5}}^2{g_m}^2(r_{o2}\|r_{o4})^2} \tag{12}$$

Using Eq. (11) and Eq. (12), the total noise voltage at Y port is:

$$\overline{dv_{yneq}^2} = \overline{dv_{M1-M4}^2}\Big|atY + \overline{dv_{M5}^2}\Big|atY \approx \frac{4kT\gamma}{gm_1^2}\left[4gm_1 + 4gm_2 + 4gm_3 + 4gm_4 + \frac{1}{g_{m5}(r_{o2}\|r_{o4})^2}\right]df \tag{13}$$

From Eq. (13), it is seen that increasing gm_2 reduces the equivalent current noise voltage at Y port. From Eq. (5), the impedance at Y terminal is also improved by increasing gm_2.

Considering the relationship between bias current and overdrive voltage with gm_2 represented in Eq. (14), reveals that the allowed supply voltage and the required power consumption set a limit on the maximum value of gm_2,

because increasing gm_2 demands high value for I_{B2} and consequently the high value of overdrive voltage V_{GS2}-V_{TH} is required to keep M_1-M_4 in saturation region. Equation (14) shows also the well-known alternative representation of gm_2 in terms of transistor aspect ratios and bias currents in strong inversion. After setting the value of I_{B1} based on circuit power budget, the value of gm_2 can be increased by selecting large values for M_1-M_2 aspect ratios. By this, although the parasitic capacitance associated with Y port will increase, but due to the concurrent reduction in Y port impedance, the effect of increasing aspect ratio of M_1-M_2 on the frequency performance will be negligible. It is worth mentioning that the transistors size increase must not push them in weak inversion region:

$$gm_2 = \frac{2I_{B1}}{V_{GS2-}V_{TH2}} = \sqrt{I_{B1}\mu_n C_{ox}\frac{W_2}{L_2}} \tag{14}$$

The noise contribution of M_5 is a voltage at Y port equal to:

$$\overline{dv_{M5}^2} = \frac{\overline{di_{n5}^2}}{A^2 g_{m5}^2} = \frac{4kT\gamma df}{A^2 g_{m5}} \tag{15}$$

where, by assuming pair wise matching between differential amplifier transistors (i.e. M_1 to M_2 and M_3 to M_4), A is:

$$A \approx g_m(ro_4 \| ro_2) \tag{16}$$

being gm the transconductance of M_1-M_2. According to Eq. (15) and Eq. (16), to reduce the noise contribution of M_5, its gm value should be high. It is remarkable that the noise voltage at Y node does not contribute to the total output noise of the TIA (see Eq. (4)).

The equivalent current noise at Y port is expressed as:

$$\begin{aligned}\overline{di_{Yneq}^2} &= \overline{di_{n6}^2} + \overline{di_{nIB2}^2} = \overline{di_{n6}^2} + \overline{di_{nMB2}^2} + \overline{di_{nMB0}^2} \\ &= 4kT\gamma(gm_6 + gm_{B2} + gm_{B0})df\end{aligned} \tag{17}$$

As M_6 is a PMOS transistor, its produced channel noise is lower. It is also worth mentioning that as there is good matching between transistors with large aspect ratios [18, 19], according to Eq. (9), to keep the value of β_0 at unity, large aspect ratios must be set for M_6-M_7. This will increase the parasitic capacitances associated with these transistors. However, as the input impedance of current mirror M_6-M_7 will reduce by increasing their aspect ratios, the effect on overall bandwidth will be partly compensated. In addition, referring to Eq. (8), to keep the α_0 close to unity, large value is required for ro_7 which can be set by increasing channel length or reducing its bias current. However, the required dynamic range sets a limit on the minimum value of bias current. The noise produced by current source I_{B2} can be made negligible by setting the gm of the related transistors as low as possible.

The equivalent current noise at X port is:

$$\begin{aligned}\overline{di_{Xneq}^2} &= \overline{di_{n7}^2} + \overline{di_{nIB3}^2} = \overline{di_{n7}^2} + \overline{di_{nMB3}^2} + \overline{di_{nMB0}^2} \\ &= 4kT\gamma(gm_7 + gm_{B3} + gm_{B0})df\end{aligned} \tag{18}$$

Similar considerations can be done for this result.

The equivalent voltage noise at X port is also obtained as:

$$\overline{dv_{Xneq}^2} = \frac{\overline{di_{n8}^2}}{gm_8^2} + \frac{\overline{di_{n9}^2}}{gm_9^2} == 4kT\gamma({gm_8}^{-1} + {gm_9}^{-1})df \tag{19}$$

As Eq. (19) implies, choosing large values for gm_8 and gm_9, the noise voltage at X terminal is reduced. In the circuit of Fig. 6, the same noise voltage at X node is produced at Z terminal.

The expression for noise current at Z port is:

$$\begin{aligned}\overline{di_{Zneq}^2} &= \overline{di_{n10}^2} + \overline{di_{nIB4}^2} = \overline{di_{n10}^2} + \overline{di_{nMB4}^2} + \overline{di_{nMB5}^2} \\ &= 4kT\gamma(gm_{10} + gm_{B4} + gm_{B5})df\end{aligned} \tag{20}$$

As the M_{B4}-M_{B5} are PMOS transistors which inherently produce low noise compared to NMOS transistors, the effective method to reduce current noise at Z output is reducing the value of g_{m10}. To avoid increasing the impedance at Z port due to the reduction of g_{m10}, the output impedance of I_{B3} current source should be increased by choosing large values for the channel length of transistor M_{B4}-M_{B5}.

3 Simulations

The VCII circuit of Fig. 4 is simulated using Spice and 0.35 μm CMOS technology with a supply voltage of ± 1.65 V. The approach we used to optimize noise performances is given in Table 1. Table 2 shows the new values for transistors' aspect ratios along with the former ones from [10]. A comparison between pre and post optimization VCIIs is given in Table 3 where noise sources at Y, X and Z ports as well as other performance parameters are given.

As it is stated in Table 2, the major increase in aspect ratio is equal to 10 times related to M_1-M_2 and M_5, so we expect approximately 30% increase in the used area. However, investigating the achieved noise results at Table 3 shows a 51 times reduction for noise current at Y node, a 121 times reduction for noise current at X, a 105 times reduction for noise voltage at X, a 58 times reduction for noise current at Z and a 107 times reduction for noise voltage at Z while the increase in power consumption is only 52 μW and other performance parameters remain rather unchanged. We added these points in the simulation results.

The output noise of the VCII based preamplifier (Fig. 1b), expressed by Eq. (4) is shown in Fig. 7 after and

Table 1 Noise reduction cause-effect table

Equation	Cause	Effect
(17–18)	Reduction of the transconductance of MB0, MB2 and M6 by decreasing W/L	Reduction in the current noise at Y and X terminals
(19)	Increment of the transconductance of M8, and M9 by increasing W/L	Reduction in the voltage noise at X terminal
(20)	Reduction of the transconductance of M10 by decreasing W/L	Reduction in the current noise at Z terminal

Table 2 Transistors aspect ratio and current source values of the VCII before [10] and after optimization

Transistors	Dimensions		Current sources	Value	
	Standard design	Optimized design		Standard design	Optimized design
M_1, M_2	W = 21 μm, L = 0.35 μm	W = 210 μm, L = 0.35 μm	I_B	30 μA	30 μA
M_3, M_4	W = 4.2 μm, L = 0.35 μm	W = 4.2 μm, L = 0.35 μm	I_{BB}	40 μA	40 μA
M_5	W = 7 μm, L = 0.35 μm	W = 210 μm, L = 0.35 μm			
M_6, M_7	W = 72.8 μm, L = 4.6 μm	W = 11.2 μm, L = 4.6 μm			
M_8, M_9	W = 28.7 μm, L = 1.4 μm	W = 50.05 μm, L = 0.7 μm			
M_{10}	W = 14 μm, L = 52 μm	W = 14 μm, L = 80.15 μm			
M_{B0}, M_{B1}	W = 2.1 μm, L = 0.7 μm	W = 0.7 μm, L = 0.7 μm			
M_{B2}, M_{B3}	W = 2.8 μm, L = 0.7 μm	W = 1.05 μm, L = 0.7 μm			
M_{B4}, M_{B5}	W = 132.3 μm, L = 42 μm	W = 133 μm, L = 42 μm			

Table 3 Performance and noise parameters of the VCII (Left) and open loaded TIA (Right) before [10] and after optimization

Parameter	Value		Noise source	Value (@ 100 kHz)	
	Standard design	Optimized design		Standard design	Optimized design
ry	49 Ω	106 Ω	Inoise at Y	220 pA/$\sqrt{}$Hz	4.3 pA/$\sqrt{}$Hz
Rx	802 kΩ	622 kΩ	Vnoise at Y	10.5 nV/$\sqrt{}$Hz	9.3 nV/$\sqrt{}$Hz
rz	79 Ω	380 Ω	Inoise at X	219 pA/$\sqrt{}$Hz	1.8 pA/$\sqrt{}$Hz
(α_0, P_α) α	0.995, 340 MHz	0.994, 483 MHz	Vnoise at X	3 μV/$\sqrt{}$Hz	28.4 nV/$\sqrt{}$Hz
(β_0, P_β) β	0.996, 14.6 MHz	0.978, 21 MHz	Inoise at Z	280 pA/$\sqrt{}$Hz	4.8 pA/$\sqrt{}$Hz
Static power dissipation	700 μW	752 μW	Vnoise at Z	2.9 μV/$\sqrt{}$Hz	27 nV/$\sqrt{}$Hz

before optimization. As it is seen, in agreement with Table 3, it is reduced from 3.2 μV/$\sqrt{}$Hz to 29.9 nV/$\sqrt{}$Hz (@100 kHz) in the optimized circuit. The frequency performance of VCII-based preamplifier for different values of Rg is also shown in Fig. 8. As it is seen, the applied optimization does not have significant effect on the frequency performance.

4 Conclusions

In this paper we address the noise model and performance of VCII-based SiPM preamplifier. As a multi-port device, each port is modeled by an equivalent voltage and current noise. It is discussed that due to the high output impedance of SiPM, the equivalent noise voltage at Y port does not contribute to the overall noise performance of VCII based preamplifier. However, both equivalent current and voltage noises at X port are transferred to the output and play an important role on the determining noise at preamplifier output port.

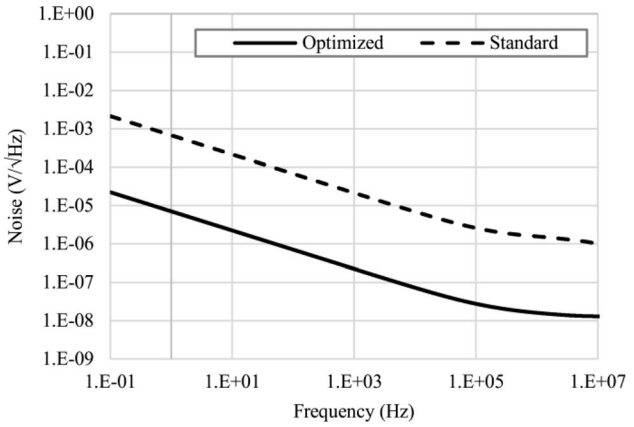

Fig. 7 The output noise of the VCII based preamplifier after and before optimization

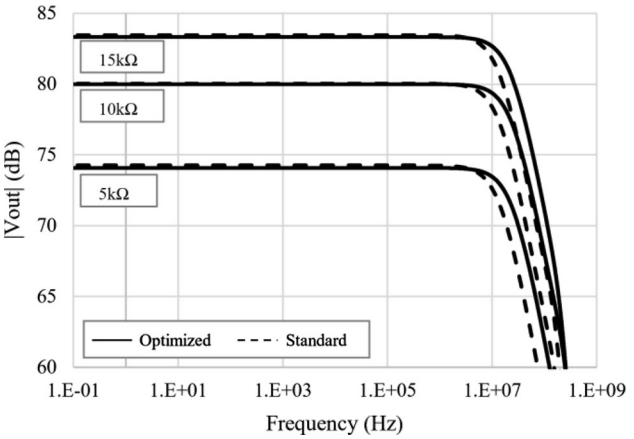

Fig. 8 The frequency performance of the VCII based preamplifier after and before optimization

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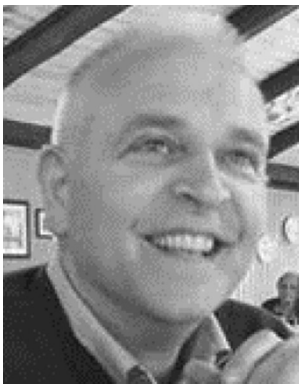

Giuseppe Ferri was born in L'Aquila, Italy. He received the "Laurea" degree (cum laude) in electronic engineering in 1988. In 1991, he joined the Department of Electronic Engineering, University of L'Aquila, L'Aquila, Italy, where he is actually a full professor of Electronics and Microelectronics. His research activity mainly concerns the design of analog electronic circuits for integrated sensor applications both in voltage and in current-mode. In this field of research, he is author or coauthor of 7 patents, 3 international books, one book chapter and about 400 publications in international journals and conference proceedings. He is an IEEE senior member and Editor of Sensors and of Journal of Circuits, Computers and Systems.

Leila Safari received the master's degree in electrical engineering from the Iran University of Science and Technology (IUST) in Islamic Republic of Iran, where she also received her Ph.D. from. She is currently area Editor of International Journal of Electronics and Communications-AEUE and reviewer of ISI Journals and IEEE conferences. Her research activity revolves around CMRR optimization in CMOS and BJT OpAmps, study on current-mode circuits, design of current-mode and mixed-mode integrated circuits and design of industrial systems.

Gianluca Barile was born in Avezzano, Italy. He received the master's degree (cum laude) in Electronics Engineering from the University of L'Aquila (Italy) in 2016, where He received his Ph.D. degree (cum laude) in 2020. His research interests revolve around discrete and integrated electronic interfaces for sensors, autonomous sensor networks, low-voltage low-power integrated circuits, current-mode readout techniques, electronics for industrial applications.

Leonardo Pantoli (M'09) received the Degree (cum laude) in Electronic Engineering and the Ph.D. in Electrical and Information Engineering from the University of L'Aquila, L'Aquila, Italy, in 2006 and 2010, respectively. In 2007 and 2008, he spent several months with the Communications Engineering Department of University of Cantabria, Spain and the C2S2 Department of the XLIM Research Institute, Brive La Gaillarde, France. He is Researcher with the University of L'Aquila and his research activities include the development of design methods for microwave nonlinear circuits, linear and nonlinear stability analysis, electronic interfaces for SiPMs and MMICs design for space and communication.

Vincenzo Stornelli was born in Avezzano, Italy. He received the "Laurea" degree (cum laude) in electronic engineering in 2004. In October 2004, he joined the Department of Electronic Engineering, University of L'Aquila, L'Aquila, Italy, where he is involved as Associate His research interests include several topics in computational electromagnetics, including microwave antenna analysis for outdoor ultrawideband applications. He serves as a reviewer for several international journals and Editor of the Journal of Circuits, Computers and Systems.