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# Electronically Tunable First Order AP/LP and LP/HP Filter Topologies Using Electronically Controllable Second Generation Voltage Conveyor (CVCII)

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**Abstract:** In this paper two new first order filter topologies realizing low-pass/all-pass (LP/AP) and low-pass/high-pass (LP/HP) outputs using electronically controllable second generation voltage conveyors (CVCIIs) are presented. Unlike second generation voltage conveyors (VCII), in CVCII each performance parameter, including ports, parasitic impedances, current and/or voltage gains can be electronically varied. Here, in particular, the proposed filter topologies are based on two CVCIIs, one resistor and one capacitor. In the first topology $V_{LP}/I_{AP}/V_{AP}$ and in the second topology $I_{LP}/V_{LP}/I_{HP}/V_{HP}$ outputs are achievable, respectively. However, the current and voltage outputs are not achievable simultaneously and a floating capacitor is used. A control current ($I_{con}$) is used to change the first CVCII Y port impedance, which sets the filter −3 dB frequency ($f_0$) of all the outputs. Moreover, in the second topology, the gains of HP and AP outputs are electronically adjusted by means of a control voltage ($V_{con}$). Favorably, no restricting matching condition is necessary. PSpice simulations using 0.18 µm CMOS technology and supply voltages of ±0.9V show that by changing $I_{con}$ from 0.5 µA to 50 µA, $f_0$ is varied from 89 kHz to 1 MHz. Similarly, for a $V_{con}$ variation from −0.9 V to 0.185 V, the gains of $I_{AP}$ and $I_{HP}$ vary from 30 dB to 0 dB and those of $V_{AP}$ and $V_{HP}$ vary from 100 dB to 20 dB. The total harmonic distortion (THD) is about 8%. The power consumption is from 0.385 mW to 1.057 mW.

**Keywords:** electronically tunable; voltage conveyor; VCII; all-pass filter; low-pass filter; high-pass filter; first order; CVCII



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## 1. Introduction

First order filters are fundamental building blocks in analog signal processing since they find wide applications in realizing higher order filter topologies [1–7]. The first order low-pass (LP) and high-pass (HP) filters are used to separate signals according to their frequency in various applications. However, the first order all-pass (AP) type has a different function. It is used to shift signal phase while its amplitude is kept constant. In addition, the first order AP type is also used to equalize the undesired phase change that occurs during signal processing. Other applications are high quality factor frequency selective filters and synthesizing quadrature and multiphase oscillators.

Due to many advantages given by current mode signal processing, in recent times various current mode active building blocks (ABBs) have been employed in the realization of first order filters [8–19]. The main benefits achieved by processing signals in current domain are high frequency operation, reduced complexity, low voltage operation, etc. Specifically, after the introduction of the second generation current controlled current conveyor (CCCII) [20], the new age of electronically tunable filter design has begun. In the electronically tunable filters, natural frequency and/or gain can be tuned using a control

voltage or current. Therefore, not only the number of passive components is reduced but also the possibility of full integration is provided.

The literature survey shows that the electronically tunable first order filters reported so far [21–32] suffer from a number of shortcomings. In [21], a first order AP filter using simple current mirrors is reported. Using two control voltages of (+VA and −VA), the bias current of the current mirrors is varied, so its input impedance is electronically varied, resulting in an electronically variable −3 dB frequency ($f_0$). Unfortunately, it lacks electronic tunability of gain. In [22], a new implementation of the first order AP/HP/LP filter is reported using inverting type second generation current conveyor (ICCII). Here, to change $f_0$, an electronically variable resistor implemented by a single MOS transistor is used, but its main limitation is that the value of the gain is not electronically controllable. In [23], BJT current mirrors are used to implement first order AP/HP filter. Similar to [21], $f_0$ is changed by varying the input impedance through a suitable variation of the bias current. However, it is not fully electronically controllable because its gain is fixed. In the topology reported in [24], CCCII is used as active building block. The impedance at X port of CCCII is varied through the control current, resulting in the electronic tuning of $f_0$. However, the filter gain is constant. In [25], a first order AP filter using current differencing transconductance amplifier (CDTA) is reported. In this circuit, the electronic tuning of $f_0$ is achieved through the control current, which tunes the value of CDTA transconductance. Nevertheless, its gain is unitary and uncontrollable. In [26], two current controlled current conveyor transconductance amplifiers (CCCCTA) implemented in BJT technology and a capacitor are used to design a first order AP filter. In this approach the first control current is used to tune $f_0$ while the second control current sets the filter gain. Unfortunately, the CCCCTA implementation requires 51 BJT transistors and high supply voltage. In [27], a first order AP filter is introduced using BJT based modified CCCII where the impedance at X port is varied by the control current. Its correct operation relies on the accuracy of the used current mirrors employed in the internal structure of CCCII. In addition, it can only provide gain value of unity. Other CCCII based AP filters, such as that described in [28], suffer from matching conditions, which are not easy to fulfil, and in which the value of parasitic impedance at the X port must be half of the used passive resistor. The topology reported in [29] using dual output CCCII suffers from matching condition restriction and no gain controllability. In [30], the used ABB is CCCTA and it provides full electronic controllability over all-pass current. In [31], a current follower cascaded transconductance amplifier (CFCTA) is used to produce first order positive/negative low-pass current with fully electronic controllability. Unfortunately, it suffers from high power consumption. In [32], an adjustable current amplifier (CA) and two current buffers (CBs) are used to produce fully differential first order AP current output. The circuit of [32] suffers from high power consumption. In summary, apart from other limitations, the common drawback of all of the electronically tunable first order filters reported in [18–32] is that the output signals are in current form so they are limited to current output applications.

Recently, for applications requiring voltage output, a new active building block called second generation voltage conveyor (VCII), which is the dual of CCII, has been used [33–38]. The advantage of this new ABB over CCII and other current mode ABBs is the possibility of processing signals in the current domain while producing the output signals in both the forms of voltage and of current. This new ABB has a low impedance current input port, a high impedance current output port and a low impedance voltage output port. Recently, voltage output second order BP/LP and first order AP filter topologies using VCII have been reported [37,38]. The VCII based filter of [38] produces first order all-pass voltage using one dual output VCII, two resistors and one capacitor. It has two main problems: first, its operation relies on matching conditions between the resistors; second, it lacks electronic tuning capability.

The aim of this paper is the design of versatile voltage and current output electronically tunable first order LP/AP/HP filters without any matching condition requirement. Two topologies are introduced based on two electronically controllable VCIIs (CVCIIs), two

external resistors and one capacitor. The first filter topology can produce first order $V_{LP}$, $I_{AP}$ and $V_{AP}$ outputs. However, $I_{AP}$ and $V_{AP}$ are not reachable simultaneously. The second topology produces first order $I_{LP}$, $V_{LP}$, $I_{HP}$ and $V_{HP}$ outputs simultaneously. It must be mentioned that $I_{LP}$ and $V_{LP}$ are not simultaneously available as $I_{HP}$ and $V_{HP}$. The outputs $V_{LP}$, $V_{HP}$ and $V_{AP}$ are available at low impedance Z ports while $I_{HP}$, $I_{LP}$ and $I_{AP}$ are available at high impedance X ports. Using a control current, the impedance at Y port of first CVCII is varied, resulting in the electronic tunablity of $f_0$. In addition, a control voltage is used to electronically control the gain value of the HP/AP outputs through setting the current gain of second CVCII. Compared to other works, the achieved results are the follows: wider frequency range, no matching condition requirement, electronic tunability of both frequency and gain of HP/AP outputs, no need for extra current or voltage buffers for produced output signals, producing both current and voltage outputs. The noticeable novelty of this paper is that for the first time CVCII is introduced and used in the design of the filters. In fact, the results of this study could open a new era for CVCII based electronically tunable filters. The organization of this paper is as follows. In Section 2 the proposed filters are introduced. In Section 3 nonideal analysis is given. Section 4 includes internal circuit implementation of the used CVCIIs. The simulation results are reported in Section 5. Finally, section VI concludes the paper.

## 2. The Proposed Filters

Symbolic representations of CVCII with electronically tunable Y port impedance and electronically tunable current gain at X terminal are shown in Figure 1a,b, respectively. The operation matrix of CVCII with electronically variable impedance at Y port is given in (1a). Here, the current gain between the Y and X ports and the voltage gain between X and Z ports are $\pm 1$ (+1 for CVCII+ and $-1$ for CVCII$-$). The impedance at Y port is shown by $r_Y$ which can be tuned by $I_{con}$. The operation of CVCII with electronically variable current gain is given in (1b). In this case, the impedance value at the Y port is ideally zero, the value of the voltage gain between the X and Z ports is unity, while the value of current gain between Y and X ports is $\pm K$ (+K for CVCII+ and $-K$ for CVCII$-$) which is adjusted by the control voltage $V_{con}$.

$$\begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix} = \begin{bmatrix} \pm 1 & 0 & 0 \\ 0 & 1 & 0 \\ r_Y & 0 & 0 \end{bmatrix} \begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} \quad (1a)$$

$$\begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix} = \begin{bmatrix} \pm K & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} \quad (1b)$$


**Figure 1.** Symbolic representation of second generation voltage conveyor (CVCII+) with (**a**) variable impedance at Y port and (**b**) variable current gain.

The proposed LP/AP filter topology is shown in Figure 2. It is based on one $CVCII_1{}^+$ with electronically variable impedance at Y port and one $CVCII_2{}^+$ with electronically variable current gain, one capacitor $C_1$ and two external resistors $R_1$ and $R_2$. The input signal is in current form and the produced outputs are $V_{LP}$, $I_{AP}$ and $V_{AP}$. The voltages $V_{LP}$

and $V_{AP}$ are available at the low impedance Z ports, while the current $I_{AP}$ is available at the high impedance X port.

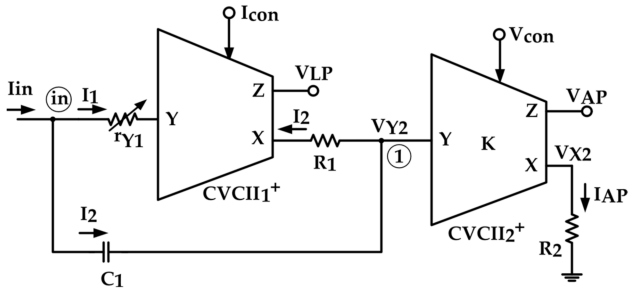



**Figure 2.** The proposed CVCII based low-pass/all-pass (LP/AP) filter topology.

By assuming Y port of $CVCII_2$+ at ground (since in ideal case $r_{Y2} = 0$), and performing the Kirchhoff current law (KCL) at input port (named as "in") results:

$$I_1 = \frac{1}{1 + sC_1r_{Y1}}I_{in} \tag{2}$$

$$I_2 = \frac{sC_1r_{Y1}}{1 + sC_1r_{Y1}}I_{in} \tag{3}$$

Using (1) and (2), $V_{LP} = V_{X1}$ is found as:

$$V_{LP} = V_{X1} = -\frac{R_1}{1 + sC_1r_{Y1}}I_{in} \tag{4}$$

Performing KCL at node 1 and using (1) and (3) result:

$$I_{AP} = K\frac{1 - sC_1r_{Y1}}{1 + sC_1r_{Y1}}I_{in} \tag{5}$$

$$V_{AP} = KR_2\left(\frac{1 - sC_1r_{Y1}}{1 + sC_1r_{Y1}}\right)I_{in} \tag{6}$$

As is seen from Equations (5) and (6), the AP pole frequency is expressed by (7a) which is electronically controlled by $r_{Y1}$, while the low frequency gain of $I_{AP}$ and $V_{AP}$ are expressed in (7b) and (7c), respectively:

$$f_0 = \frac{1}{2\pi C_1r_{Y1}} \tag{7a}$$

$$Gain_{I_{AP}} = K \tag{7b}$$

$$Gain_{V_{AP}} = KR_2 \tag{7c}$$

From Equation (7b,c), we can say that the gain is also electronically controllable by K.

The proposed LP/HP filter topology is shown in Figure 3. In this topology the outputs are $V_{LP}$, $I_{LP}$, $V_{HP}$ and $I_{HP}$. Repeating the same analysis gives Equation (4) for $V_{LP}$ while $I_{LP}$ is found as in the previous topology:

$$I_{AP} = K\frac{1 - sC_1r_{Y1}}{1 + sC_1r_{Y1}}I_{in} \tag{8}$$

The HP current and voltage outputs are found as:

$$I_{HP} = K\frac{sC_1r_{Y1}}{1 + sC_1r_{Y1}}I_{in} \tag{9}$$

$$V_{HP} = -KR_2 \frac{sC_1 r_{Y1}}{1 + sC_1 r_{Y1}} I_{in} \quad (10)$$

From Equations (9) and (10) it is seen that both of the gain and center frequency are electronically controllable while in the LP output only $f_0$ is electronically controllable. Fortunately, the voltage and current outputs are available at low impedance Z ports and high impedance X ports of the used CVCIIs, respectively. It must be mentioned that although outputs in both the forms of current and voltage signals are produced, current and voltage signals of the same type are not simultaneously available. This can be considered as the main limitation of the proposed circuit. It also employs a floating capacitor, which is not desirable from the integration point of view.

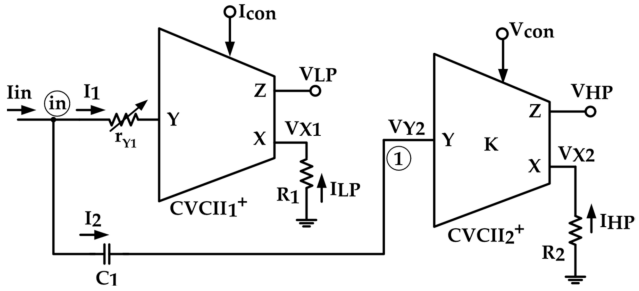



**Figure 3.** The proposed LP/HP filter topology.

## 3. Nonideal Analysis

The matrix operation of the used CVCII+s in a nonideal condition is shown in (11). Here, current gain between Y and X ports for $CVCII_1{}^+$ is shown by $\beta$, which has a close to unity value and it is shown by K for $CVCII_2{}^+$, which is controllable by $V_{con}$. The nonideal voltage gain between the X and Z ports for $CVCII_1{}^+$ and $CVCII_2{}^+$ is shown by $\alpha$ with a value close to unity. The parameters $r_x$ and $r_z$ are the parasitic impedances at the X and Z ports. In $CVCII_1{}^+$ $r_y$ is the parasitic impedance at Y port which is controllable by $I_{con}$. For $CVCII_2{}^+$ $r_y$ is a nonzero constant value in the range of a few $\Omega$.

$$\begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix} = \begin{bmatrix} \beta(K) & 1/r_x & 0 \\ 0 & \alpha & r_z \\ r_Y & 0 & 0 \end{bmatrix} \begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} \quad (11)$$

Figure 4 shows the proposed LP/AP filter of Figure 2 in nonideal condition where all parasitic elements are modeled. The parasitic elements related to the $CVCII_1{}^+$ are named $r_{Y1}$ and $r_{X1}$ while those related to the $CVCII_2{}^+$ are named $r_{Y2}$ and $r_{X2}$.

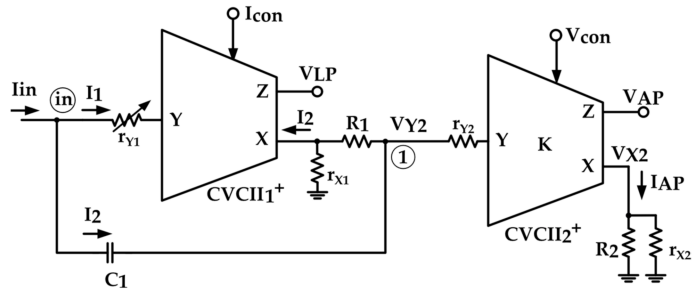



**Figure 4.** The proposed LP/AP filter topology (shown in Figure 2) in nonideal condition.

By assuming $r_{Y2} \ll R_1$ and $r_{Y2} \ll r_{X1}$, we have:

$$I_1 = \frac{1 + sC_1 r_{Y2}}{1 + sC_1 (r_{Y1} + r_{Y2})} I_{in} \quad (12)$$

$$I_2 = \frac{sC_1 r_{Y1}}{1 + sC_1(r_{Y1} + r_{Y2})} I_{in} \tag{13}$$

Using (11)–(13) and assuming $sC_1 r_{Y2} \ll 1$, $V_{x1}$ and $V_{LP}$ are found, respectively, as:

$$V_{X1} \approx -\beta_1 R_1 \left[\frac{1}{1 + sC_1(r_{Y1} + r_{Y2})}\right] I_{in} \tag{14}$$

$$V_{LP} \approx -\beta_1 \alpha_1 R_1 \left[\frac{1}{1 + sC_1(r_{Y1} + r_{Y2})}\right] I_{in} \tag{15}$$

where $\alpha_1$ and $\beta_1$ are related to $CVCII_1{}^+$.

Performing KCL at node 1 and using (14) and (15) results in:

$$I_{AP} \approx \beta_1 K \left[\frac{1 - sC_1(r_{Y1} - \beta_1 r_{Y2})}{1 + sC_1(r_{Y1} + r_{Y2})}\right] I_{in} \tag{16}$$

$$V_{AP} \approx \beta_1 K \alpha_2 (R_2 // r_{X2}) \left[\frac{1 - sC_1(r_{Y1} - \beta_1 r_{Y2})}{1 + sC_1(r_{Y1} + r_{Y2})}\right] I_{in} \tag{17}$$

where K and $\alpha_2$ are current gain and voltage gains related to $CVCII_2{}^{+,}$ respectively. The corresponding phase for the AP outputs is:

$$\varphi(\omega) = 180^\circ - \arctan[\omega C_1(r_{Y1} - \beta_1 r_{Y2})] - \arctan[\omega C_1(r_{Y1} + r_{Y2})] \tag{18}$$

From (18), it is noted that to reduce the effect of parasitic and nonideal elements on AP response, we must have $r_{Y1} \gg r_{Y2}$. This condition is easily met because $r_{Y1}$ and $r_{Y2}$ are in the range of a few kΩ and a few tens of Ω, respectively. The value of $\beta_1$ is also close to unity.

Performing similar nonideal analysis for the LP/HP filter of Figure 3 results:

$$I_{LP} = \beta_1 \frac{1 + sC_1 r_{Y2}}{1 + sC_1(r_{Y1} + r_{Y2})} I_{in} \tag{19}$$

$$V_{LP} = -\beta_1 R_1 \alpha_1 \frac{1 + sC_1 r_{Y2}}{1 + sC_1(r_{Y1} + r_{Y2})} I_{in} \tag{20}$$

$$I_{HP} = K \frac{sC_1 r_{Y1}}{1 + sC_1(r_{Y1} + r_{Y2})} I_{in} \tag{21}$$

$$V_{HP} = -K(R_2 // r_{X2}) \alpha_2 \frac{sC_1 r_{Y1}}{1 + sC_1(r_{Y1} + r_{Y2})} I_{in} \tag{22}$$

## 4. Internal Implementation of the Used CVCIIs

A possible CMOS implementation of the used $CVCII_1{}^+$ is shown in Figure 5a. Although here the current sources are shown as ideal for simplicity, in simulations they are implemented by simple current mirrors. The input section at the Y port is composed of the common gate transistor $M_2$. The current sources $I_{B1}$ and $I_{B2}$ are used for biasing purposes, while $I_{con}$ is a variable current source which is used to set the value of impedance at the Y port. The diode connected transistor $M_1$ provides proper bias voltage at $M_1$ gate. The impedance at Y port can be expressed as:

$$r_{Y1} = \frac{1}{gm_{M2}} \tag{23}$$

where $gm_{M2}$ (with usual meaning of symbols) is:

$$gm_{M2} = \sqrt{\mu C_{ox} \frac{W_{M2}}{L_{M2}} I_{con}} \tag{24}$$

As is seen from (24), the value of $gm_{M2}$ is controllable by $I_{con}$. Therefore, the appropriate value of the Y port impedance can be achieved by setting the value of $I_{con}$. To set zero offset voltage at the Y port, $I_{con}$ is also applied to the drain of $M_1$, so the DC value of gate–source voltage of $M_1$ and $M_2$ is kept equal, resulting in zero DC offset voltage at Y port.

The input current applied to the Y terminal is transferred to the X terminal through a simple current mirror made of $M_3$–$M_4$. The voltage produced at the X port is transferred to the Z port through voltage buffer made of $M_5$–$M_9$ transistors. Here, the low impedance at the Z port is provided by negative feedback loop realized by $M_9$. The $CVCII_2{}^+$ shown in Figure 5b is formed by a series connection of a current buffer made of $M_1$–$M_7$, $M_{6C}$–$M_{7C}$ transistors and a voltage buffer formed by $M_8$–$M_{12}$ transistors. The required low impedance at the Y terminal is provided by negative feedback loop established with $M_5$. By connecting the gate of $M_1$ at the ground, the DC value of the Y port offset voltage is set at ground. The used degenerated current mirror, made of $M_6$, $M_{6C}$, $M_7$, $M_{7C}$ transistors, transfers the input current from Y to X terminals. As it was previously used in [39,40], by setting the value of $V_{con}$, the gain of the current mirror is tuned resulting in a variable current gain between Y and X ports. The current gain between X and Y terminals (K) is expressed by (25) with usual meaning of symbols.

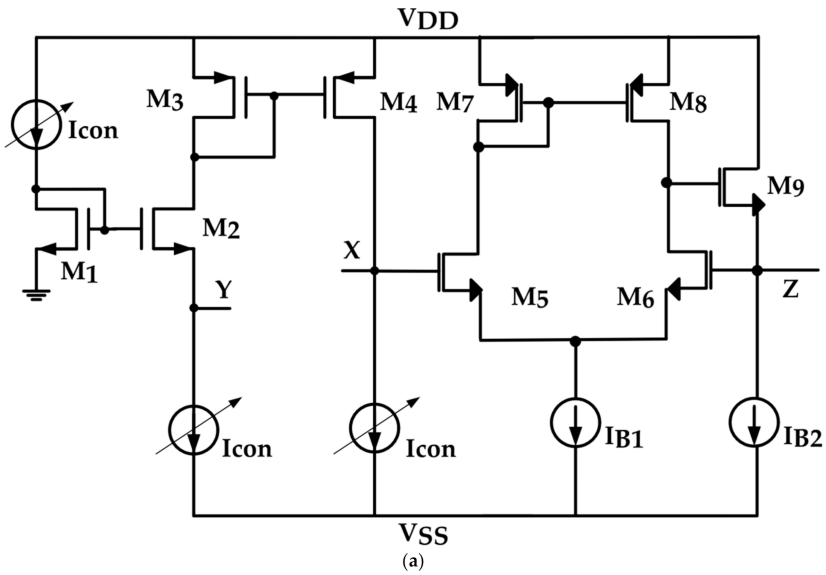
$$K = \frac{gm_{M6}}{gm_{M7}} \frac{1 + gm_{M6} rds_{M6C}}{1 + gm_{M7} rds_{M7C}} \tag{25}$$

Similar to $CVCII_1{}^+$ of Figure 5a, in the voltage buffer section, the voltage produced at the X terminal is transferred to the Z terminal through voltage buffer formed by the $M_8$–$M_{12}$ transistors. The negative feedback loop made of $M_{12}$ provides low impedance at the Z port.

being:

$$rds_{M7c} = \frac{1}{\mu C_{ox} \frac{W_{M7C}}{L_{M7C}} (V_{dd} - V_{con} - |V_{THP}|)} \tag{26a}$$

$$rds_{M6c} = \frac{1}{\mu C_{ox} \frac{W_{M6C}}{L_{M6C}} (V_{dd} - |V_{THP}|)} \tag{26b}$$




(a)

**Figure 5.** *Cont*.

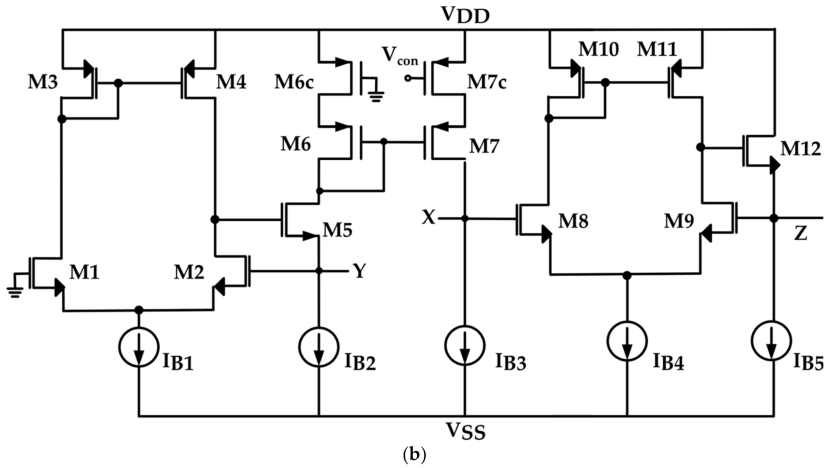



**Figure 5.** CMOS implementation of the used (**a**) $CVCII_1{}^+$ and (**b**) $CVCII_2{}^+$.

## 5. Simulation Results

The proposed electronically tunable LP/AP filter of Figure 2 and LP/HP filter of Figure 3 has been simulated using SPICE and 0.18 µm CMOS technology parameters and supply voltage of ±0.9 V. The used transistors aspect ratios are reported in Table 1. The values of the bias current sources which are realized by simple current mirrors are reported in Table 2. The performance parameters of $CVCII_1{}^+$ and $CVCII_2{}^+$ are summarized in Table 3. The variation of $CVCII_1{}^+$ Y port impedance ($r_{Y1}$) by $I_{con}$ is shown in Figure 6. As is seen, by increasing $I_{con}$ from 0.5 µA to 50 µA the value of $r_{Y1}$ varies from 45 kΩ to 3.5 kΩ. The variation of $CVCII_1{}^+$ power consumption is from 0.101 mW to 0.423 mW for $I_{con}$ = 0.5 µA and $I_{con}$ = 50 µA, respectively. The variation of $CVCII_2{}^+$ current gain K versus $V_{con}$ is shown in Figure 7. As is seen, K falls from 30 to 1 while $V_{con}$ varies from −0.9 V to 0.185 V. The variation of $CVCII_2{}^+$ power consumption is 0.284 mW and 0.634 mW for $V_{con}$ = 0.185 V and $V_{con}$ = −0.9 V, respectively.

In the filters presented in Figures 2 and 3 we have set the values of $C_1$, $R_1$ and $R_1$ as 20 pF, 15 kΩ and 1 kΩ, respectively. The frequency performance of LP output for three different values of $I_{con}$ is shown in Figure 8. It is seen that the −3 dB frequency is 89 kHz, 370 kHz and 1 MHz for $I_{con}$ = 0.5 µA, $I_{con}$ = 5 µA and $I_{con}$ = 50 µA, respectively. The low frequency gain value is about 83 dB. To test the time domain response of LP output, a sinusoidal input signal with peak to peak value of 10 µA and frequency of 1 MHz is used as input signal with $I_{con}$ = 50 µA. The resulted total harmonic distortion (THD) is shown in Figure 9, which shows maximum value of 8% for THD at LP output.

**Table 1.** $CVCII_1{}^+$ and $CVCII_2{}^+$ main transistors aspect ratio and bias currents.

| | W, L | |
|---|---|---|
| | **$CVCII_1{}^+$** | **$CVCII_2{}^+$** |
| $M_1$, $M_2$ | 4.5 µm, 4.5 µm | 7.2 µm, 1.8 µm |
| $M_3$, $M_4$ | 90 µm, 1.8 µm | 9 µm, 1.8 µm |
| $M_5$ | 3.6 µm, 1.8 µm | 270 µm, 0.9 µm |
| $M_6$ | 3.6 µm, 1.8 µm | 5.04 µm, 0.54 µm |
| $M_7$ | 9 µm, 1.8 µm | 50.4 µm, 0.54 µm |
| $M_8$ | 9 µm, 1.8 µm | 7.2 µm, 1.8 µm |
| $M_9$ | 360 µm, 0.9 µm | 7.2 µm, 1.8 µm |
| $M_{12}$ | - | 270 µm, 0.9 µm |
| $M_{6c}$ | - | 0.9 µm, 0.54 µm |
| $M_{7c}$ | - | 9 µm, 0.54 µm |
| $M_{10}$, $M_{11}$ | - | 9 µm, 1.8 µm |
| $I_{b1}$, $I_{b2}$ | 30 µA,30 µA | 28 µA,7 µA |
| $I_{b3}$, $I_{b4}$, $I_{b5}$ | - | 70 µA, 28 µA, 7 µA |

**Table 2.** Performance parameters of the designed $CVCII_1^+$ and $CVCII_2^+$.

| | $CVCII_1^+$ | $CVCII_2^+$ |
|---|---|---|
| $R_Y$ | From 45 KΩ ($I_{con}$ = 0.5 μA) to 3.5 KΩ ($I_{con}$ = 50 μA) | 81 Ω |
| $R_X$ | From 1.6 MΩ ($I_{con}$ = 0.5 μA) to 286 KΩ ($I_{con}$ = 50 μA) | From 1 MΩ ($V_{con}$ = 0 V) to 96 kΩ ($V_{con}$ = −0.9 V) |
| $C_Y$ | From 117 fF ($I_{con}$ = 5 μA) to 123 fF ($I_{con}$ = 50 μA) | 3.3 fF |
| $R_Z$ | 54 Ω | 57 Ω |
| DC offset at Y | 11 mV | 2.6 mV |
| DC offset at Z | 5 mV | 6 mV |
| DC offset at X | 6 mV | −2.4 mV |
| A | 0.985 | 0.989 |
| B | 0.993 for $I_{con}$ = 0.5 μA and 0.965 for $I_{con}$ = 50 μA | 9.5 |
| Power | 101 μW for $I_{con}$ = 0.5 μA to 423 μW for $I_{con}$ = 50 μW | From 284 μW for $V_{con}$ = 0.185 V to 634 μW for $V_{con}$ = −0.9 V |

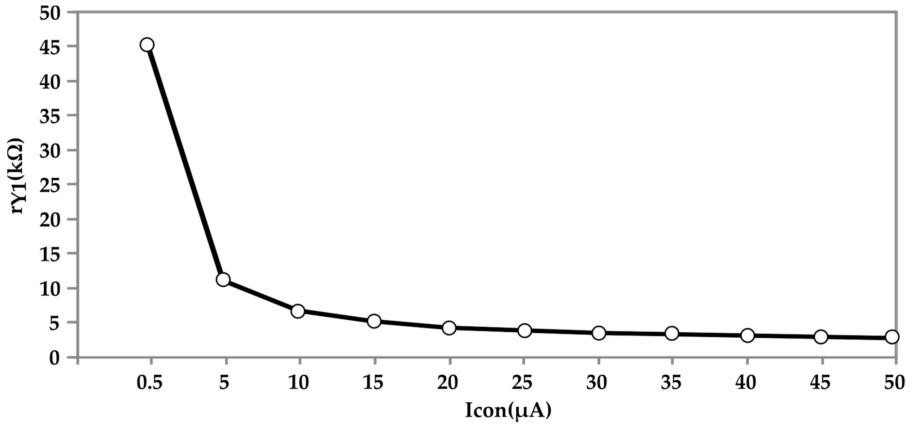



**Figure 6.** Variation of $r_{Y1}$ as a function of $I_{con}$ for $CVCII_1^+$.

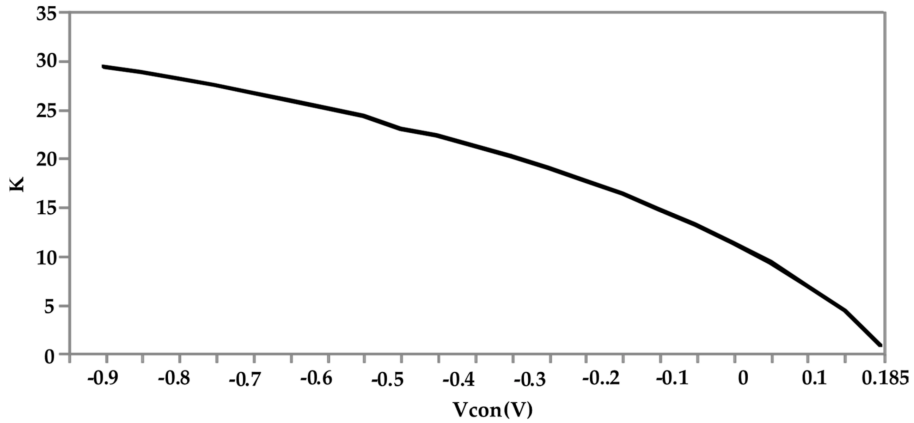



**Figure 7.** Variation of K as a function of $V_{con}$ for $CVCII_2^+$.

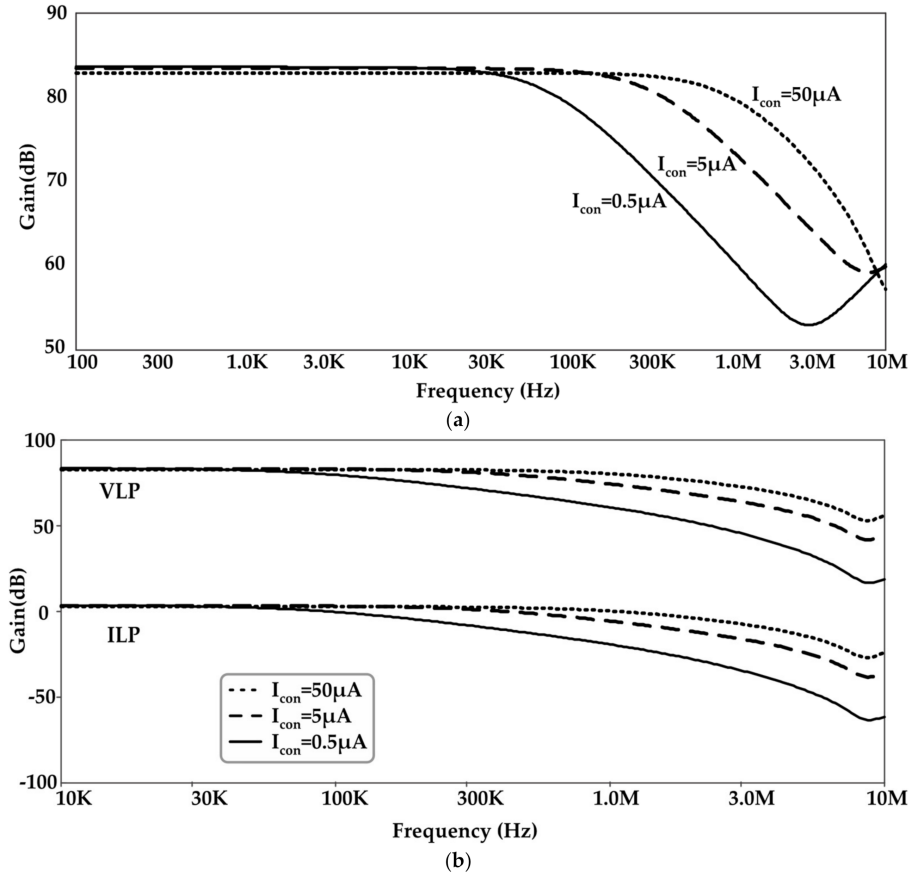



**Figure 8.** Frequency performance of LP output for different values of $I_{con}$ for the filters represented in Figures 2a and 3b.

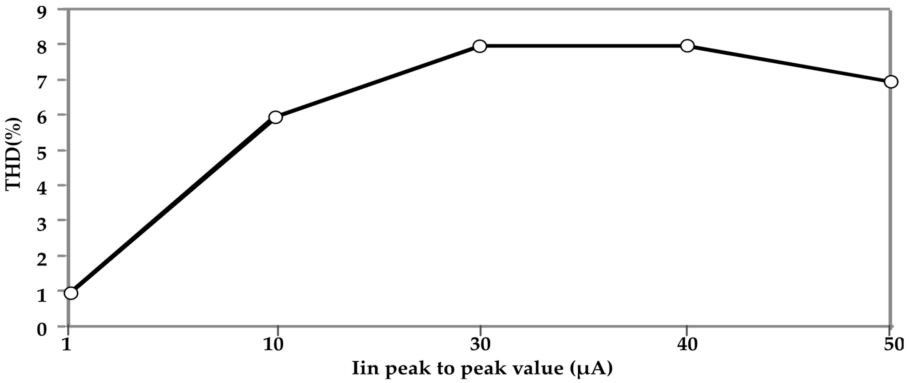



**Figure 9.** Low-pass (LP) output total harmonic distortion (THD) value for a sinusoidal input signal with frequency of 1 MHz ($I_{con}$ = 50 μA) at different values of input signal for the filter reported in Figure 2.

Figure 10 shows the gain and phase frequency performances of the $I_{AP}$ and $V_{AP}$ outputs for different values of $I_{con}$ and $V_{con}$ from which the electronic tunability of both frequency and gain is evident. To examine the time domain performance of the proposed AP filter, a sinusoidal input with peak-to-peak amplitude of 2 μA and frequency of 1 MHz is applied to the proposed circuit. For $I_{con}$ = 50 μA and $V_{con}$ = 0 V, the input and output signals are shown in Figure 11, where an 87° phase shift for both produced $I_{AP}$ and $V_{AP}$ is found. In this case, THD is 2%.

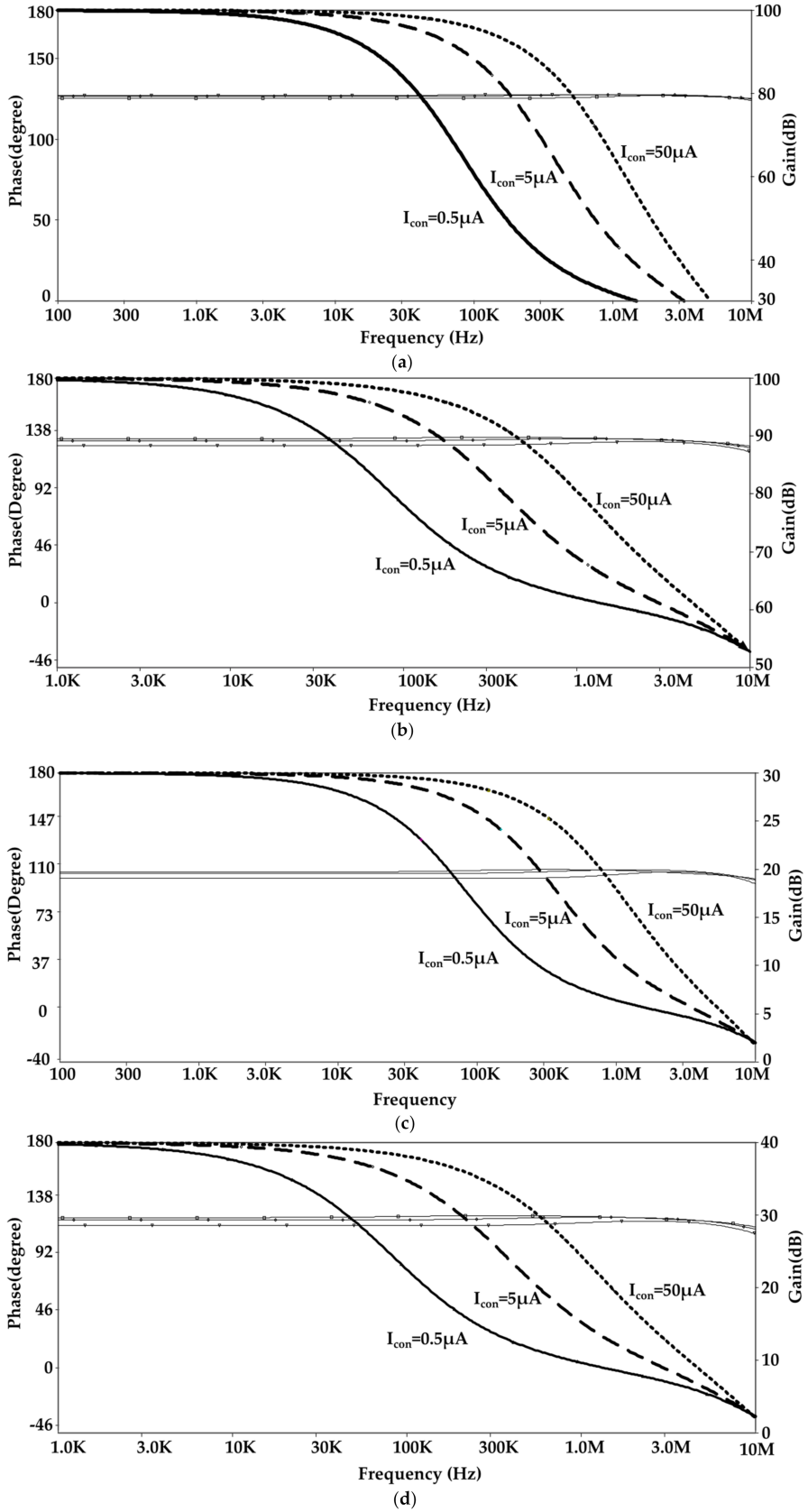



**Figure 10.** Gain and phase frequency response of (**a**) $V_{AP}$ for $V_{con}$ = 0 V, (**b**) $V_{AP}$ for $V_{con}$ = −0.9 V, (**c**) $I_{AP}$ for $V_{con}$ = 0 and (**d**) $I_{AP}$ for $V_{con}$ = −0.9 V.

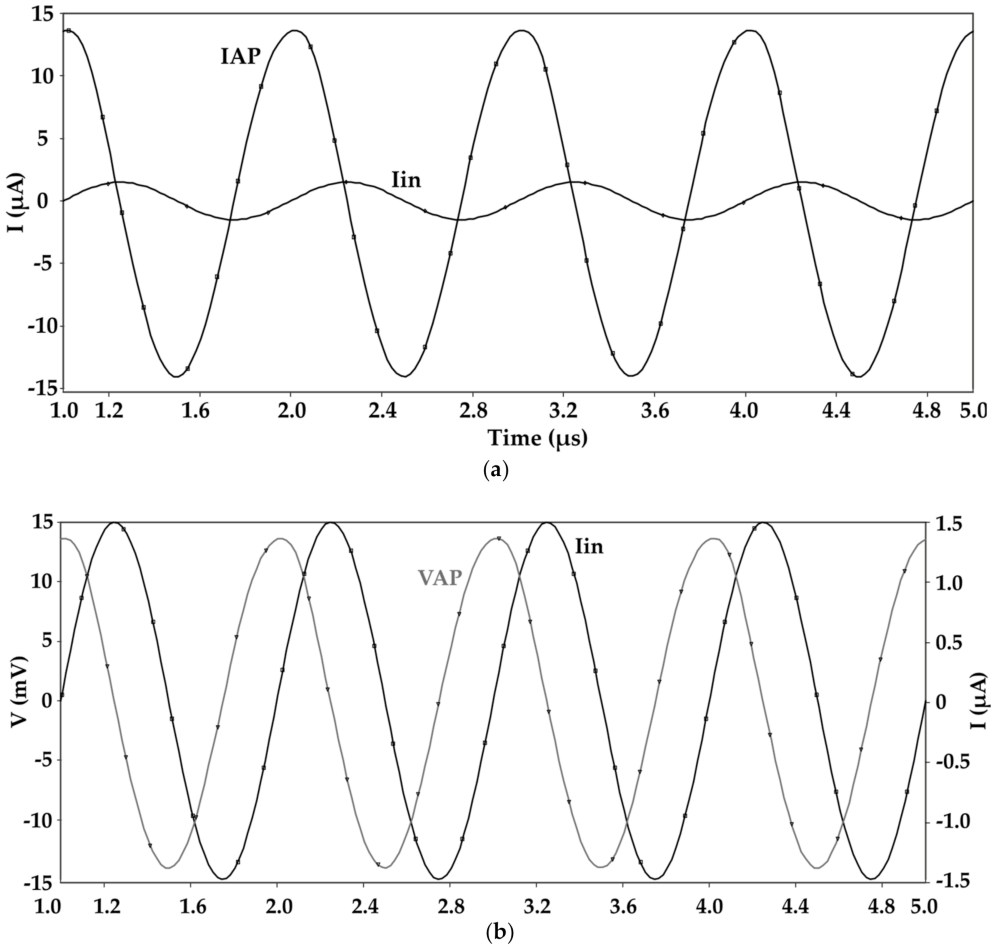



**Figure 11.** Time domain outputs for (**a**) $I_{AP}$ and (**b**) $V_{AP}$ in the case of $I_{con}$ = 50 μA and $V_{con}$ = 0 V.

Figure 12 reports the frequency performances of $I_{HP}$ and $V_{HP}$ outputs for different values of $I_{con}$ and $V_{con}$. The value of $f_0$ for HP outputs is 81 kHz, 360 kHz and 1 MHz for $I_{con}$ = 0.5 μA, 5 μA and 50 μA, respectively. The gain of $I_{HP}$ varies from 0.980 dB to 29 dB for $V_{con}$ variation from 0.185 V to −0.9 V. For $V_{HP}$ gain, variation is from 60 dB to 88.9 dB. The THD values are 7.7% and 10% for $I_{HP}$ and $V_{HP}$ for input signal of 1 MHz and 5 μA peak to peak value and $I_{con}$ = 50 μA and $V_{con}$ = −0.9 V.

A comparison between the proposed circuit and other previously reported ones is given in Table 3. As is seen, the proposed circuit offers many advantages, such as full electronic controllability, being free from any matching condition, versatility for providing both current and voltage signals, providing both LP and AP outputs and simple implementation compared to the available works. However, the proposed circuit employs a floating capacitor, which is not desirable from an integration point of view.

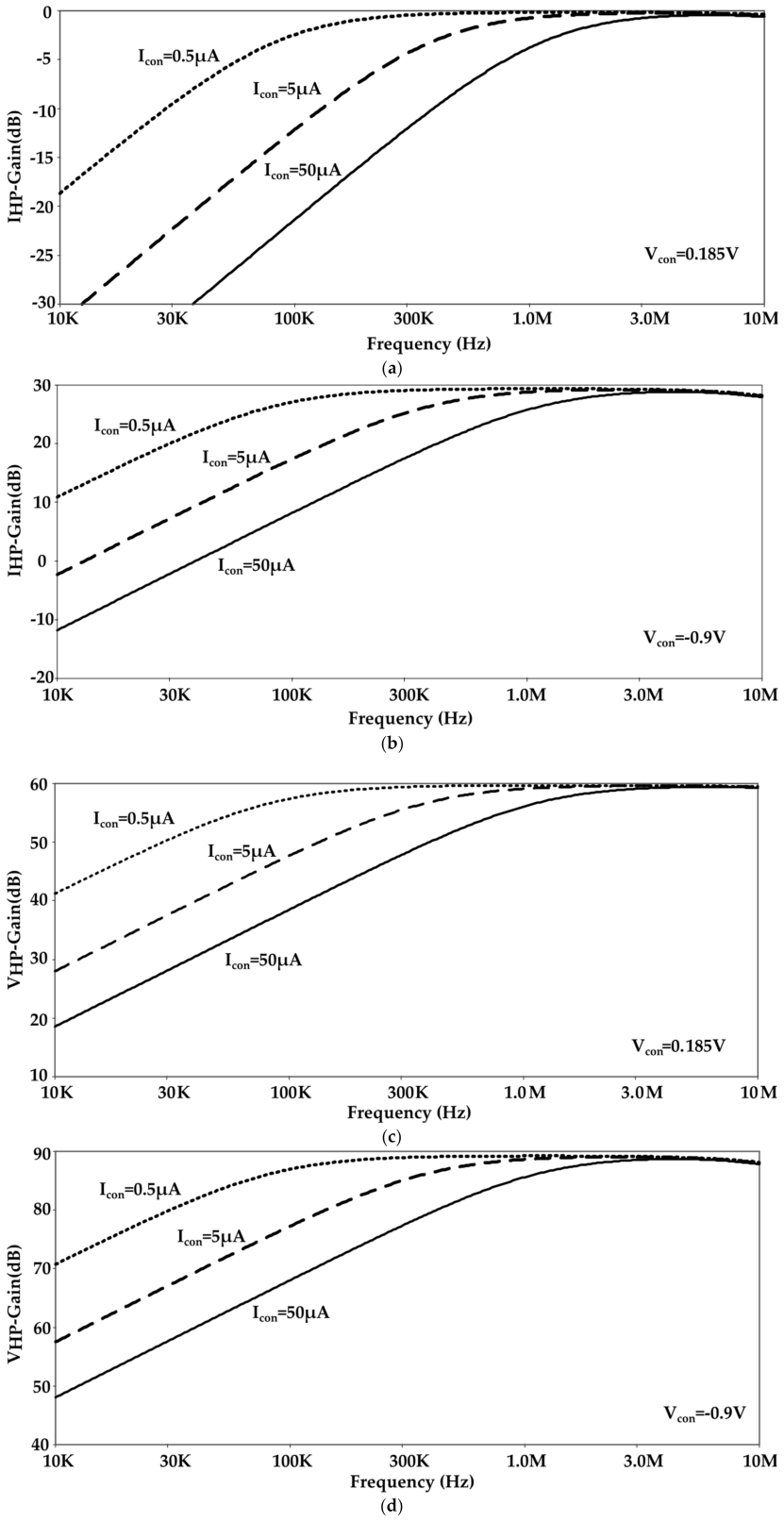



**Figure 12.** Gain frequency response of (**a**) $I_{HP}$ for $V_{con}$ = 0.185 V (**b**) $I_{HP}$ for $V_{con}$ = −0.9 V (**c**) $V_{HP}$ for $V_{con}$ = 0.185 V and (**d**) $V_{HP}$ for $V_{con}$ = −0.9 V at three different values of $I_{con}$ for the filter proposed in Figure 3.

**Table 3.** Comparison between proposed circuit and other circuits reported in the literature.

| Ref | ABB | #R | Floating C | # Transistors | $V_{DD}$ $V_{SS}$ | Pd (W) | Output | Match | Electronic Tunability | | $f_0$(Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | $f_0$ | G | |
| [1] | 1DXCCII | 2 | Yes [1] | 20 | ±1.25 V | 2.1 m | $V_{AP}$ [2] | Yes | No | No | 1.59 M |
| [2] | 1DDCCII | 1 | Yes/No [3] | 18 | ±2.5 V | NA [4] | $V_{AP}$ [2] | No | No | No | 10 M |
| [10] | DV-DXCCII | 2 | Yes [1] | 30 | ±1.25 V | NA | $V_{AP}$ [2] | Yes | No | No | 6.133 M |
| [12] | 3CA | 1 | Yes | 120 | ±5 V | 25.7 m | $I_{AP}$ | No | No | Yes | 100 k |
| [17] | 1Dx-MOCCII | 1 | Yes | 40 | ±1.25 V | NA | $\pm I_{AP}/I_{HP}/I_{LP}$ | No | No | No | 7.962 M |
| [18] | 2OFCC | 2 | No | 42 | ±1.5 V | NA | $I_{HP}/I_{LP}/I_{AP}$ | Yes | No | No | 159 K |
| [19] | 1DD-DXCCII | 3 | Yes | 30 | ±1.2 V | NA | $I_{HP}/I_{LP}/I_{AP}$ | Yes | No | No | 6.43 M |
| [21] | Current Mirror | 0 | No | 10 | ±0.9 V | 0.266 m | $I_{AP}$ | No | Yes | No | 3 M |
| [22] | 1ICCII | 0 | Yes | 44 | ±0.75 V | 2.75 m | $I_{LP}/I_{AP}/I_{HP}$ | No | Yes | No | 2.6 M |
| [23] | Current Mirror | 0 | No | 8 | +1.5 | 0.169 m | $I_{AP}/I_{HP}$ | No | Yes | No | 159 k |
| [24] | 2CCCII | 0 | Yes | 35 | ±2.5 V | NA | $+I_{AP}/-I_{AP}$ | No | Yes | No | 4.8 M |
| [25] | 2CDTA | 0 | Yes | 84 | ±2 V | 9 m | $+I_{AP}/-I_{AP}$ | No | Yes | No | 1 M |
| [26] | 2CCCCTA | 0 | No | 54 | ±2.5 V | NA | $I_{AP}$ | No | Yes | Yes | <1 M |
| [27] | Modified CCCII | 0 | No | 42 | ±2.5 V | NA | $I_{AP}$ | No | Yes | No | 1 M |
| [28] | 2CCCII | 0 | Yes | 38 | NA | NA | $I_{AP}$ | No | Yes | No | 58 k 200 kHz |
| [29] | 1Do-CCCII | 0 | Yes [1] | 42 | ±3 V | NA | $+I_{AP}/-I_{AP}$ | Yes | Yes | No | 1.632 M |
| [30] | 1CCCTA | 1 | Yes [1] | 25 | ±1.5 V | NA | $I_{AP}$ | No | Yes | Yes | 1.66 M |
| [31] | 1CFCTA | 1 | No | 35 | ±1.25 V | 5.5 m | $\pm I_{LP}$ | No | Yes | Yes | 2 M |
| [32] | 1CA+2CB | 0 | Yes | 46 | ±1.2 V | 3.88 m 5.29 m | $I_{AP}$ | No | Yes | Yes | 1.41 M |
| [35] | $1VCII^{\pm}$+$1VCII^{+}$ | 3 | No | 34 | ±0.9 V | 0.489 m | $V_{AP}/I_{AP}$ | Yes | No | No | 1 M |
| Proposed#1 | $2CVCII^{+}$ | 2 | Yes | 36 | ±0.9 V | 0.385 m 1.057 m | $I_{AP}/V_{AP}/V_{LP}$ | No | Yes [5] | Yes | 89 K–1 M |
| Proposed#2 | $2CVCII^{+}$ | 2 | Yes | 36 | ±0.9 V | 0.385 m 1.057 m | $I_{HP}/V_{HP}/V_{LP}/I_{LP}$ | No | Yes | Yes | 89 K–1 M |

[1] Two floating compensation capacitors are used in the internal structure of the used active building blocks (ABB); [2] Additional voltage buffer is required for $V_{AP}$ output; [3] There are two structures one with floating C and one without; [4] Not Available; [5] Only for AP outputs.

## 6. Conclusions

Two new electronically tunable first order LP/AP and LP/HP filter topologies based on two CVCIIs, two resistors and one capacitor have been presented. The first topology produces $V_{LP}/I_{AP}/V_{AP}$ outputs and second topology produces $I_{LP}/V_{LP}/I_{HP}/V_{HP}$ outputs. The $f_0$ of LP output is electronically tunable while both $f_0$ and gain of AP and HP outputs are fully electronically tunable using electronically variable VCII. The value of $f_0$ is controlled by $I_{con}$, which is used to vary the Y port impedance of the first CVCII. The gains are also controlled by $V_{con}$, which is used to change the current gain of the second CVCII. The circuit is free from any matching condition. The total number of used transistors is only 36. Due to the circuit's simplicity, the proposed circuit enjoys high frequency performance compared to its counterparts. The only drawback of the proposed circuit is that it employs a floating capacitor.

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