Three-Port High Step-Up and High Step-Down DC-DC Converter With Zero Input Current Ripple

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***Abstract*—In this article, a nonisolated three-port dc–dc converter with high voltage conversion ratio is proposed. In the proposed converter, by changing the place of input voltage source between each of the three ports, three different single-input two-output operation modes are achieved. The input current ripple of the proposed converter is eliminated at the low voltage side for the whole range of duty cycles. The voltage conversion ratios of the proposed converter can be increased by increasing the turns ratio of second winding of coupled inductors. Moreover, the proposed converter has achieved proper output voltage regulations for all output ports, simultaneously. The proposed converter can be utilized in the renewable energy conversion systems such as in photovoltaic and fuel cells. In this article, the voltage conversion ratios of the output ports, the voltage stress on switches, the average currents of switches and inductors, and the required condition for cancelling input current ripple at low voltage side are calculated theoretically. The theoretical results are verified and experimental results for 24 V input voltage and 304 V, 240 V output voltages with 400 W power are extracted for two different operation modes.**

***Index Terms*—Coupled-inductor based converter, dc–dc single-input/two-output converter, high voltage gain, input current ripple cancellation, three-port converter.**

I. Introduction

NOWADAYS, due to the wide use of different renewable energy sources, such as photovoltaic (PV), fuel cell (FC), etc., and applying them as hybrid renewable energy sources, the multiport dc–dc converters, have obtained more attention and play a significant role in interfacing the generated powers [1]–[4]. Multiport dc–dc converters have the capability of interfacing different dc voltage levels and transfer high volume of power to the output loads, where this feature is more interesting in the renewable energy systems [5], [6]. In the case of grid-connected renewable energy sources, the different output dc voltage levels of multi-output converter are connected to dc–ac inverters [7], [8]. Utilizing coupled inductors in dc converters is an effective approach to increase the conversion ratio of the converter. In the coupled inductor-based converters, by increasing the turns ratio of the secondary winding of the coupled inductors, the voltage conversion ratios would be increased [9], [10]. Moreover, the dc–dc converters with low or zero input current ripple would be preferred for use in the PV or FC and generally renewable energy sources [11].

The interleaved converters have the capability of reducing the input current ripple [12], [13]. However, for example, in the interleaved two-phase converters have complicated control systems for output voltage regulation. On the other hand, in some cases, by using coupled inductors, the input current ripple is decreased or eliminated thoroughly [14], [15]. The main constraint of the converters in [14] and [15] is their complicated control abilities. The presented multiport dc–dc converters in [16] and [17] have low input current ripples, but the presented converter in [18] has higher input current ripple. In [19]–[23] single-input, two-output dc–dc converters are presented, which have two stepped-up voltages at their output ports. However, the disadvantage of the converters in [19]–[22] is the low voltage gain. The presented three-port dc–dc converter in [24] has low voltage gain and the converter suffers from pulsating input current. Three-port dc–dc converters with a battery as a storage in one port is presented in [25]–[29]. In [26]–[28], three-port dc–dc converters based on coupled inductors are presented. The conversion ratios of these converters are high. In [29], a transformer-based three-port dc converter is presented. This converter suffers from high voltage stress on its semiconductor elements.

In this article, a new nonisolated three-port high voltage gain dc–dc converter with zero input current ripple at low voltage side is proposed. In the proposed converter, by changing the place of input voltage source between each of the three ports, three different operations with single-input and two-output structures are achieved. The proposed converter is analyzed. Finally, the analytical results are reconfirmed by using experimental results.

II. Proposed Converter

The power circuit of the proposed converter and its equivalent power circuit using a transformer model of the coupled

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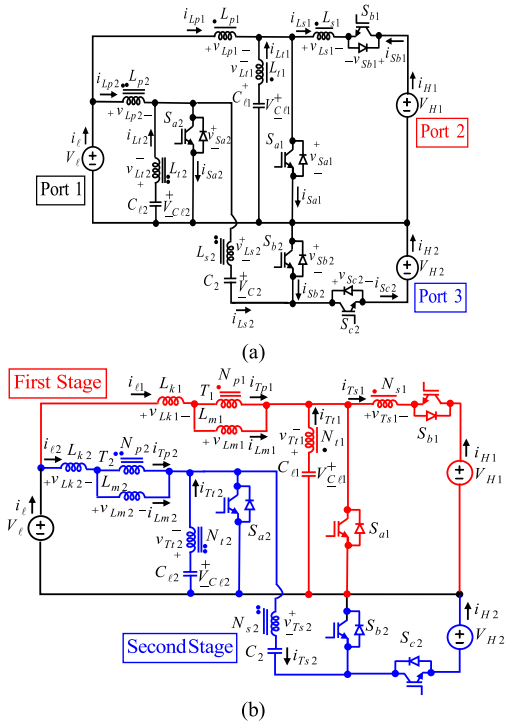

Fig. 1. Proposed three-port converter and its equivalent power circuit. (a) Converter Topology. (b) Equivalent power circuit.

inductors are shown in Fig. 1(a) and (b), respectively. In Fig. 1(a), three-winding coupled inductor consists of the inductances L_{p1} as first winding, L_{s1} as second winding, L_{t1} as third winding, and the mutual inductances M_{ps1}, M_{pt1}, M_{st1} as the coupling inductances between two windings of coupled inductor. By using a transformer model of the coupled inductors in Fig. 1(b) it can be seen that the first coupled inductor is modeled with the magnetizing inductor of L_{m1}, which is paralleled with the transformer T_1 and placed in series with the leakage inductance of L_{k1}. The first, second, and third windings of transformer T_1 has N_{p1}, N_{s1} and N_{t1} turns, respectively. The turns ratio of the second and third windings of transformer T_1 is considered as $n_{s1} = N_{s1}/N_{p1}$ and $n_{t1} = N_{t1}/N_{p1}$. The capacitors $C_{\ell 1}$, $C_{\ell 2}$, and C_2 are assumed to be large enough, so, the voltages across them are considered to be constant values as $V_{C\ell 1} = V_\ell$, $V_{C\ell 2} = V_\ell$, V_{C2}, respectively. Fig. 2 illustrates the theoretical waveforms of the proposed converter for duty cycle condition of $D_1 > D_2$. Based on Fig. 2, the proposed converter has three modes during a switching period. Note that in the analysis, $i_{Lp1} = i_{\ell 1}$ and $i_{Lp2} = i_{\ell 2}$. The proposed converter has three different operations with single-input, two-output ports which are named as boost, buck and buck-and-boost operations. The equivalent power circuits of these operations during a switching period for $D_1 > D_2$ are shown in Figs. 3, 4, 5 respectively. In boost operation, the low voltage V_ℓ is utilized as the input voltage source. In buck operation, the voltage V_{H1} is considered as input voltage source. In buck and boost operation, the voltage V_{H2} is considered as input voltage source.

The illustrations of the second modes for all operations of the proposed converter when $D_2 > D_1$ is shown in Fig. 6. Note that

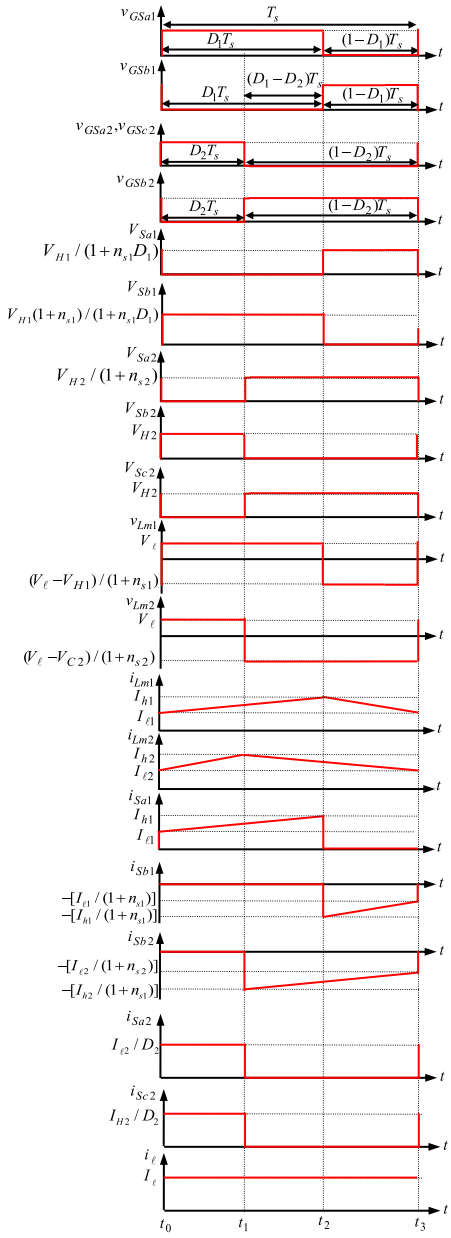

Fig. 2. Theoretical waveforms of the proposed converter during a switching period for $D_1 > D_2$.

the equivalent circuits for the first and third modes in $D_2 > D_1$ are same as the ones for $D_1 > D_2$ in all three boost, buck and buck-and-boost operations of the converter. Also, it is considered that $V_{H1} > V_{H2} > V_\ell$.

III. Analysis of the Proposed Converter

A. Analysis of First Stage Circuit

In this part, the analysis of proposed converter during a switching period at the both first and second stages of the proposed converter in Fig. 1(b) is given. For simplifying the equations, the required conditions of achieving zero input current ripple at the low voltage side (i_ℓ) ($n_{t2} = n_{t1} = 1$), which are explained in details in Section III-D.

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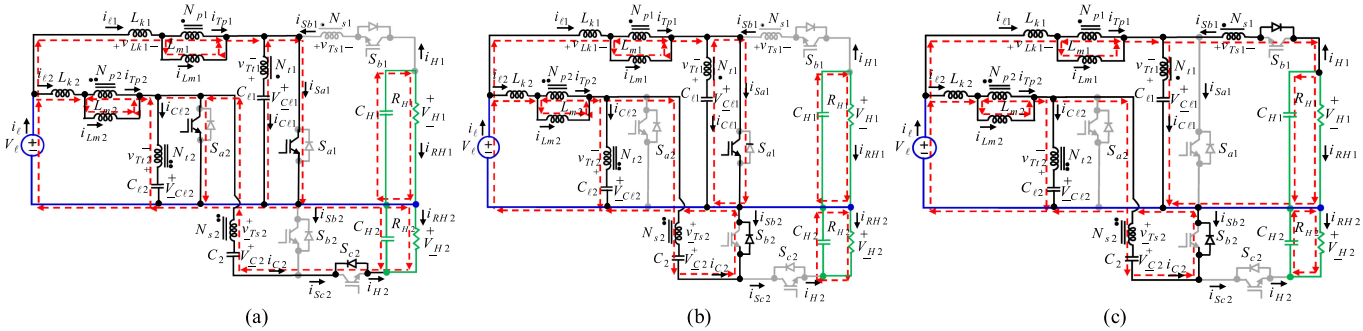

Fig. 3. Equivalent power circuit of the boost operation during a switching period for $D_1 > D_2$. (a) Mode 1. (b) Mode 2. (c) Mode 3.

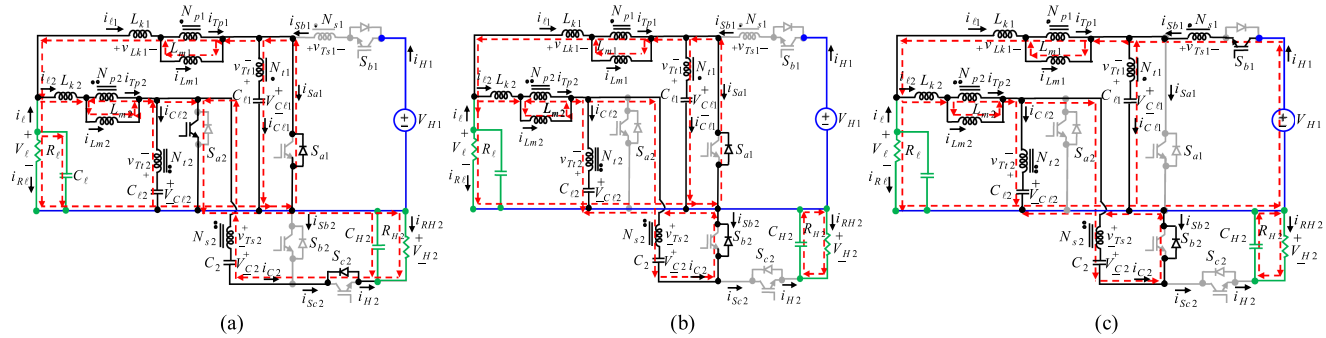

Fig. 4. Equivalent power circuits of buck operation during a switching period for $D_1 > D_2$. (a) Mode 1. (b) Mode 2. (c) Mode 3.

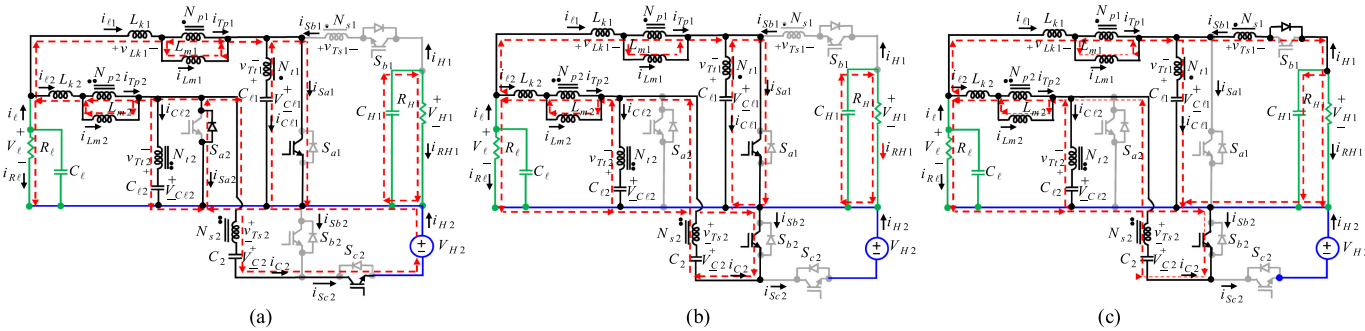

Fig. 5. Equivalent power circuit of buck-and-boost operation during a switching period for $D_1 > D_2$. (a) Mode 1. (b) Mode 2. (c) Mode 3.

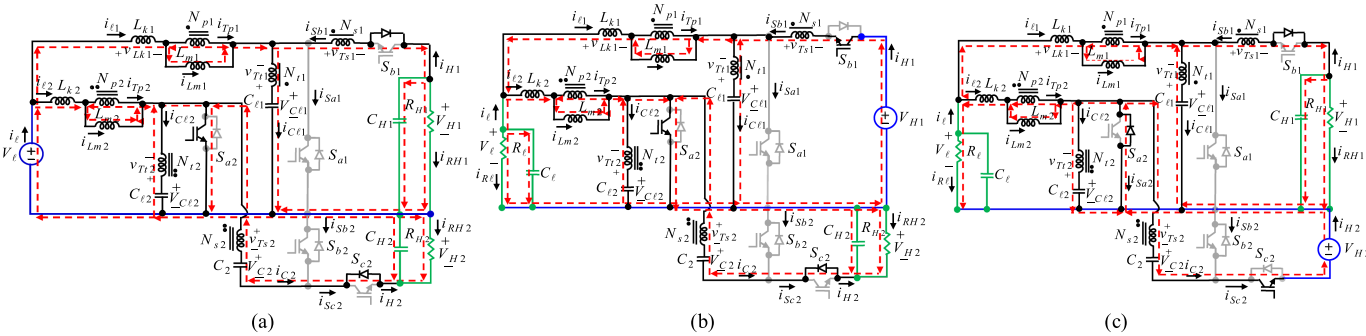

Fig. 6. Equivalent power circuit of boost, buck, buck-and-boost operations during mode 2 for $D_2 > D_1$. (a) Boost operation. (b) Buck operation. (c) Buck-and-boost operation.

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Time Interval of $0 < t < D_1T_s$*:* This state is shown in Fig. 3(a) and (b). Therefore, based on $n_{t1} = 1$, the voltage v_{Lm1} is equal to V_ℓ. As a result, the inductor current can be as follows:

$$i_{Lm1} = (V_\ell/L_{m1})(t - t_0) + i_{Lm1}\,|_{t=t_0}\ . \tag{1}$$

The current of i_{Sa1} is calculated as $i_{Sa1} = i_{Lm1}$.

Time Interval of $D_1T_s < t < T_s$*:* This state is indicated in Figs. 3(c) and 6(a). Therefore, the voltage v_{Lm1} is calculated as $(V_\ell - V_{H1})/(1 + n_{s1})$. Then, the inductor's current can be written as follows:

$$i_{Lm1} = [(V_\ell - V_{H1})/(1+n_{s1})](t - t_0)/L_{m1} + i_{Lm1}\,|_{t=D_1T_s}\ . \tag{2}$$

IV. Steady State Analysis of First Stage

In steady state, the voltage balance law for the inductor L_{m1} can be written as follows:

$$\tilde{v}_{Lm1} = D_1V_\ell + (1 - D_1)(V_\ell - V_{H1})/(1 + n_{s1}) = 0. \tag{3}$$

By simplifying the above equation, the first voltage conversion ratio of $G_1 = V_{H1}/V_\ell$ is obtained as follows:

$$G_1 = V_{H1}/V_\ell = (1 + n_{s1}D_1)/(1 - D_1). \tag{4}$$

The voltage stress on switches S_{b1} and S_{a1} are calculated as follows:

$$V_{Sb1} = n_{s1}V_\ell + V_{H1} = V_{H1}(1 + n_{s1})/(1 + n_{s1}D_1) \tag{5}$$

$$V_{Sa1} = V_\ell - v_{Lm1} = V_\ell/(1 - D_1) = V_{H1}/(1 + n_{s1}D_1). \tag{6}$$

At the steady state, the current balance law for the capacitor $C_{\ell 1}$ can be written as follows:

$$\tilde{i}_{C\ell 1} = D_1(I_{\ell 1} - i_{Lm1}) + (1 - D_1)[I_{\ell 1} - i_{Lm1}/(1 + n_{S1})] = 0. \tag{7}$$

By simplifying the above equation, the average inductor current of i_{Lm1} can be obtained as follows:

$$I_{Lm1} = (1 + n_{s1})(-I_{H1})/(1 - D_1). \tag{8}$$

Consequently, the average current of $I_{\ell 1}$ would be obtained as follows:

$$I_{\ell 1} = (1 + n_{s1}D_1)(-I_{H1})/(1 - D_1). \tag{9}$$

A. Analysis of Second Stage Circuit

Interval time of $0 < t < D_2T_s$*:* This state is shown in Figs. 3(a) and 6(a). Therefore, considering $n_{t2} = 1$, the inductor current can be obtained as:

$$i_{Lm2} = (V_\ell/L_{m2})(t - t_0) + i_{Lm2}\,|_{t=t_0}\ . \tag{10}$$

Based on Fig. 1(b), the average currents of i_{Sa2} and i_{Sc2} in steady state are calculated as $I_{Sa2} = I_{\ell 2}$ and $I_{Sc2} = I_{H2}$, respectively.

Interval time of $D_2T_s < t < T_s$*:* This state is shown in Figs. 3(b) and 3(c). As a result, the voltage v_{Lm2} is obtained as $(V_\ell - V_{C2})/(1 + n_{s2})$. Therefore, it can be written that

$$i_{Lm2} = [(V_\ell - V_{C2})/(1+n_{s2})](t - t_0)/L_{m2} + i_{Lm2}\,|_{t=D_2T_s}. \tag{11}$$

The current of switch i_{Sb2} is calculated as $i_{Sb2} = -i_{Lm2}/(1 + n_{s2})$.

B. Steady-State Analysis of Second Stage

At steady state, the voltage balance law for the inductor L_{m2} can be written as follows:

$$\tilde{v}_{Lm2} = D_2V_\ell + (1 - D_2)(V_\ell - V_{C2})/(1 + n_{s2}) = 0. \tag{12}$$

By simplifying the above equation the voltage V_{C2} is obtained as follows:

$$V_{C2} = (1 + n_{s2}D_2)\ V_\ell/(1 - D_2). \tag{13}$$

As a result, it can be written that $V_{H2} = V_{C2} + n_{s2}V_\ell$. Consequently, the second voltage conversion ratio of $G_2 = V_{H2}/V_\ell$ is obtained as follows:

$$G_2 = V_{H2}/V_\ell = (1 + n_{s2})/(1 - D_2). \tag{14}$$

The voltage stress on switches S_{b2}, S_{a2} and S_{c2} will be as follows:

$$V_{Sb2} = n_{s2}V_\ell + V_{C2} = V_{H2} \tag{15}$$

$$V_{Sa2} = V_\ell - v_{Lm2} = V_\ell/(1 - D_2) = V_{H2}/(1 + n_{s2}) \tag{16}$$

$$V_{Sc2} = V_{H2}. \tag{17}$$

The current balance law for the capacitor C_2 is written as follows:

$$\tilde{i}_{C2} = D_2(I_{H2}/D_2) + (1 - D_2)I_{Lm2}/(1 + n_{s2}) = 0. \tag{18}$$

Consequently, the average inductor current of i_{Lm2} can be obtained as follows:

$$I_{\ell 2} = I_{Lm2} = (1 + n_{s2})(-I_{H2})/(1 - D_2). \tag{19}$$

All the equations in (1)–(19) are the same for boost, buck, and buck-and-boost operations of the proposed converter.

C. Output Currents' Calculations

1) Boost Operation: The output currents I_{RH1} and I_{RH2} are equal to $I_{RH1} = -I_{H1} = V_{H1}/R_{H1}$ and $I_{RH2} = -I_{H2} = V_{H2}/R_{H2}$, respectively.

2) Buck Operation: The output currents are equal to $I_{R\ell} = -I_\ell = V_\ell/R_\ell$ and $I_{RH2} = -I_{H2} = V_{H2}/R_{H2}$, respectively.

3) Buck-and Boost-Operation: The output currents $I_{R\ell}$ and I_{RH1} are equal to $I_{R\ell} = -I_\ell = V_\ell/R_\ell$ and $I_{RH1} = -I_{H1} = V_{H1}/R_{H1}$, respectively.

D. Cancelling Input Current Ripple

In this part, the required conditions of achieving zero input current ripple at the low voltage side (i_ℓ) are obtained during a

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switching period. According to the Fig. 1, it can be written that

$$\begin{aligned} L_{p1} &= L_{m1} + L_{k1} \\ L_{t1} &= {n_{t1}}^2 L_{m1} \\ L_{s1} &= {n_{s1}}^2 L_{m1} \\ M_{pt1} &= M_{tp1} = n_{t1} L_{m1} \\ M_{ps1} &= M_{sp1} = n_{s1} L_{m1} \\ M_{ts1} &= M_{st1} = n_{t1} n_{s1} L_{m1}. \end{aligned} \tag{20}$$

The voltages across the windings of the first coupled inductor in Fig. 1(a) can be written as follows:

$$v_{Lp1} = L_{p1}(di_{Lp1}/dt) + M_{ps1}(di_{Ls1}/dt) + M_{pt1}(di_{Lt1}/dt) \tag{21}$$

$$v_{Ls1} = M_{ps1}(di_{Lp1}/dt) + L_{s1}(di_{Ls1}/dt) + M_{st1}(di_{Lt1}/dt) \tag{22}$$

$$v_{Lt1} = M_{pt1}(di_{Lp1}/dt) + M_{st1}(di_{Ls1}/dt) + L_{t1}(di_{Lt1}/dt). \tag{23}$$

1) Canceling Input Current Ripple at First Stage ($i_{\ell 1}$): Time Interval of $0 < t < D_1 T_s$*:* According to Fig. 1(a), it is obtained that

$$di_{Lp1}/dt = V_\ell (L_{t1} - M_{pt1})/(L_{t1} L_{p1} - {M_{pt1}}^2). \tag{24}$$

$$L_{t1} = M_{pt1} \quad \text{or} \quad {n_{t1}}^2 L_{m1} = n_{t1} L_{m1} \quad \text{or} \quad n_{t1} = 1 \tag{25}$$

$${M_{pt1}}^2 \neq L_{p1} L_{t1} \quad \text{or} \quad L_{k1} \neq 0. \tag{26}$$

Time Interval of $D_1 T_s < t < T_s$*:* In this state, based on Fig. 1(a), it can be obtained that

$$di_{Lp1}/dt = (V_\ell - V_{H1})\, D/(BD + AC). \tag{27}$$

$$(D = L_{t1} + M_{st1} - M_{ps1} - M_{pt1} = 0) \text{ or } (n_{t1} = 1) \tag{28}$$

$$(C = L_{p1} + M_{ps1} - M_{pt1} - M_{st1} \neq 0) \text{ or } (L_{k1} \neq 0). \tag{29}$$

Interval time of $0 < t < D_2 T_s$*:* Considering Fig. 1(a) the following equations can be obtained:

$$v_{Lt2} + v_{Ls2} = v_{Ls2} + v_{Lp2} = V_\ell + V_{H1} - V_{C2} \tag{30}$$

$$di_{Lp2}/dt = (V_\ell + V_{H2} - V_{C2}) D/(BD + AC). \tag{31}$$

Therefore, the required conditions for achieving zero input current ripple, is obtained as follows:

$$(D = 0) \text{ or } (n_{t2} = 1) \text{ and } (C \neq 0) \text{ or } (L_{k2} \neq 0). \tag{32}$$

2) Cancelling Input Current Ripple at Second Stage ($i_{\ell 2}$): Interval time of $D_2 T_s < t < T_s$*:* During this time interval, the following equations can be obtained:

$$v_{Lt2} + v_{Ls2} = v_{Ls2} + v_{Lp2} = V_{C2} - V_{C\ell 2} = V_\ell - V_{C2} \tag{33}$$

$$di_{Lp2}/dt = (V_\ell - V_{C2}) D/(BD + AC). \tag{34}$$

As a result, the required conditions for achieving zero input current ripple would be the same as (32).

TABLE I
MINIMUM ESTIMATED VALUES OF CAPACITORS

$C_{\ell 1\_\min}$	$D_1(-n_{s1})(-I_{H1}) / \left[0.01 V_{C\ell 1} - r_{C\ell 1} \dfrac{n_{s1}(-I_{H1})}{(1-D_1)}\right] f_s$
$C_{\ell 2\_\min}$	$n_{s2}(-I_{H2}) / \{[0.01 V_{C\ell 2} - r_{C\ell 2} n_{s2}(-I_{H2}) / [(1-D_2)D_2]] f_s\}$
$C_{2\_\min}$	$-I_{H2} / \{[0.01 V_{C2} - r_{C2}(-I_{H2}) / [D_2(1-D_2)]] f_s\}$
$C_{H1\text{–}\min}$	$C_{H1\_ESR} = D_1 I_{H1} / \{[0.01 V_{CH1} - r_C I_{H1} / (1-D_1)] f_s\}$ $C_{H1\_THT} = \dfrac{1}{0.01 R_{H1}(0.1 f_s)}$, $C_{H1\text{–}\min} = \max(C_{H1\_ESR}, C_{H1\_THT})$
$C_{H2\text{–}\min}$	$C_{H2\_ESR} = \dfrac{(1-D_2) I_{H2}}{[0.01 V_{CH2} - r_C(-I_{H2}) / D_2] f_s}$ $C_{H2\text{–}THT} = \dfrac{1}{0.01 R_{H2}(0.1 f_s)}$, $C_{H2\text{–}\min} = \max(C_{H2}\big\vert_{ESR}, C_{H2}\big\vert_{THT})$

E. Design Considerations

In continuous conduction mode (CCM) operation of the proposed converter, the following inequalities has to be verified:

$$L_{m1} > D_1(n_{s1} D_1 + 1) V_\ell / [2(1 + n_{s1}) I_{\ell 1} f_s] \tag{35}$$

$$L_{m2} > (V_\ell D_2 T_s)/[2(I_{\ell 2})] = (D_2/2 f_s)(V_\ell / I_{\ell 2}). \tag{36}$$

According to (20), it can be written that

$$\begin{aligned} L_{p1} &= L_{m1} + L_{k1} = L_{m1}/{K_1}^2 \\ L_{S1} &= {n_{s1}}^2 L_{m1}\ , L_{t1} = L_{m1} \\ M_{pt1} &= M_{tp1} = L_{m1}\ ,\ M_{ps1} = M_{sp1} \\ &= M_{st1} = M_{ts1} = n_{s1} L_{m1} \end{aligned} \tag{37}$$

$$\begin{aligned} L_{p2} &= L_{m2} + L_{k2} = L_{m2}/{K_2}^2 \\ L_{s2} &= {n_{s2}}^2 L_{m2}\ \ ,\ L_{t2} = L_{m2} \\ M_{pt2} &= M_{tp2} = L_{m2}\ ,\ M_{ps2} = M_{sp2} \\ &= M_{st2} = M_{ts2} = n_{s2} L_{m2} \end{aligned} \tag{38}$$

where K_1 and K_2 are coupling coefficients of the coupled inductors.

By considering the hold-up time required for step-load response, voltage ripple across each of the output capacitors (ΔV_{Co}) and voltage ripple caused by the equivalent series resistance of the output capacitors $\Delta V_{o1} = \Delta V_{Co1} + \Delta V_{Co-\mathrm{ESR}} = \Delta V_{Co1} + r_{Co1} \Delta I_{Co1}$. As a result, the minimum value of capacitors can be calculated as given in Table I.

F. Small Signal Analysis and Controlling System for Boost Operation of the Proposed Converter

According to Fig. 3, it is assumed that the inductor currents $i_{Lk1}, i_{Lm1}, i_{Lk2}$, and i_{Lm2}, capacitor voltages $v_{c\ell 1}$, $v_{c\ell 2}$, v_{CH1}, v_{c2}, and v_{CH2} are the state variables. The output voltages are v_{CH1} and v_{CH2} which should be regulated. Accordingly, the state matrixes as follows:

$$sX = AX + B_0 \tilde{v}_\ell + B_1 \tilde{d}_1 + B_2 \tilde{d}_2. \tag{39}$$

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As a result, the transfer functions of the output voltages v_{CH1} v_{CH2} are obtained as follows:

$$G_1(s) = \tilde{v}_{CH1}/\tilde{d}_1\Big|_{\tilde{v}_\ell=0} = G_{v_{CH1}-d1}(s)/G_p(s) = C_1B_1(sI-A)^{-1} \quad (42)$$

$$G_2(s) = \tilde{v}_{CH2}/\tilde{d}_2\Big|_{\tilde{v}_\ell=0} = G_{v_{CH2}-d2}(s)/G_p(s) = C_2B_2(sI-A)^{-1} \quad (43)$$

$$C_1 = \begin{bmatrix} 0\,0\,0\,1\,0\,0\,0\,0\,0 \end{bmatrix} \quad (44)$$

$$C_2 = \begin{bmatrix} 0\,0\,0\,0\,0\,0\,0\,0\,1 \end{bmatrix}. \quad (45)$$

Therefore, by adjusting the PI parameters K_{p1} and K_{i1} of the voltage loop controllers, the closed-loop system which is shown in Fig. 7, can achieve a better stability performance

$$G_{c1} = K_{p1} + K_{i1}/s = 0.00001 + 0.012/s \quad (46)$$

$$G_{c2} = K_{p2} + K_{i2}/s = 0.00001 + 0.016/s. \quad (47)$$

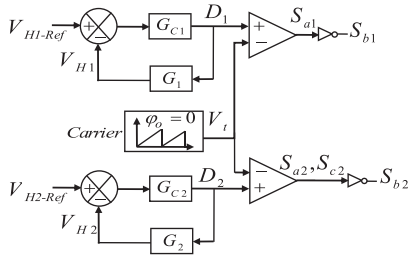

Fig. 7. Closed-loop controller of the output voltages for the proposed converter in boost operation.

V. Comparison Results

For comparing the proposed converter and the conventional dc–dc single-input, dual-output converters, the dc characteristics including voltage conversion ratio of first output port $(G_{\text{port}-1})$, second output port $(G_{\text{port}-2})$, total voltage gain (G_T), the total normalized maximum voltage stresses on the switches and diodes $[\Sigma(V_S+V_D)_{\max}/V_{o\_\max}]$, number of switches (N_S), diodes (N_D), inductors (N_I), capacitors (N_C), coupled-inductors (N_{CI}) the total components number (N_T),

$$X = \begin{bmatrix} \tilde{i}_{Lk1} \\ \tilde{i}_{Lm1} \\ \tilde{v}_{C\ell 1} \\ \tilde{v}_{CH1} \\ \tilde{i}_{Lk2} \\ \tilde{i}_{Lm2} \\ \tilde{v}_{C\ell 2} \\ \tilde{v}_{C2} \\ \tilde{v}_{CH2} \end{bmatrix}, B_0 = \begin{bmatrix} 1/L_{k1} \\ 0 \\ 0 \\ 0 \\ 1/L_{k2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, B_1 = \begin{bmatrix} 0 \\ (n_{s1}V_\ell + V_{H1})/(1+n_{s1})/L_{m1} \\ -I_{Lm1}[n_{s1}/(1+n_{s1})]/C_{\ell 1} \\ -I_{Lm1}/(1+n_{s1})/C_{H1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (40)$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ (n_{s2}V_\ell + V_{C2})/(1+n_{s2})/L_{m2} \\ \frac{-I_{Lm2}n_{s2}}{(1+n_{s2})C_{\ell 2}} + \frac{n_{s2}(V_{CH2}-V_{C2}-n_{s2}V_\ell)}{r_C C_{\ell 2}} \\ \frac{\frac{I_{Lm2}}{(1+n_{s2})} + (V_{CH2}-V_{C2}-n_{s2}V_\ell)/r_C}{C_2} \\ (-V_{CH2}+V_{C2}+n_{s2}V_\ell)/r_C\,/C_{H2} \end{bmatrix}$$

$$A = \begin{bmatrix} 0 & 0 & -1/L_{k1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1+n_{s1}D_1}{(1+n_{s1})L_{m1}} & \frac{-(1-D_1)}{(1+n_{s1})L_{m1}} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_{\ell 1}} & \frac{-(1+n_{s1}D_1)}{(1+n_{s1})C_{\ell 1}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1-D_1}{(1+n_{s1})C_{H1}} & 0 & \frac{-1}{R_{H1}C_{H1}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1/L_{k2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1+n_{s2}D_2}{(1+n_{s2})L_{m2}} & \frac{-(1-D_2)}{(1+n_{s2})L_{m2}} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{\ell 2}} & \frac{-(1+n_{s2}D_2)}{(1+n_{s2})C_{\ell 2}} & \frac{-{n_{s2}}^2 D_2}{r_C C_{\ell 2}} & \frac{-n_{s2}D_2}{r_C C_{\ell 2}} & \frac{n_{s2}D_2}{r_C C_{\ell 2}} \\ 0 & 0 & 0 & 0 & 0 & \frac{1-D_2}{(1+n_{s2})C_2} & \frac{-n_{s2}D_2}{r_C C_2} & \frac{-D_2}{r_C C_2} & \frac{D_2}{r_C C_2} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{n_{s2}D_2}{r_C C_{H2}} & \frac{D_2}{r_C C_{H2}} & -\left(\frac{D_2}{r_C}+\frac{1}{R_{H2}}\right)\frac{1}{C_{H2}} \end{bmatrix} \quad (41)$$

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TABLE II
COMPARISON OF HIGH VOLTAGE GAIN SINGLE-INPUT/DUAL-OUTPUT CONVERTERS

DC-DC Converters	$G_{port\_1}=V_{o1}/V_i$	$G_{port\_2}=V_{o2}/V_i$	G_T	$\Sigma(V_S+V_D)_{\max}/V_{o\_\max}$	N_S	N_D	N_I	N_C	N_{CI}	N_T	Δi_i	⏚	Size
[2]	$1/(1-D)$	$1/D$	$[1/(1-D)]+1/D$	3	3	-	2	4	2	11	Low	Yes	Medium
[3-A]	$1/(1-D)$	$-1/(1-D)$	$2/(1-D)$	4	1	3	1	3	-	8	Low	Yes	Small
[3-B]	$1/(1-D)$	$2/(1-D)$	$3/(1-D)$	5/2	1	3	1	3	-	8	Low		Small
[3-C]	$1/(1-D)$	$(2-D)/(1-D)$	$(3-D)/(1-D)$	$4/(1-D)$	1	3	1	3	-	8	High		Small
[6]	$2N/(1-D)$	$D/(1-D)$	$(2n+D)/(1-D)$	$2+(2/n)$	4	3	-	3	2	12	High	No	Big
[16]	$D/(1-D)$	$D/(1-D)$	$2D/(1-D)$	$3/D$	2	1	3	3	-	9	Low	Yes	Medium
[17]	$1/(2D)$	$1/(2D)$	$1/D$	6	2	2	1	2	-	7	Low	No	Medium
[18]	$1/D$	$1/D$	$2/D$, $0<D<0.5$	3	3	3	1	3	-	10	High	Yes	Big
[19]	$1/(2-2D)$ $0.5<D<1$	$(1-D)/(2-2D)$ $0.5<D<1$	$(2-D)/(2-2D)$ $0.5<D<1$	3	4	2	2	3	-	11	Equal to zero	No	Medium
[23]	$1/(1-D)$	$1/(1-D)$	$2/(1-D)$	4	2	2	-	2	1	7	low	No	Medium
Proposed converter	$(n_{s1}D+1)/(1-D)$	$(n_{s2}+1)/(1-D)$	$(n_s+n_sD+2)/(1-D)$	$2/(n_s+1)+3$	5	-	-	6	2	13	Equal to zero	Depending on the application	Medium

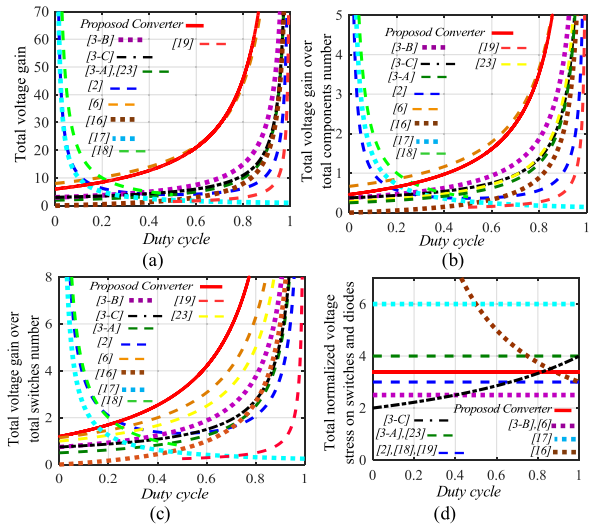

Fig. 8. Comparison results versus duty cycle *(D)*. (a) Total voltage gain. (b) Total voltage gain over the total component number. (c) Total voltage gain over the number of switches. (d) Total normalized voltage stress on switches and diodes.

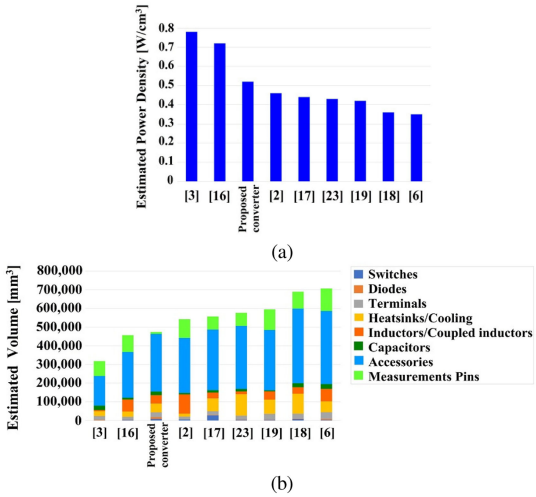

Fig. 9. Comparison results. (a) Estimated power density per $[W/\mathrm{cm}^3]$. (b) Estimated volume per $[\mathrm{mm}^2]$.

input current ripple (Δi_i), the common ground of the ports and size of compared converters are given in Table II.

Please, note that depending on the application of the proposed converter whether the port 3 is going to supply an inverter, there would be no polarity consideration but in the case of dc loads, the polarity of the third port is reverse from other two ports. Considering Table II and turn ratio of coupled inductors $n=4$, Fig. 8(a)–(d) is plotted. Fig. 8(b) shows the ratio of total voltage gain over the total components number (G_T/N_T) versus duty cycle. G_T in the SIDO converters is defined as $G_T=V_{o1}/V_i+V_{o2}/V_i$. Fig. 8(c) shows that the ratio of G_T/N_S in the proposed converter is higher than the compared converters. Fig. 8(d) shows the ratio of $\Sigma(V_{S\_\max}+V_{D\_\max})/V_{o\_\max}$.

From Fig. 9(a), the proposed converter is third from the aspect of power density and the power extracted from every cm^3 unit of the converter. Note that to achieve the results of Fig. 9, the converters are considered to be operated in the power of 250 W. Also, Fig. 9(b) shows the volume of the compared converters. Moreover, considering Table II the input current ripple is equal to zero in the proposed converter, which is not the same for other compared converters.

VI. EXPERIMENTAL RESULTS

In this part, the theoretical analysis is reconfirmed by using experimental results for two operations of the proposed converter. The values of used parameters in the experimental prototype are given in Table III.

A. Boost Operation of the Proposed Converter

In the practical prototype of proposed converter for this operation, two output loads of $R_{H1}=370\ \Omega$ and $R_{H2}=380\ \Omega$, a low input voltage of $V_\ell=24$ V as source are used.

The total output power of the boost operation is equal to $P_{oT}=P_{H1}+P_{H2}=401$ W. Measured results shown in Figs. 10 and 11 for this operation of the converter. Both two

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TABLE III
EXPERIMENTAL PARAMETERS

Voltages	$V_\ell / V_{H1} / V_{H2} = 24\,V / 304\,V / 240\,V$
Output Powers	For boost operation: $P_{H1} / P_{H2} = 250W / 151\,W$ For buck operation: $P_\ell / P_{H2} = 250W / 150W$
Duty cycles/Frequency	$D_1 = 0.7$, $D_2 = 0.6$, $f_s = 50\,kHz$
Capacitors	$C_{\ell 1} = 220\mu F$, $C_{\ell 2} = C_2 = 100\mu F$
Output capacitors	For boost operation: $C_{H1} = C_{H2} = 100\mu F$ For buck operation: $C_\ell = C_{H2} = 100\mu F$ For buck and boost operation: $C_\ell = C_{H1} = 100\mu F$
Inductors	$L_{m1} = L_{m2} = 150\,\mu H$, $L_{k1} = L_{k2} = 10\mu H$ $n_{S1} = 4$, $n_{S2} = 3$, Type: Toroid TDK PC40-T72
Switches/Diodes	$S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{c2}$: IPW60R017C7 Reverse parallel diodes: DSEI 120
Loads	$R_{H1} = 370\,\Omega$, $R_{H2} = 380\,\Omega$ for boost operation $R_\ell = 2.3\,\Omega$, $R_{H2} = 380\,\Omega$ for buck operation

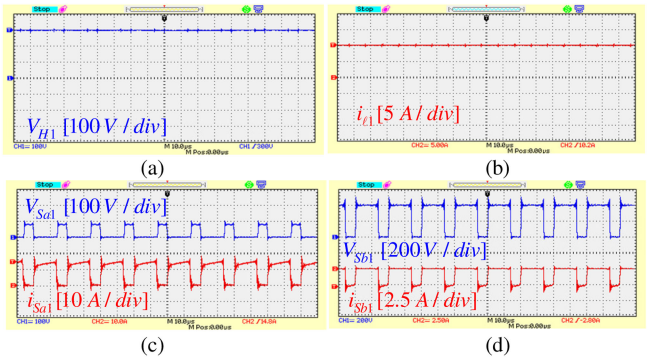

Fig. 10. Voltages and currents of first stage for boost operation.

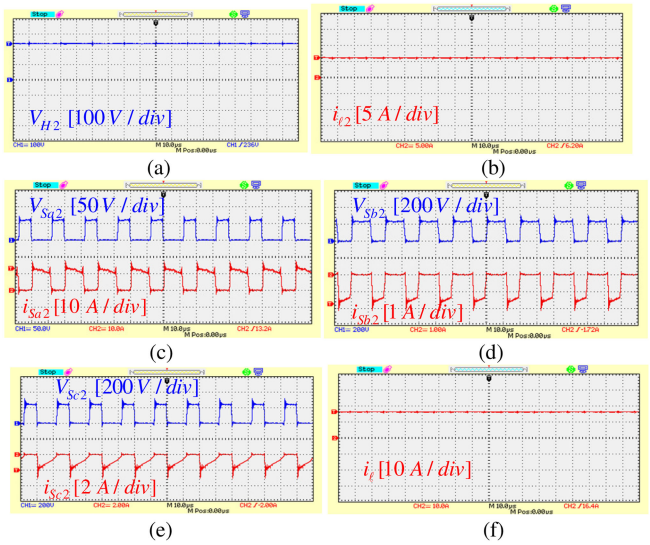

Fig. 11. Voltages and currents of second stage for boost operation.

output voltages can be controlled simultaneously to an acceptable extent, as shown in Fig. 12.

B. Buck Operation of the Proposed Converter

In the practical prototype of proposed converter for this operation, two output loads of $R_{H2} = 380\ \Omega$ and $R_\ell = 2.3\ \Omega$ are

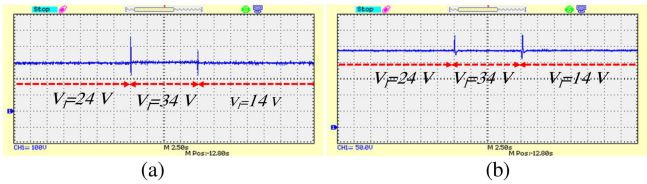

Fig. 12. Output voltages regulation and dynamic response under the input voltage variation for boost operation. (a) V_{H1}. (b) V_{H2}.

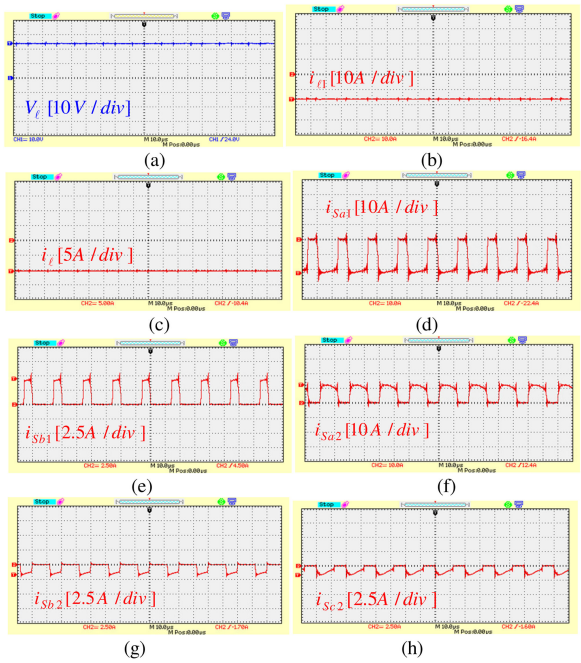

Fig. 13. Experimental results for buck operation.

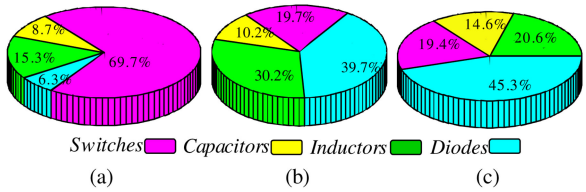

Fig. 14. Power loss distribution for $P_{oT} = 400$ W. (a) Boost operation. (b) Buck operation. (c) Buck-and-boost operation.

supplied by using the high input voltage source of $V_{H1} = 304$ V. In this operation, the voltage stress on switches, V_{H2}, V_{C2}, are same as in boost operation. The output power is equal to $P_{oT} = P_\ell + P_{H2} = 401$ W.

C. Efficiency of the Proposed Converter

In boost operation, the power loss calculation is done for the output power equal to $P_{oT} = 400$ W. where, $P_{H1} = 250$ W and $P_{H2} = 150$ W. Therefore, the total power loss is obtained as $P_{\text{Loss}} = 24.8444$ W. In the buck operation, the power loss calculation is done for the output power equal to $P_{oT} = 400$ W where $P_\ell = 250$ W and $P_{H2} = 150$ W. In buck-and-boost operation, the power loss calculation is done for the output power equal to $P_{oT} = 400$ W. where, $P_\ell = 250$ W and $P_{H2} = 150$ W. As

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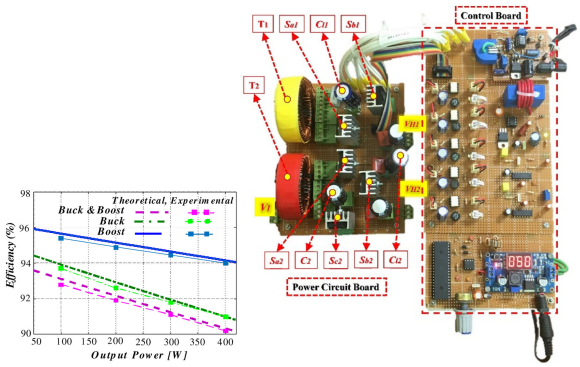

Fig. 15. Experimental and theoretical efficiency and implemented prototype of the proposed converter: (a) efficiency; (b) implemented prototype.

a result, the power loss distribution among the different components for three operations is shown in Fig. 14. The efficiency curves of proposed converter versus output power are plotted as illustrated in Fig. 15(a) for three operations.

VII. Conclusion

In this article, a three-port dc–dc converter with three functions and high voltage conversion ratios was proposed. The proposed converter can be applied for supplying loads such as batteries, automobile headlamps, uninterruptible power supplies (UPS), dc motor drives, green houses, etc. Also, it can be an interface of inverters to supply ac loads. The proposed converter has the merit of achieving the zero-input current ripple at the low voltage side for the whole range of operating duty cycles. The ratio of total voltage gain over the total component number in the proposed converter is higher than the other recently presented converters. In this article, the converter is analyzed theoretically for a switching period and the analysis are confirmed by the experimental results for a prototype with specifications of 24 V/304 V, 240 V and 400 W.

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