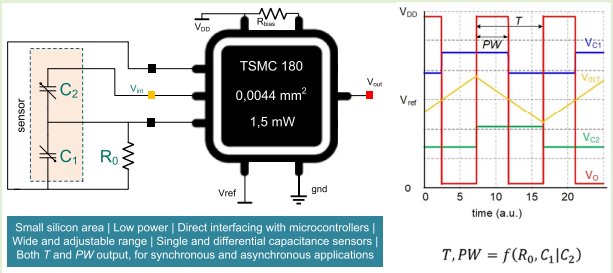
A 180-nm CMOS Integrated Capacitance-to-Time Converter for Capacitive Sensing Applications

Hala Darwish, Càndid Reig, *Senior Member, IEEE*, Gildas Leger, Guido Di Patrizio Stanchieri, *Member, IEEE*, Orazio Aiello, *Senior Member, IEEE*, and Andrea De Marcellis, *Member, IEEE*

***Abstract*—This article presents the implementation of a capacitance-to-time converter in standard 0.18-μm CMOS technology. It is based on a square-wave relaxation oscillator that incorporates both pulsewidth modulation (PWM) and proportional to magnitude (PM) dependencies. The circuit is designed to interface with differential capacitance sensors but can also interface with single-capacitance sensors using a reference capacitor. It works with various capacitive values, ranging from a few nanofarads to less than one picofarad, considering different external R_0 resistor values. Characterization tests proved that the fabricated chips exhibit the expected performance across the full range of use, achieving a sensitivity of 207 μs/ΔpF in the differential mode (110 μs/pF in the single mode) and a resolution of 0.5 fF in the differential mode ((0.9 fF in the single mode). The circuit occupies a silicon area of 0.0044 mm^2, with a maximum power consumption of 1.5 mW. The circuit has also been successfully tested in real applications, such as measuring liquid levels in microfluidic applications. By using COTS level-meters, it achieved a sensitivity of 0.4 pF/mL with a resolution of 100 μL. Measuring the dielectric constant in liquids was also demonstrated by using specifically designed 3-D-printed fluidic capacitance sensors.**



***Index Terms*— Capacitance-to-time converter, CMOS integrated circuit, differential capacitance sensors.**

I. Introduction

CAPACITIVE sensors have traditionally been very popular due to their inherent characteristics in terms of manufacturing routes, their application in many scenarios, and their ease of electronic interfacing. The basic behavior of a capacitive sensor can be described by the well-known formula $C = A\epsilon/d$, where A is the area of the capacitor, ϵ is the permittivity of the material, and d is the distance between the metal electrodes. A change in capacitance can be due to a relative displacement between the electrodes or to a change in the permittivity of the separating material. In the first group, we find position and pressure sensors or accelerometers. Gas sensors or liquid-level gauges should be good examples of the second. Both types of sensors share the additional property that they can be implemented in a differential topology, with the inherent advantages that this brings.

Today, new applications arising from the development of cutting-edge technologies, such as the Internet of Things (IoT) [1], biotechnology [2], [3], or artificial intelligence (AI) [4], have reactivated the need for devices based on these types of sensors, but with more demanding features. The current common requirements for these devices are small size, low power consumption, low price, easy integration, and, if possible, direct interfacing with small microcontrollers [1], [2], [3], [4]. In this respect, advanced manufacturing technologies compatible with CMOS integration have allowed

Received 2 May 2025; revised 8 July 2025 and 23 July 2025; accepted 26 July 2025. Date of publication 14 August 2025; date of current version 2 October 2025. This work was supported in part by the Ministerio de Ciencia e Innovación (co-funded by the FEDER Program), Spanish Government, under Project PID2023-149071NB-C53; and in part by European Union—NextGenerationEU, Mission 4, Component 2, under Italian Ministry of University and Research (MUR) National Innovation Ecosystem—VITALITY—CUP E13C22001060006 under Grant ECS00000041. The associate editor coordinating the review of this article and approving it for publication was Prof. Benoit Gosselin. *(Corresponding author: Càndid Reig.)*

Hala Darwish and Càndid Reig are with the Department of Electronic Engineering, University of Valencia, 46100 Burjassot, Spain (e-mail: candid.reig@uv.es).

Gildas Leger is with the Institute of Microelectronics of Seville (IMSE-CNM, CSIC), 41092 Seville, Spain.

Guido Di Patrizio Stanchieri and Andrea De Marcellis are with the Department of Information Engineering, Computer Science and Mathematics (DISIM), University of L'Aquila, 67100 L'Aquila, Italy.

Orazio Aiello is with the Dipartimento di ingegneria navale, elettrica, elettronica e delle telecomunicazioni (DITEN), Universitã di Genova, 16145 Genoa, Italy.

Digital Object Identifier 10.1109/JSEN.2025.3597027

© 2025 The Authors. This work is licensed under a Creative Commons Attribution 4.0 License.
For more information, see https://creativecommons.org/licenses/by/4.0/

TABLE I
CURRENT APPLICATIONS OF MINIATURIZED CAPACITIVE SENSORS

Ref.	Magnitude	Fabrication process	C nom.	Sensit.	Diff.
[5]	Humidity	Flexible thin films	∼250 pF	–	No
[6]	Displace.	machining	∼200 pF	–	Yes
[7]	Pressure	Stretchable PDMS	∼35 pF	–	No
[8]	Force	Flexible polymer	∼25 pF	–	Yes
[9]	Humidity	Inkjet printing	∼2 pF	–	No
[10]	Acceler.	3D printed	0–1 pF	–	Yes
[11]	Pressure	SiC	0–1 pF	1 fF/kPa	Yes
[12]	Pressure	MEMS	∼150 fF	–	Yes
[13]	Acceler.	Monolithic BiCMOS	∼120 fF	–	No
[14]	Pressure	CMOS MEMS	∼25 fF	150 aF/kPa	No
[15]	Acceler.	MEMS	0–15 fF	15.5 fF/g	Yes

this qualitative and quantitative step. For these miniaturized applications, A must necessarily be small, so that the nominal capacitance becomes also small and, in most cases, so is the sensitivity. We show significant examples from the recent literature in Table I. From this table, it can be seen that well-performing sensors implemented with different microfabrication techniques (flexible polymers, machining, ink-jet, and 3-D printing) are obtained in the 1-pF–1-nF range. When microelectronic processes are used, their nominal capacitance remains below the picofarad limit. In addition, if the nature of the sensor allows it, differential topologies are used because of their inherent advantages in terms of higher sensitivity, linearity, and immunity to external phenomena.

Designing integrated electronic interfaces for these novel capacitive sensors is not a simple task. Capacitance sensor interfaces can be classified into different families: switched-capacitor (SC) [16], iterative-delay-chain (IDC) [17], capacitance-to-voltage (CV) [18], or capacitance-to-time (CT) converters [19]. For low-voltage/low-power applications, CT converters are often preferred due to their simplicity, robustness, sensitivity, and noise issues. CT converters are typically based on square-wave relaxation oscillators, where the period T or pulse PW is a function of the measured capacitance. CT-based architectures can also be directly connected to microcontrollers [20], [21], [22], [23], allowing the addition of valuable functionalities such as auto-balancing or auto-calibration [24], [25], [26], [27]. Table II provides an up-to-date list of on-chip comparable proposals. Discrete element solutions can also be found, for example, in [28], [29], [30], and [31], but they are not included in this comparative table. As observed from the table, all the proposed solutions show good figures within their specific range of application. In general, CT converters display lower power consumption and require less silicon area than SC ones.

In this article, we present the CMOS implementation of a capacitance-to-time converter, based on a square-wave relaxation oscillator, providing both a pulsewidth (PW) and a proportional-to-magnitude (PM) dependency of the quasidigital output signal. The circuit is designed for interfacing differential capacitance sensors, but single-capacitance sensors can also be connected by using a reference capacitor. Circuit topology, including a breadboard implementation, was introduced in [30]. Then, its CMOS integration was proposed in [43], where simulation results were presented.

The proposed solution has clear advantages. The simplicity of the design allows for a streamlined CMOS implementation that is particularly well-suited for limited silicon areas, overperforming other approaches (see Table II). The system provides a quasidigital output signal, independent of supply drift, allowing seamless integration with conventional microcontrollers. It offers high detection sensitivity and resolution, with very low sensitivity to common-mode noise and interference. By incorporating an external resistor, it accommodates a wide range of capacitance values, spanning more than three orders of magnitude, from a few nanofarads to less than one picofarad, covering most of the detection ranges displayed in Table II with a unique design. In addition, both single and differential capacitive sensor topologies can be connected. This versatile circuit accommodates both PM and PW modulation (PWM) dependencies, allowing it to be used with both synchronous and asynchronous measurement schemes.

This article is structured as follows. After the introduction, Section II describes the topology and functional principles of the proposed capacitance-to-time converter, along with its CMOS implementation details. Section III presents the experimental characterization of the circuit, highlighting its performance across different capacitance ranges and configurations. Section IV explores two practical applications that validate the circuit's versatility, including liquid-level sensing and dielectric constant measurement. Finally, Section V concludes this article by summarizing the key findings and the potential of the proposed design for future capacitive sensing systems.

II. CIRCUIT DESCRIPTION

In the next paragraphs, the working principle of the circuit will be briefly described, and its implementation in standard CMOS technology will be explained.

A. Topology and Function Explanation

The electrical scheme of the circuit interface considered, adapted from that proposed in [30], is shown in Fig. 1(a). In Fig. 1(b), the time-dependent voltage signals at the main nodes are depicted. The circuit consists of a voltage integrator connected to a differential capacitive sensor, along with two hysteresis voltage comparators and a mixer. The comparators, in combination with seven resistors, enable adjustment of the circuit's dynamic range, detection sensitivity, and resolution. The mixer consolidates all signal information to generate a pulsed output signal, the period and duty cycle (DC) of which depend on the sensor' two capacitances, C_1 and C_2. Specifically, the mixer helps reduce the measurement time by producing an output signal [V_o; see Fig. 1(b)] with a period equal to half that of the internal square-wave signal (V_{c2})

TABLE II
CHARACTERISTIC PARAMETERS OF THE PROPOSED CIRCUIT AS COMPARED TO OTHER SIMILAR SOLUTIONS

Ref.	Sensor topology	Circuit typology	CMOS technology	Output format	Detection range	Sensitivity	Resolution	Area	Power
[32]	Single	Mixed signal	0.35 μm / 3.3 V BiCMOS STM	PWM	0.8-1.2 pF	47 μs/pF	0.9 fF	0.20 mm^2	15.84 mW
[33]	Single	Mixed signal	0.35 μm / 3.3 V CMOS	PM	1.8-6.8 pF	1.12 ms/pF	0.2 fF	0.51 mm^2	0.211 mW
[34]	Single	Mixed signal	0.16 μm / 1.0 V CMOS	PM	0-8 pF	–	1.4 fF	0.05 mm^2	0.014 mW
[35]	Single	Analog	0.32 μm / 3.3 V CMOS STM	PWM	16-256 fF	32 μs/pF	0.8 fF	0.53 mm^2	0.084 mW
[36]	Single	Analog	0.13 μm / 1.0 V CMOS TSMC	PWM	0-9 pF	1.82 μs/pF	13 aF	0.011 mm^2	0.060 mW
[37]	Single	Analog	0.35 μm CMOS	PWM	2.5-2.8 pF	3.9 μs/pF	2.8 fF	0.09 mm^2	0.705 mW
[38]	Single	Analog	On-chip integration	PWM	1-22 pF	3.6 μs/pF	11 aF		
[39]	Differ.	Mixed signal	On-chip integration	PWM	40-60 fF (single) -20/+20 fF (differ.)	127 μs/pF (differ.)	0.16 fF (differ.)		
[40]	Single	Mixed signal	CMOS 180	PW / Digital	360 pF	–	7.2 fF	0.01 mm^2	1.5 µW
[41]	Differ.	SC	UMC 180	Analog / Diff.	25 fF – 8 pF	4 mV/fF	70 aF	0.8 mm^2	5.2 mW
[16]	Differ.	SC	CMOS 0.35 µm	Analog	0.2 – 100 pF	20 mV/pF	0.2 pF	7.8 mm^2	3.3 mW
[42]	Single	IDC	UMC 180	Digital	0.25 – 250 pF	–	–	0.0192 mm^2	–
[17]	Single	IDC	UMC 180	Digital	60 fF – 880 pF	–	36.4 fF	0.18 mm^2	2.1 µW
This work	Single / Diff.	Quasi digital	0.18 µm / 1.8 V CMOS TSMC	PM / PWM	1 pF-1 nF	110 µs/pF (single) 207 µs/ΔpF (differ.)	0.9 fF (single) 0.45 fF (differ.)	0.0044 mm^2	1.5 mW

generated by the closed-loop oscillator formed by the integrator and the two comparators—effectively doubling the frequency.

The XNOR logic gate is an important component of the proposed circuit. The square waves V_{c1} and V_{c2} are generated starting from the same triangular wave V_{int} and show the same frequency. The XNOR purpose is to convert the phase delay (i.e., the overlapping time) between V_{c1} and V_{c2} into a PW variation of the output V_o. In addition, V_{c1} and V_{c2}, since they are the outputs of the two OP-AMP-based comparators, suffer from the load effect due to the different resistors (R_1–R_6) connected at their output nodes. This reduces the full dynamic variation range of the output voltages V_{c1} and V_{c2} (i.e., rail-to-rail operation not provided) and, in addition, the waveforms also present a slight distortion. Therefore, with the use of the XNOR, it is also possible to generate an enhanced square-wave V_o with an improved output voltage variation (i.e., a quasidigital V_o signal, swinging from *gnd* to V_{DD} so guaranteeing a rail-to-rail dynamic response). Moreover, the XNOR also allows for improving the measurement speed, since the period of V_o is equal to a semi-period (i.e., a double frequency) of V_{c1} and V_{c2} [see Fig. 1(b)]. In other words, by measuring only one period of V_o (i.e., one semi-period of V_{c1} and V_{c2}), it is possible to estimate T and PW in a reduced time. These two parameters, T and PW, are measured to estimate and calculate the values of C_1 and C_2. Additionally, the operating range of the interface (i.e., the sensor's variation range) can be easily configured via the resistors used, which also allow fine-tuning of the overall circuit's detection sensitivity.

From a conventional circuit node analysis and considering ideal components, the period T and the pulsewidth PW of the output voltage are given by (6) and (7). This system of equations can be inverted to obtain C_1 and C_2 as functions of the time parameters [30]. In any case, as observed, R_0 has the greatest impact on the relationship between T, PW, C_1, and C_2. More specifically, referring to Fig. 1(a), it is possible to highlight that the resistor couples $R_1|R_2$, $R_3|R_4$, and $R_5|R_6$ work simply as resistive voltage dividers generating V_b, V_a, and V_{i1}, respectively. Moreover, the comparator generates two square-wave signals that depend on the output of the integrator. More in detail, the integrator and "Comparator 2" generate a positive closed loop that triggers the circuit oscillation when the voltage at node V_b reaches the threshold voltage V_a. In this sense, V_a and V_b input voltages of the "Comparator 2" are expressed in (1) and (2), while (3) reports the expression of the other threshold voltage V_{i1}, that is also

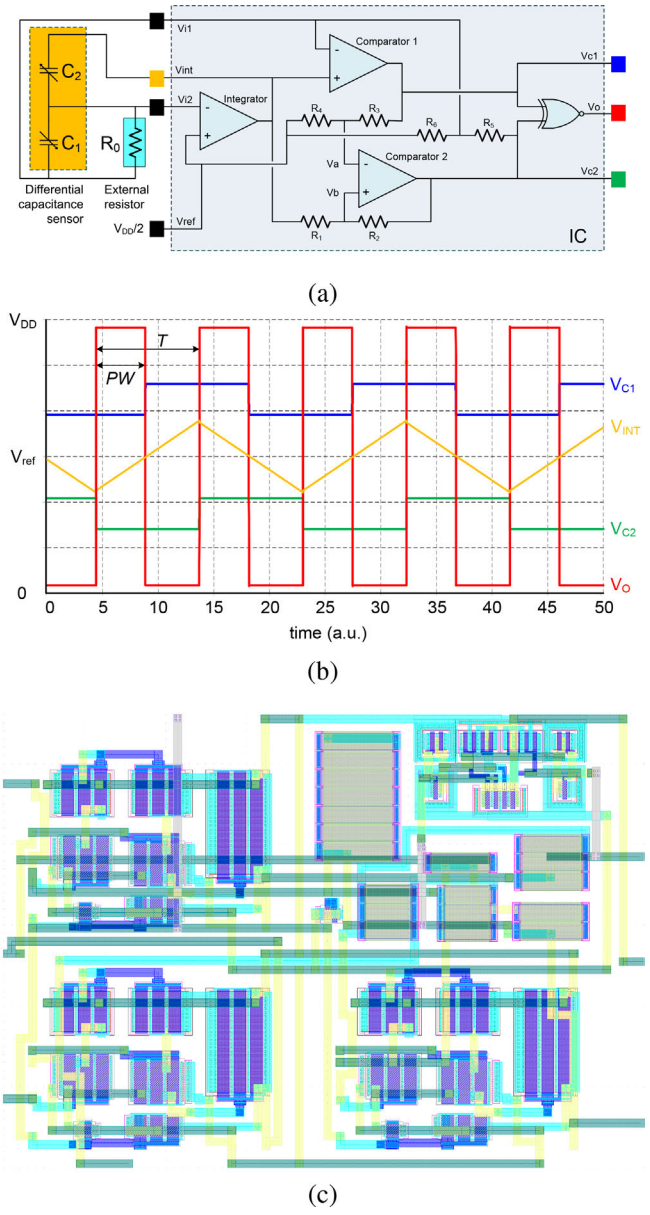


Fig. 1. (a) Block scheme of the proposed capacitance-to-time converter system. (b) Time-domain voltage signals of the main nodes. (c) CMOS layout of the system (80 × 50 μm).

the excitation voltage of the differential capacitance sensor (C_1 and C_2) combined with the external resistor (R_0) and (4) shows the expression of V_{int} signal

$$V_a(t) = (V_{c2}(t) - V_{\text{int}}(t))\left(\frac{R_1}{R_1+R_2}\right) + V_{\text{int}}(t) \quad (1)$$

$$V_b(t) = (V_{c1}(t) - V_{\text{ref}})\left(\frac{R_4}{R_3+R_4}\right) + V_{\text{ref}} \quad (2)$$

$$V_{i1}(t) = (V_{c2}(t) - V_{\text{ref}})\left(\frac{R_6}{R_5+R_6}\right) + V_{\text{ref}} \quad (3)$$

$$V_{\text{int}}(t) = V_{\text{ref}}\left(\frac{1-\frac{R_4}{R_3+R_4}-2\frac{R_1}{R_1+R_2}}{1-\frac{R_1}{R_1+R_2}}\right) - \left(V_{i1}(t)\frac{C_1}{C_2} + \int_0^t \frac{V_{i1}(t)}{R_0\,C_2}dt\right). \quad (4)$$

By considering that V_{ref} is equal to $V_{\text{DD}}/2$, and V_{c1}, V_{c2}, and V_{i1} are square waveforms that assume constant values during each semi-period of their oscillations (V_{c1} and V_{c2} assume the saturation voltages gnd $-$ V_{DD}, V_{i1} is proportional to V_{DD} by R_5 and R_6 relationship) and that a semi-period of V_{c1} and V_{c2} is equal to T of V_o, then (4) becomes

$$V_{\text{int}}(T) = V_{\text{ref}}\left(\frac{1-\frac{R_4}{R_3+R_4}-2\frac{R_1}{R_1+R_2}}{1-\frac{R_1}{R_1+R_2}}\right) - V_{i1}(T)\left(\frac{C_1}{C_2}+\frac{T}{R_0\,C_2}\right). \quad (5)$$

Consequently, by combining the overall equation system composed of (1), (2), (3), and (5), it is possible to extract the expressions of the period T and the related pulsewidth PW of the output voltage V_0 that are given by (6) and (7), as shown at the bottom of the next page. Moreover, these last equations can be inverted by extracting the expressions to calculate the value of C_1 and C_2 (i.e., to estimate the sensor capacitance values, and so to evaluate the physical/chemical parameter changes), by employing the measurements of T and PW values.

The resistors R_1–R_6 enable the main circuit to achieve a suitable tradeoff among capacitance dynamic range, sensitivity, and linearity response. In particular, the resistors R_1–R_6 allow for regulating the oscillation frequency and the relative phase shift of V_{C1} and V_{C2} as well as the corresponding relationship between T and PW of V_0. In this regard, considering (6) and (7), it is possible to analyze the T and PW sensitivities for all the passive components, in particular to the resistors R_1–R_6. In more detail, the resistor values are chosen to regulate the voltage thresholds of the two comparators. In particular, this applies to R_5 and R_6, which also regulate the excitation voltage of the differential capacitance sensor (C_1 and C_2) combined with the external resistor (R_0). In this regard, R_5 and R_6 also affect the instantaneous variation of V_{INT} when a commutation of the oscillator occurs and, so, V_{C1} and V_{C2} switch from 0 V to V_{DD} (and vice versa). The amplitude of this variation edge affecting V_{int}, after the commutation of V_{C2}, is equal to $C_1/C_2 \cdot [V_{\text{DD}} \cdot R_6/(R_5+R_6)]$. Consequently, to reduce or neglect this sudden variation affecting V_{int}, the factor $R_6/(R_5+R_6)$ should be small by properly selecting the values of R_5 and R_6. Moreover, as a further consideration, all the values have also been optimized to make the load effects negligible at the output of the operational amplifiers (depending on their output driving current capabilities). Finally, according to (6) and (7), it is possible to evaluate that there is a linear dependence of T and PW from R_0. Another setting can be achieved by adjusting the external resistor R_0. This setting allows the input dynamic range of capacitance values to be selected from a few nanofarads to below the picofarad scale, while maintaining output time ranges from a few milliseconds to a few microseconds. In other words, by externally operating on R_0, it is possible to regulate directly the sensitivity of the circuit.

B. CMOS Implementation

The standard TSMC 180-nm technology was considered for the CMOS implementation. The same eight-transistor simple topology was used for the three op-amps (the integrator and both comparators). The mixer consisted of a standard two-input XNOR gate. Fig. 1(c) shows the designed circuit layout obtained using standard cells provided by TSMC 180-nm CMOS technology. The required on-chip Si area is only about 80 × 55 µm (4400 µm^2). Cadence postlayout simulations were performed to ensure the appropriate function of the circuit [43]. From this study, the proposed resistor values are: $R_1 = 3.9\,\text{k}\Omega$, $R_2 = 8.2\,\text{k}\Omega$, $R_3 = 12.0\,\text{k}\Omega$, $R_4 = 1.0\,\text{k}\Omega$, $R_5 = 16.4\,\text{k}\Omega$, and $R_6 = 1.0\,\text{k}\Omega$. With the proper selection of the value of the external R_0 resistor, the circuit can be tuned to interface capacitance values from a few nanofarads to below the picofarad scale. The obtained output times range from a few milliseconds to a few microseconds. For the subsequent analyses, it is worth substituting the corresponding resistor values into (6) and (7)

$$T = 2R_0\,(10.213 \cdot C_2 - C_1) \tag{10}$$

$$PW = 2R_0\,(4.607 \cdot C_2 - C_1)\,. \tag{11}$$

Because variations in the values of these resistors inevitably introduce deviations in the output signal, a sensitivity analysis was performed (see results in Table III). Considering a typical tolerance of ±5% for all resistors, the output range (3σ) will be about ±11% of the nominal value, according to a statistical analysis. However, this is not a major issue because direct interfacing with a microcontroller is straightforward. Therefore, a subsequent calibration procedure should easily address the issue.

The design was included in a multiproject run for fabrication [see Fig. 2(a)]. The circuit has $V_{DD} = 1.8\,\text{V}$, as per technology requirements, and the bias resistor can be ranged from 10 to 47 kΩ while keeping its functionality. Recommended values are from 22 to 39 kΩ. In this interval, the static (OP) power consumption ranges from 1.5 to 1.0 mW. The static (OP) Ibias ranges from 67 to 21 µA, which is divided between three comparators. The test bench included a 10 pF/10 MΩ parallel for the output pin and a 0 pF/1 GΩ parallel for the V_{C1} and V_{C2} pins. For this power consumption characterization, $R_0 = 1\,\text{M}\Omega$ and $C_1 = C_2 = 1\,\text{pF}$ were considered.

TABLE III
SENSITIVITY AND LINEARITY OF T AND PW AS A FUNCTION OF THE CONSIDERED RESISTORS

Resistor	Pulse width (PW)	Period (T)	linearity (r)
R_1	21.54	44.62	1.0000
R_2	-9.79	-20.96	-0.9996
R_3	-1.62	-3.25	-0.9997
R_4	21.30	42.00	1.0000
R_5	5.88	12.01	-0.9996
R_6	-96.30	-197.00	1.0000
R_0	0.75	1.88	1.0000

III. CIRCUIT CHARACTERIZATION

As indicated in Section I, this circuit is proposed for interfacing capacitance sensors, with differential or single topology, in the range of 1 pF–1 nF, by considering different R_0 values. Fig. 2(a) shows the fabricated ASIC that includes the designed capacitance-to-time converter. A special printed circuit board (PCB), reported in the experimental photograph in Fig. 2(b), was designed and manufactured to test the encapsulated integrated circuit. Different experiments were carried out to prove its correct operation and limitations [see Fig. 2(b)]. With a view to further applications, preliminary tests were considered for capacitance sensors in the 1-nF range and also in the 100-pF range. The application of the circuit to single-capacitance sensors with a fixed reference capacitor was also considered. Similar to the time domain simulations shown in Fig. 1(b), Fig. 2(c) reports an example of the main measured signals of the system. Considering $R_0 = 100\,\text{k}\Omega$ and $C_1 = C_2 = 105\,\text{pF}$, the traces of Fig. 2(c) reported from the top to the bottom

$$T = 2\,R_0\left(C_2\frac{\left(\frac{R_1}{R_1+R_2}+\frac{R_4}{R_3+R_4}\right)}{\left(1-\frac{R_1}{R_1+R_2}\right)\left(\frac{R_6}{R_5+R_6}\right)} - C_1\right) \tag{6}$$

$$PW = R_0\left(C_2\frac{\frac{R_1}{R_1+R_2}\cdot\frac{R_6}{R_5+R_6}+\frac{R_1}{R_1+R_2}+\frac{R_4}{R_3+R_4}-\frac{R_6}{R_5+R_6}}{\left(1-\frac{R_1}{R_1+R_2}\right)\frac{R_6}{R_5+R_6}} - 2\,C_1\right) \tag{7}$$

$$C_1 = \frac{1}{R_0}\,(PW - T)\left[\frac{\left(\frac{R_1}{R_1+R_2}+\frac{R_4}{R_3+R_4}\right)}{\left(\frac{R_1}{R_1+R_2}\quad\frac{R_6}{R_5+R_6}\right)-\frac{R_1}{R_1+R_2}-\frac{R_4}{R_3+R_4}-\frac{R_6}{R_5+R_6}}\right] - \frac{1}{R_0}\frac{T}{2} \tag{8}$$

$$C_2 = \frac{1}{R_0}\,(PW - T)\left[\frac{\left(1-\frac{R_1}{R_1+R_2}\right)\left(\frac{R_6}{R_5+R_6}\right)}{\left(\frac{R_1}{R_1+R_2}\quad\frac{R_6}{R_5+R_6}\right)-\frac{R_1}{R_1+R_2}-\frac{R_4}{R_3+R_4}-\frac{R_6}{R_5+R_6}}\right] \tag{9}$$

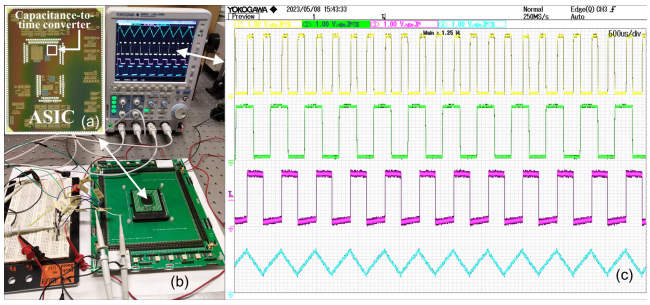


Fig. 2. (a) Fabricated designed ASIC. (b) Experimental setup. (c) Main signals of the proposed system during time-domain measurements.

correspond to V_o, V_{C1}, V_{C2}, and V_{INT}, respectively. As a case of example, Fig. 3 shows how the output frequency and duty-cycle change as a function of C_1 and C_2 capacitances, considering $R_0 = 100\,\text{k}\Omega$. In particular, Fig. 3(a) is obtained considering $C_1 = 60\,\text{pF}$ and $C_2 = 150\,\text{pF}$ ($T = 306.018\,\mu\text{s}$, $PW = 132.892\,\mu\text{s}$), Fig. 3(b) with $C_1 = C_2 = 105\,\text{pF}$ ($T = 209.275\,\mu\text{s}$, $PW = 73.440\,\mu\text{s}$), and Fig. 3(c) setting $C_1 = 150\,\text{pF}$ and $C_2 = 60\,\text{pF}$ ($T = 110.070\,\mu\text{s}$ and $PW = 28.300\,\mu\text{s}$).

The requirements on the time basis precision and accuracy for the measurement and the conversion of the output square-wave Vo are important to achieve high sensitivity and resolution values. In this regard, the maximum averaged rms jitter levels, measured on the rising/falling edges of the output square-wave signal V_o, are always lower than about 93 (differential capacitance) and 99 ns (single capacitance), which, in other words, represent the required minimum time basis precisions.

A. 1-nF Operation Range

For generating the differential capacitance behavior, C_1 and C_2 ranged oppositely between 400 and 1200 pF, while keeping their sum constant, with the help of standard nominal capacitors and capacitance decade boxes. V_o and the other signals were captured by an oscilloscope (YOKOGAWA DLM2034), also used to measure T and PW, as introduced in Section II. For R_0, values of $1\,\text{M}\Omega$, $100\,\text{k}\Omega$, and $10\,\text{k}\Omega$ were considered to obtain the time parameters within different ranges. So, the obtained results, compared to the theoretically calculated values, are collected in Fig. 4. DC is also included in the same graphs.

For testing the response of the circuit to nondifferential capacitance sensors, scans of C_1 from 400 to 1400 pF were performed with fixed $C_2 = 800$, pF. Then, the same experiment was repeated, interchanging C_1 and C_2. Results are shown in Fig. 5.

From these sets of experimental data, numerical fittings were performed to extract nominal values for the period (T_0), the pulsewidth (PW_0), and the associated sensitivities (S_T and S_{PW}). So, obtained values are collected in Table IV.

Some conclusions can be directly extracted from the data. The first one is that experimental data perfectly fit the theory. It is also shown that both single and differential modes can be used. Because the circuit output is more responsive to variations in C_2 [see (10) and (11)], using C_2 as the sensor

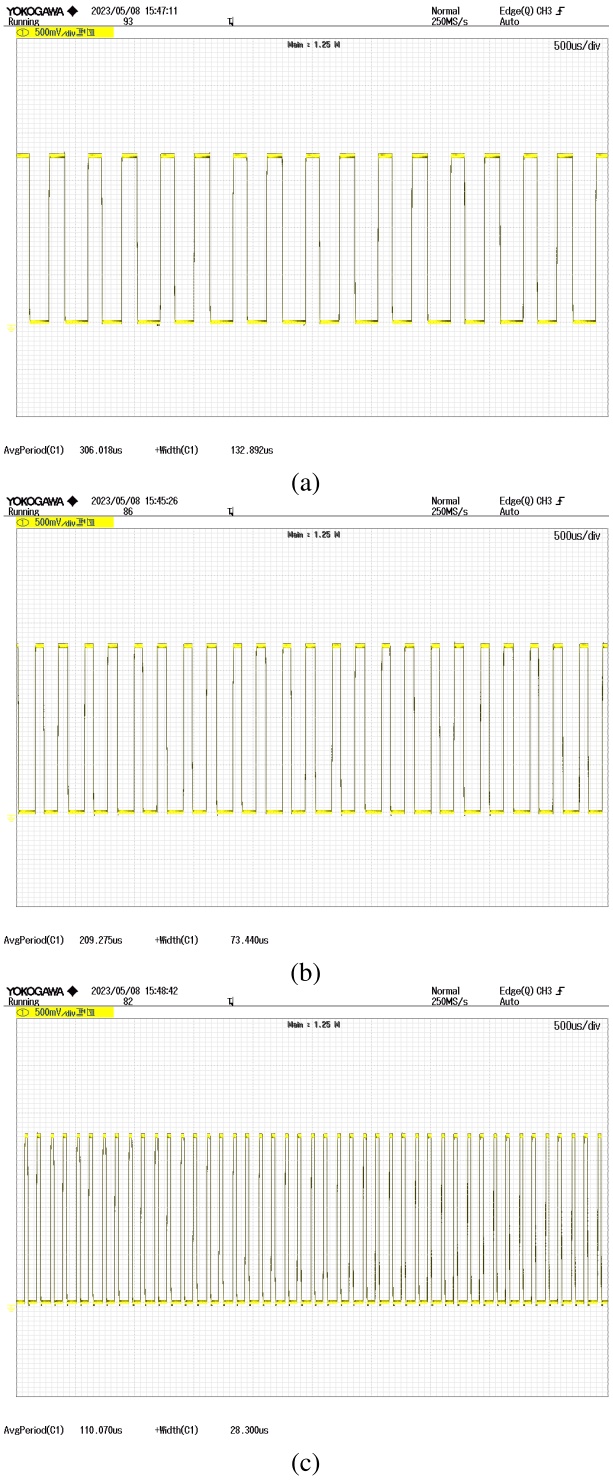


Fig. 3. V_o traces for different capacitance values: (a) $C_1 = 60$ pF, $C_2 = 150$ pF; (b) $C_1 = C_2 = 105$ pF; and (c) $C_1 = 105$ pF, $C_2 = 60$ pF.

maximizes the detection sensitivity, improves resolution, and minimizes error propagation during capacitance estimation. In contrast, using C_1 as the sensor would reduce the impact of its variations on the output, effectively reducing sensitivity. But the highest linearity is achieved with the differential topology. In any case, nominal values of T_0 and PW_0 and the sensitivities S_T and S_{PW} can be stated (from ms to µs) by selecting proper values of the external R_0 (from $1\,\text{M}\Omega$ to $10\,\text{k}\Omega$).

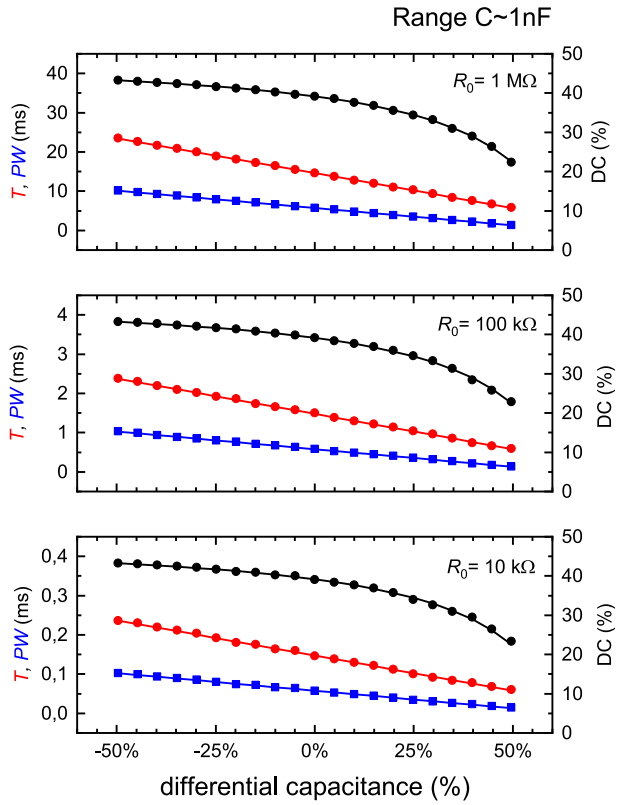


Fig. 4. Time response versus relative capacitance. Both C_1 and C_2 are variable from 800 to 1400 pF. Relative capacitance is defined as $(C_1 - C_2/(C_1 + C_2)$. The DC is included on the right axis of the graphs.

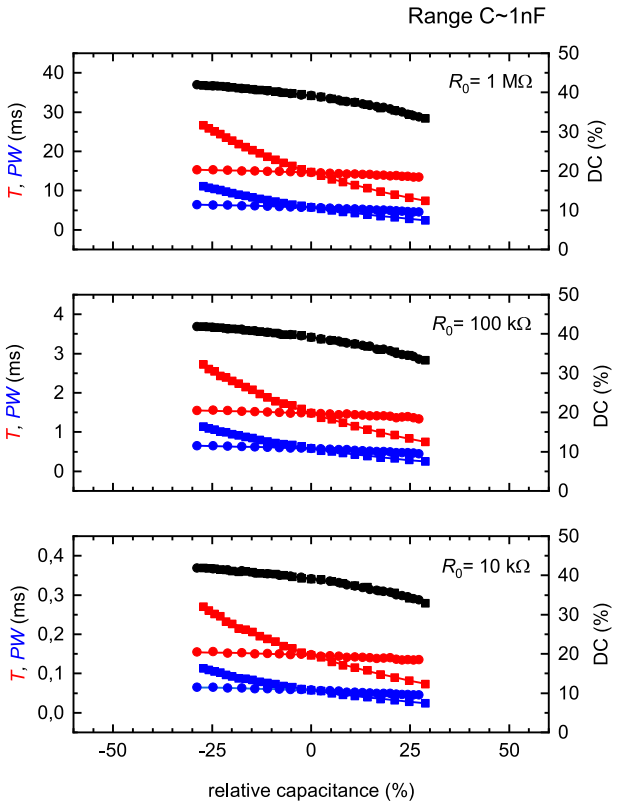


Fig. 5. Time response versus relative capacitance. (a) C_1 = 800 pF and C_2 ranging from 400 to 1400 pF. (b) C_2 = 800 pF and C_1 ranging from 400 to 1400 pF. Relative capacitance is defined as $(C_1 - C_2/(C_1 + C_2)$. The DC is included on the right axis of the graphs.

TABLE IV
PERFORMANCE PARAMETERS OF THE CIRCUIT FOR THE 1-NF RANGE

DIFFERENTIAL (C_1 variable and C_2 variable)

R_0	T_0 [ms]	S_T [µs/ΔpF]	PW_0 [ms]	S_{PW} [µs/ΔpF]
1 MΩ	14.6	8.1	5.73	4.0
100 kΩ	1.48	0.82	0.582	0.41
10 kΩ	0.148	0.082	0.0579	0.041

WITH C_1 AS REFERENCE (C_1 fixed and C_2 variable)

R_0	T_0 [ms]	S_T [µs/ΔpF]	PW_0 [ms]	S_{PW} [µs/ΔpF]
1 MΩ	15.6	16	6.16	7.1
100 kΩ	1.58	1.6	0.625	0.72
10 kΩ	0.156	0.16	0.0617	0.071

WITH C_2 AS REFERENCE (C_1 variable and C_2 fixed)

R_0	T_0 [ms]	S_T [µs/ΔpF]	PW_0 [ms]	S_{PW} [µs/ΔpF]
1 MΩ	14.5	1.5	5.63	1.5
100 kΩ	1.47	0.16	0.569	0.16
10 kΩ	0.146	0.017	0.0565	0.016

Finally, estimated values for C_1 and C_2 were calculated from measured T and PW and compared with nominal values. Results for every combination of both capacitors (C_1 variable/C_2 variable, C_1 variable/C_2 fixed, and C_1 fixed/C_2 variable) are shown in Fig. 6, while the errors analysis is reported in Table V.

Two direct conclusions can be extracted. Because the sensitivity of C_2 is higher than that of C_1, the error associated with its measurement is lower. Also, as expected, the measures

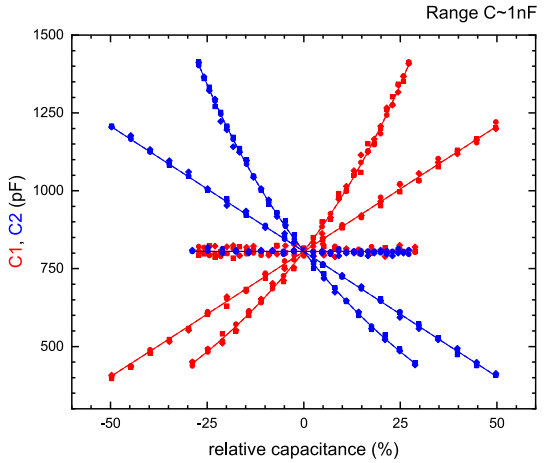


Fig. 6. Estimated values of C_1 and C_2 from T and PW measurements. Capacitance range 1 nF.

with higher R_0, related to higher T and PW (involving slower acquisition), imply lower errors.

B. 100-pF Range Capacitors

For generating differential capacitance behavior, C_1 and C_2 ranged oppositely between 50 and 170 pF, while keeping constant their sum, with the help of standard nominal capacitors and capacitance decade boxes. V_o and the other signals were captured by an oscilloscope, also used to measure T and PW, as introduced in Section II. For R_0, the values of

TABLE V
CAPACITANCE EVALUATION ERROR IN THE 1-NF RANGE

C_1 var. / C_2 var.	$R_0 = 1\,\text{M}\Omega$	$R_0 = 100\,\text{k}\Omega$	$R_0 = 10\,\text{k}\Omega$
C_1	1.2%	0.9%	0.9%
C_2	0.3%	0.7%	1.0%
C_1 var. / C_2 fix.	$R_0 = 1\,\text{M}\Omega$	$R_0 = 100\,\text{k}\Omega$	$R_0 = 10\,\text{k}\Omega$
C_1	0.9%	1.4%	1.3%
C_2	0.2%	0.4%	0.8%
C_1 fix. / C_2 var.	$R_0 = 1\,\text{M}\Omega$	$R_0 = 100\,\text{k}\Omega$	$R_0 = 10\,\text{k}\Omega$
C_1	1.1%	0.8%	1.5%
C_2	0.2%	0.6%	0.8%

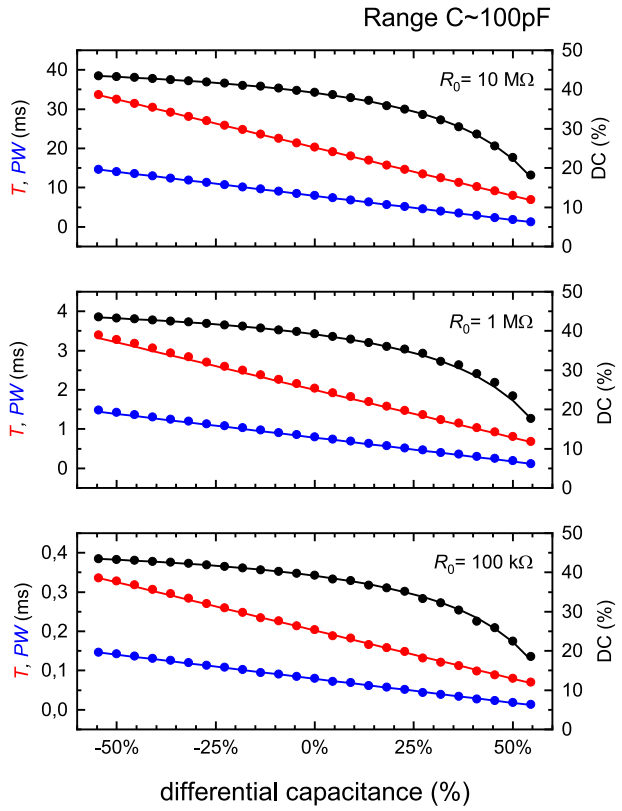


Fig. 7. Time response versus relative capacitance. Both C_1 and C_2 are variable from 40 to 140 pF. Relative capacitance is defined as $(C_1 - C_2/(C_1 + C_2)$. The DC is included on the right axis of the graphs.

10 MΩ, 1 MΩ, and 100 kΩ were considered to obtain the time parameters within different ranges. So, the results obtained, compared to the theoretically calculated values, are collected in Fig. 7. DC is also included in the same graphs.

From these sets of experimental data, numerical fittings were performed to extract nominal values for the period (T_0), the pulsewidth (PW_0), and the associated sensitivities (S_T and S_{PW}). So, obtained values are collected in Table VI.

Then, scans of C_1 from 50 to 170 pF were performed with fixed $C_2 = 110$ pF. The same experiment was repeated, interchanging C_1 and C_2. Results are shown in Fig. 8.

As with the 1-nF case, experimental data perfectly fit the theory. It is also shown that both single and differential modes can be used. Because the factor multiplying C_2 is greater than the one multiplying C_1 in equations (10) and (11), the system

TABLE VI
PERFORMANCE PARAMETERS OF THE CIRCUIT FOR THE 100-PF RANGE

DIFFERENTIAL (C_1 variable and C_2 variable)

R_0	T_0 [ms]	S_T [µs/ΔpF]	PW_0 [ms]	S_{PW} [µs/ΔpF]
10 MΩ	20.3	110	7.94	56
1 MΩ	2.04	11	0.802	5.6
100 kΩ	0.203	1.1	0.0794	0.57

WITH C_1 AS REFERENCE (C_1 fixed and C_2 variable)

R_0	T_0 [ms]	S_T [µs/ΔpF]	PW_0 [ms]	S_{PW} [µs/ΔpF]
10 MΩ	20.9	210	8.21	93
1 MΩ	2.08	21	0.819	9.3
100 kΩ	0.208	2.1	0.0816	0.93

WITH C_2 AS REFERENCE (C_1 variable and C_2 fixed)

R_0	T_0 [ms]	S_T [µs/ΔpF]	PW_0 [ms]	S_{PW} [µs/ΔpF]
10 MΩ	20.2	20	7.90	20
1 MΩ	2.00	1.8	0.781	2.0
100 kΩ	0.202	0.20	0.0079	0.20

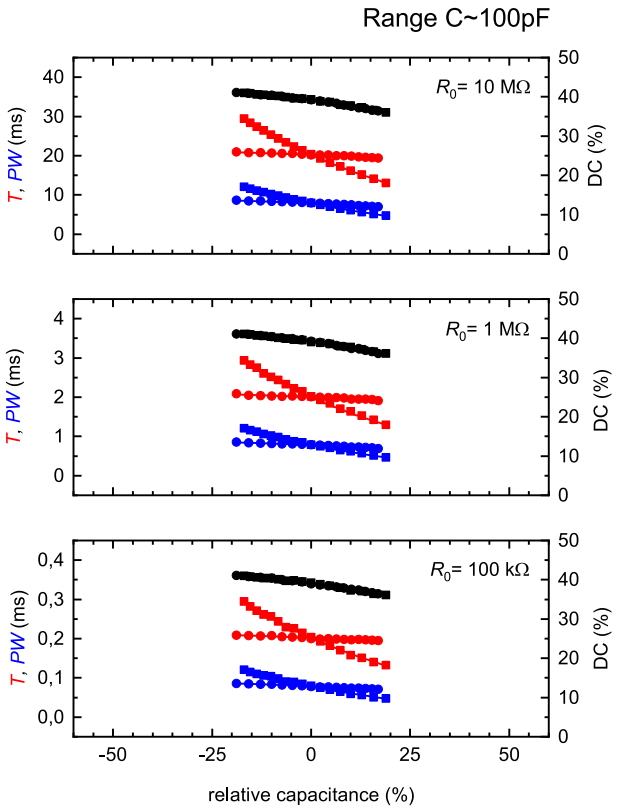


Fig. 8. Time response versus relative capacitance. (a) $C_1 = 110$ pF and C_2 ranging from 40 to 140 pF. (b) $C_2 = 110$ pF and C_1 ranging from 40 to 140 pF. Relative capacitance is defined as $(C_1 - C_2/(C_1 + C_2)$. The DC is included on the right axis of the graphs.

is more sensitive to C_2 changes. Then, C_2 should be the sensor and C_1 the reference capacitor. But the highest linearity is achieved with the differential topology. In any case, nominal values of T_0 and PW_0 and the sensitivities S_T and S_{PW} can be stated (from ms to µs) by selecting proper values of the external R_0 (from 10 MΩ to 100 kΩ).

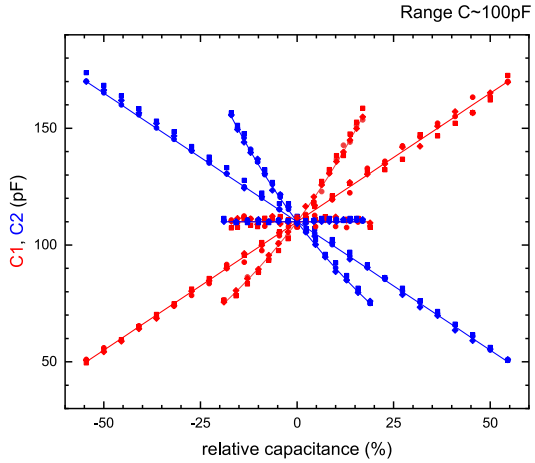


Fig. 9. Estimated values of C_1 and C_2 from T and PW measurements. Capacitance range 100 pF.

TABLE VII
CAPACITANCE EVALUATION ERROR IN THE 100-PF RANGE

C_1 var. / C_2 var.	$R_0 = 10\,\text{M}\Omega$	$R_0 = 1\,\text{M}\Omega$	$R_0 = 100\,\text{k}\Omega$
C_1	1.5%	1.1%	0.9%
C_2	0.4%	2.0%	1.0%
C_1 var. / C_2 fix.	$R_0 = 10\,\text{M}\Omega$	$R_0 = 1\,\text{M}\Omega$	$R_0 = 100\,\text{k}\Omega$
C_1	1.3%	1.9%	0.6%
C_2	0.4%	0.7%	0.4%
C_1 fix. / C_2 var.	$R_0 = 10\,\text{M}\Omega$	$R_0 = 1\,\text{M}\Omega$	$R_0 = 100\,\text{k}\Omega$
C_1	1.3%	1.5%	0.8%
C_2	0.4%	1.4%	0.7%

Finally, estimated values for C_1 and C_2 were obtained from the measured T and PW and compared with the nominal values. Results are shown in Fig. 9, and the errors reported in Table VII.

As with the 1-nF case, when the sensitivity of C_2 is higher than that of C_1, the error associated with its measurement is lower. Also, again, the measures with higher R_0, related to higher T and PW (involving slower acquisition), imply lower errors. However, in this case, due to the lower precision in measuring the nominal values of the tested capacitors, along with the higher relative effect of parasitic capacitance, these relationships become less evident.

C. PTV Characterization

Fig. 10 shows relative errors achieved with the estimation of C_2 under PVT variations compared to the values obtained with typical operating conditions (i.e., TT @ $V_{DD} = 1.8\,\text{V}$ and $T = 25\,^\circ\text{C}$). This data demonstrates that various fabricated ASICs/dies, having different characteristics and/or under specific operating conditions (PVT), have been measured and tested, showing a maximum relative error always less than $\pm 3\%$ concerning the typical case (reference TT ASIC/die). In particular, the process and temperature variations mainly affect the performance of the circuit, while variations for V_{DD} changes are negligible (within the range $V_{DD} = 1.6\,\text{V}$ and $V_{DD} = 2.0\,\text{V}$), as expected since the proposed capacitance-to-time converter is based on a square-wave relaxation oscillator.

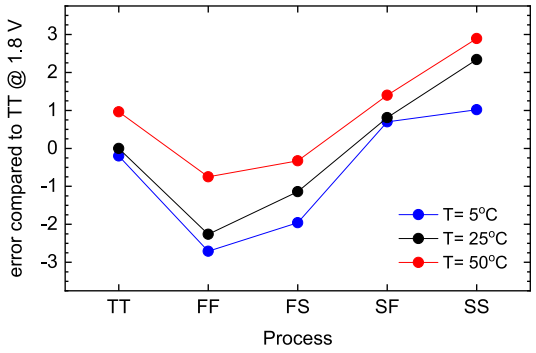


Fig. 10. Maximum relative error achieved with the estimation of C_2 under PVT variations compared to TT conditions $V_{DD} = 1.8\ V$ and $T = 25\,^\circ$ C.

IV. PRACTICAL APPLICATIONS: EXPERIMENTAL MEASUREMENTS AND RESULTS

Recent advances in sensing technologies [44] include integrating capacitive sensors characterized by exceptionally low nominal values and sensitivities [45]. Within these contexts, the implementation of the proposed circuit can effectively illustrate its advantages in both single-ended and differential capacitance configurations. In this sense, we propose two real-world applications in which this circuit can be used: small-volume liquid level measurement and dielectric constant characterization. We also provide experimental evidence of this performance.

A. Small Liquid-Level Measurement

Measuring liquid levels is a key task in many industrial and scientific processes. Mechanical (gauges) or reflectometric (ultrasonic, radar, or laser)-based approaches commonly used in industry cannot be applied to measure small liquid volumes due to their size [46]. For these scenarios, capacitance-based sensors are preferred. In these cases, the detectivity limits are related to the system's topology (integration of the capacitor terminals with the liquid container) and the sensitivity of the electronic interface. The proposed circuit can fit different sensor topologies, such as those using reference and active capacitive sensors [47] or true differential capacitive sensors [30]. To focus on the performance of the circuit, we have considered a 1-mL COTS sensor, directly connected to the proposed circuit, using $R_0 = 10\,\text{M}\Omega$ as the external resistor and $C_1 = 1.2\,\text{pF}$ as the reference capacitor. The experimental results for distilled water, methanol, and chloroform are shown in Fig. 11. From linear fits of the data in Fig. 11, results collected in Table VIII were extracted. These data are extracted from repeated measurements, so evaluating reduced error/uncertainty and standard deviation from the expected nominal values demonstrates the high repeatability of the measurements.

As observed, the system can resolve changes in the liquid level below the mL. Due to the different dielectric constants, different sensitivities, and so different resolutions (i.e., detectivities) are observed for the various liquids employed for the measurements since the liquid level variation linearly changes

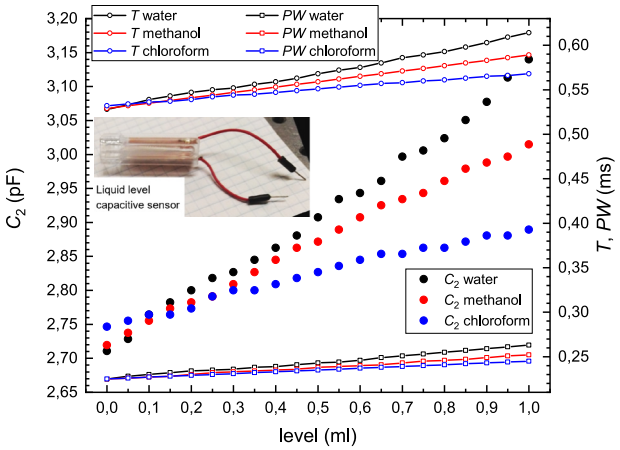


Fig. 11. Measured values of *PW* and *T*, and derived values of C_2 ($C_1 = 1.2$ pF) from *T* and *PW* from liquid-level measurement of distilled water, ethanol, and chloroform.

TABLE VIII
LIQUID-LEVEL MEASUREMENT OF WATER, METHANOL, AND CHLOROFORM

Measured liquid	$C_{2,0}$ (pF)	Senitivity (fF/ml)	Error (fF)	Resolution (µL)
Water	2.710 ± 0.005	407 ± 8	50	110
Methanol	2.724 ± 0.002	295 ± 3	20	70
Chloroform	2.750 ± 0.002	145 ± 4	50	150

the overall sensor capacitance value. The drift on the empty value of C_2 is attributed to limitations of the cleaning of the container between measurements. On average, the resolution of the sensor/circuit system is about 100 μL in each case. This value is hard to compare with the literature because most of the investigations focus on the sensor topology, with experimental data well above 1 mL. On the other hand, by taking 10 V/µs as the slew rate of the circuit and combining the sensitivities of the circuit and the sensor, the theoretical resolution limit of the system should be 5 µL, requiring a 5-MHz bandwidth minimum microcontroller interface.

B. Dielectric Constant Measurement

As mentioned in Section I, some capacitive sensors (mainly gases or liquids) are based on the change in the permittivity of the dielectric material of a capacitor ($C = A\epsilon/d$). In real applications (e.g., in point-of-care (PoC) measurements), the available amount of the material under test is usually small, or the variation of the constant is small (e.g., small changes in the concentration). To validate the use of the proposed solution in these applications, a 3-D-printed capacitive sensor was specifically designed and fabricated. It was comprised of a $(25 \times 22 \times 2)\,\text{mm}^3$ microfluidics chip with an inner meandered channel of 1 mm diameter (160 µL of volume), and two rectangular copper pads covering both major faces of the chip. The final device is displayed as an inset in Fig. 12. To test it, the channel was filled with different liquids (chloroform, methanol, and water) with the help of a syringe. We used $R_0 = 10\,\text{M}\Omega$ as the external resistor and $C_1 = 1.2\,\text{pF}$ as the reference capacitor. The measured values are

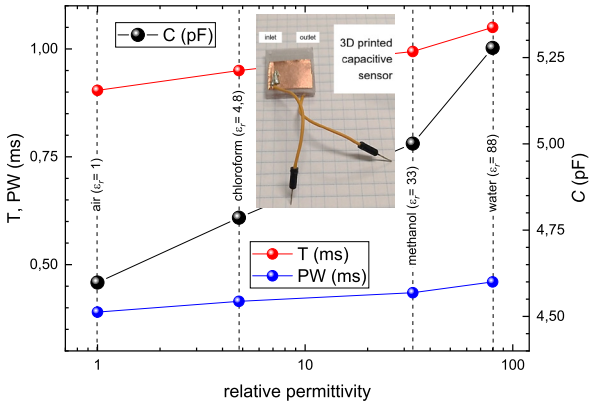


Fig. 12. Estimated values of C_1 and C_2 from *T* and *PW* measurements as a function of the liquid level.

shown in Fig. 12. As observed, the system can unambiguously identify the substances of interest from a very small amount of them, which is very useful in microfluidics-based devices. We should keep in mind that the container has not been optimized. By following the same argumentation as before, it can be stated that, theoretically, the system should be able to distinguish variations of the relative permittivity constant close to 2% in the whole range from 1 to 100.

V. CONCLUSION

The present capacitance-to-time converter has been demonstrated as a robust and versatile solution for interfacing capacitive sensors, especially in scenarios demanding compact, low-power, and high-resolution circuits. Through CMOS integration and careful circuit design, the system maintains consistent performance across a wide capacitance range, with configurable sensitivity enabled by external resistance tuning.

Experimental characterization across both single and differential configurations confirmed theoretical expectations and highlighted the benefits of differential operation in terms of linearity and noise rejection. The circuit's compatibility with a variety of sensing modalities, validated through applications in liquid-level measurement or dielectric characterization, supports its adaptability to real-world use cases.

Notably, the converter achieved accurate and repeatable measurements down to the femtofarad scale, using a minimal silicon footprint and power budget. These results suggest that the proposed design can serve as a general-purpose front-end for capacitive sensors, particularly in embedded or resource-constrained environments. In particular, considering the reported achievements, especially in term of high resolution, low power, and compatibility with low-capacitance sensors, the proposed system can be considered an excellent candidate for advancing wearable optical biosensors, such as photoplethysmography (PPG), pulse oximetry, near-infrared spectroscopy (NIRS), as well as MEMS integrated devices for biomedical applications.

REFERENCES

[1] K. S. Patle, R. Saini, A. Kumar, S. G. Surya, V. S. Palaparthy, and K. N. Salama, "IoT enabled, leaf wetness sensor on the flexible substrates for in-situ plant disease management," *IEEE Sensors J.*, vol. 21, no. 17, pp. 19481–19491, Sep. 2021.

[2] Y. Zeng, Y. Qin, Y. Yang, and X. Lu, "A low-cost flexible capacitive pressure sensor for health detection," *IEEE Sensors J.*, vol. 22, no. 8, pp. 7665–7673, Apr. 2022.

[3] D. Kosmas, H.-P. van Jonbergen, M. Schouten, M. Abayazid, and G. Krijnen, "A sensorized 3-D printed gap-gauge aiming to improve knee prosthesis survival," *IEEE Sensors J.*, vol. 24, no. 21, pp. 34625–34634, Nov. 2024.

[4] W. Deabes and K. M. J. Khayyat, "Image reconstruction in electrical capacitance tomography based on deep neural networks," *IEEE Sensors J.*, vol. 21, no. 22, pp. 25818–25830, Nov. 2021.

[5] E. Zampetti et al., "Design and optimization of an ultra thin flexible capacitive humidity sensor," *Sens. Actuators B, Chem.*, vol. 143, no. 1, pp. 302–307, Dec. 2009.

[6] W. Fan, M. Chen, H. Jin, and Y. Wang, "Multi-layer concentric ring differential capacitance displacement sensor," *Measurement*, vol. 136, pp. 615–621, Mar. 2019.

[7] L. Zhang, M. Gao, R. Wang, Z. Deng, and L. Gui, "Stretchable pressure sensor with leakage-free liquid-metal electrodes," *Sensors*, vol. 19, no. 6, p. 1316, Mar. 2019.

[8] J. A. Dobrzynska and M. A. M. Gijs, "Polymer-based flexible capacitive sensor for three-axial force measurements," *J. Micromech. Microeng.*, vol. 23, no. 1, Jan. 2013, Art. no. 015009.

[9] A. Rivadeneyra, J. Fernández-Salmerón, M. Agudo, J. A. López-Villanueva, L. F. Capitan-Vallvey, and A. J. Palma, "Design and characterization of a low thermal drift capacitive humidity sensor by inkjet-printing," *Sens. Actuators B, Chem.*, vol. 195, pp. 123–131, May 2014.

[10] V. Zega et al., "The first 3D-printed and wet-metallized three-axis accelerometer with differential capacitive sensing," *IEEE Sensors J.*, vol. 19, no. 20, pp. 9131–9138, Oct. 2019.

[11] L. Beker, A. Maralani, L. Lin, and A. P. Pisano, "Modeling, fabrication, and characterization of SiC concentrically matched differential capacitance output pressure sensors," *Sens. Actuators A, Phys.*, vol. 273, pp. 293–302, Apr. 2018.

[12] E. Unigarro, J. C. Bohórquez, A. Achury, F. Ramirez, J. Sacristán, and F. Segura-Quijano, "Differential capacitive pressure sensor design based on standard CMOS," *Electron. Lett.*, vol. 53, no. 11, pp. 737–739, May 2017.

[13] K. H.-L. Chau, S. R. Lewis, Y. Zhao, R. T. Howe, S. F. Bart, and R. G. Marcheselli, "An integrated force-balanced capacitive accelerometer for low-g applications," *Sens. Actuators A, Phys.*, vol. 54, nos. 1–3, pp. 472–476, Jun. 1996.

[14] M. Narducci, L. Yu-Chia, W. Fang, and J. Tsai, "CMOS MEMS capacitive absolute pressure sensor," *J. Micromech. Microeng.*, vol. 23, no. 5, May 2013, Art. no. 055007.

[15] M. Keshavarzi and J. Yavand Hasani, "Design and optimization of fully differential capacitive MEMS accelerometer based on surface micromachining," *Microsyst. Technol.*, vol. 25, no. 4, pp. 1369–1377, Apr. 2019.

[16] J. Cai et al., "Design of interface ASIC with power-saving switches for capacitive accelerometers," *Micromachines*, vol. 16, no. 1, p. 96, Jan. 2025.

[17] A. Ria, M. Cicalini, P. Bruschi, M. Piotto, and M. Dei, "Wide-range low-power low-voltage integrated capacitance-to-digital converter for on-body sweat-rate sensing," *IEEE Sensors J.*, vol. 25, no. 6, pp. 10250–10260, Mar. 2025.

[18] M. S. Arefin, J.-M. Redoute, and M. R. Yuce, "A MEMS interface IC with low-power and wide-range frequency-to-voltage converter for biomedical applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 455–466, Apr. 2016.

[19] A. De Marcellis, G. Ferri, and P. Mantenuto, "A CCII-based non-inverting Schmitt trigger and its application as astable multivibrator for capacitive sensor interfacing," *Int. J. Circuit Theory Appl.*, vol. 45, no. 8, pp. 1060–1076, Aug. 2017.

[20] J. A. Hidalgo-López, "A simple digital readout circuit for differential resistive or capacitive sensors," *Meas. Sci. Technol.*, vol. 34, no. 8, Aug. 2023, Art. no. 085117.

[21] J. A. Hidalgo-López, "Direct interface circuit for capacitive sensors affected by parasitic series resistances," *IEEE Trans. Instrum. Meas.*, vol. 72, pp. 1–8, 2023.

[22] Z. Czaja, "A new approach to capacitive sensor measurements based on a microcontroller and a three-gate stable RC oscillator," *IEEE Trans. Instrum. Meas.*, vol. 72, pp. 1–9, 2023.

[23] Z. Czaja, "Measurement method for capacitive sensors for microcontrollers based on a phase shifter," *Measurement*, vol. 192, Mar. 2022, Art. no. 110890.

[24] L. Areekath, B. George, and F. Reverter, "An auto-balancing capacitance-to-pulse-Width converter for capacitive sensors," *IEEE Sensors J.*, vol. 21, no. 1, pp. 765–775, Jan. 2021.

[25] A. Depari et al., "Autobalancing analog front end for full-range differential capacitive sensing," *IEEE Trans. Instrum. Meas.*, vol. 67, no. 4, pp. 885–893, Apr. 2018.

[26] R. Tirupathi and S. K. Kar, "On-chip implementable autocalibration of sensor offset for differential capacitive sensor interfaces," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–9, 2021.

[27] X. Li, P. Wang, G. Li, and Y. Zhang, "Design of a novel self-test-on-chip interface ASIC for capacitive accelerometers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 7, pp. 2834–2843, Jul. 2023.

[28] R. A. Brookhuis, T. S. J. Lammerink, and R. J. Wiegerink, "Differential capacitive sensing circuit for a multi-electrode capacitive force sensor," *Sens. Actuators A, Phys.*, vol. 234, pp. 168–179, Oct. 2015.

[29] N. Madhu Mohan, A. R. Shet, S. Kedarnath, and V. Jagadeesh Kumar, "Digital converter for differential capacitive sensors," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 11, pp. 2576–2581, Nov. 2008.

[30] A. De Marcellis, C. Reig, and M.-D. Cubells-Beltrán, "A capacitance-to-time converter-based electronic interface for differential capacitive sensors," *Electronics*, vol. 8, no. 1, p. 80, Jan. 2019.

[31] L. Areekath, B. George, and F. Reverter, "A closed-loop capacitance-to-frequency converter for single-element and differential capacitive sensors," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 11, pp. 8773–8782, Nov. 2020.

[32] P. Bruschi, N. Nizza, and M. Piotto, "A current-mode, dual slope, integrated capacitance-to-pulse duration converter," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1884–1891, Sep. 2007.

[33] Z. Tan, S. H. Shalmany, G. C. M. Meijer, and M. A. P. Pertijs, "An energy-efficient 15-bit capacitive-sensor interface based on period modulation," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1703–1711, Jul. 2012.

[34] Y. He, Z. Y. Chang, L. Pakula, S. H. Shalmany, and M. Pertijs, "27.7 a 0.05 mm^2 1V capacitance-to-digital converter based on period modulation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 58, Jun. 2015, pp. 486–487.

[35] N. Nizza, M. Dei, F. Butti, and P. Bruschi, "A low-power interface for capacitive sensors with PWM output and intrinsic low pass characteristic," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 6, pp. 1419–1431, Jun. 2013.

[36] J. H.-L. Lu, M. Inerowicz, S. Joo, J.-K. Kwon, and B. Jung, "A low-power, wide-dynamic-range semi-digital universal sensor readout circuit using pulsewidth modulation," *IEEE Sensors J.*, vol. 11, no. 5, pp. 1134–1144, May 2011.

[37] M.-L. Sheu, W.-H. Hsu, and L.-J. Tsao, "A capacitance-ratio-modulated current front-end circuit with pulsewidth modulation output for a capacitive sensor interface," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 2, pp. 447–455, Feb. 2012.

[38] M. S. Arefin, J.-M. Redouté, and M. R. Yuce, "A low-power and wide-range MEMS capacitive sensors interface IC using pulse-width modulation for biomedical applications," *IEEE Sensors J.*, vol. 16, no. 17, pp. 6745–6754, Sep. 2016.

[39] F. Aezinia and B. Bahreyni, "Low-power, parasitic-insensitive interface circuit for capacitive microsensors," *IET Circuits, Devices Syst.*, vol. 10, no. 2, pp. 104–110, Mar. 2016.

[40] H. Hao et al., "A wireless artificial mechanoreceptor in 180-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 6, pp. 2907–2920, Jun. 2021.

[41] R. Tirupathi and S. K. Kar, "Low-offset differential output switched-capacitor interface for micro-capacitive acceleration sensors," *IET Sci., Meas. Technol.*, vol. 15, no. 3, pp. 279–291, May 2021.

[42] M. Cicalini, M. Piotto, P. Bruschi, and M. Dei, "Design of a capacitance-to-digital converter based on iterative delay-chain discharge in 180 nm CMOS technology," *Sensors*, vol. 22, no. 1, p. 121, Dec. 2021.

[43] H. Darwish, C. Reig, M. D. Cubells-Beltran, G. Leger, and A. De Marcellis, "CMOS capacitance-to-time converter-based interface for differential capacitive sensors," in *Proc. Global Congr. Electr. Eng. (GC-ElecEng)*, Sep. 2020, pp. 61–64.

[44] O. Kanoun, A. Y. Kallel, and A. Fendri, "Measurement methods for capacitances in the range of 1 pF–1 nF: A review," *Measurement*, vol. 195, May 2022, Art. no. 111067.

[45] J. A. Uc-Martín, A. Ortega-Aguilar, A. Guadarrama-Santana, and A. García-Valenzuela, "Variable-capacitance sensor to measure the evaporation rate and lifetime of microliter droplets," *IEEE Sensors J.*, vol. 23, no. 8, pp. 8443–8450, Apr. 2023.
[46] P. Mohindru, "Development of liquid level measurement technology: A review," *Flow Meas. Instrum.*, vol. 89, Mar. 2023, Art. no. 102295.
[47] H. Canbolat, "A novel level measurement technique using three capacitive sensors for liquids," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 10, pp. 3762–3768, Oct. 2009.

Hala Darwish received the master's degree in microelectronics from the University of Seville, Seville, Spain, in 2010. She is pursuing the Ph.D. degree with the University of Valencia, Burjassot, Spain.

Her research focuses on analog and mixed-signal systems for sensor applications.

Càndid Reig (Senior Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in physics from the University of Valencia, Burjassot, Spain, in 1994, 1995, and 2000, respectively.

In 1997, he joined the Department of Applied Physics, University of Valencia, where he developed his doctoral thesis. In 2002, he was an Assistant Professor with the University of Valencia and a Postdoctoral Fellow with INESC-MN, Lisbon, Portugal, working on sensor integration. He has been an Associate Professor with the Department of Electronic Engineering, University of Valencia, since 2007, where he teaches and does research. He also served as an external consultant for Analog Devices in 2013 and 2015 and ams OSRAM from 2024 to 2025. He has been a researcher and principal investigator in different national and international scientific research projects. He has published about 50 JCR journal articles, contributed more than 50 works to conferences, edited a book, and co-authored six book chapters. He actively participates in periodic international conference program committees and acts as a referee for different research journals. His current research interests include the development of sensors (mainly magnetic and vision) and their integration at the integrated circuit level.

Dr. Reig was a co-recipient of the IETE-J C Bose Memorial Award in 2011 and the Magnetic Society of Japan Best Publication Award in 2014. He was the General Co-Chair of the IEEE Sensors Conference, Valencia, in 2014, and the Chair of the Spanish Chapter of the IEEE Sensors Council, from 2015 to 2020.

Gildas Leger received the Ingénieur en Génie Physique degree from l'Institut National des Sciences Appliquées (INSA) at Rennes, Rennes, France, in 1999, and the Ph.D. degree in microelectronics from the University of Seville, Seville, Spain, in 2007.

Since 2008, he has held the position of Tenured Scientist for the Spanish National Science Council (CSIC), Microelectronics Institute of Seville (IMSE-CNM), Seville. His main research interests are focused on both the design and test of AMS-RF circuits, with a particular emphasis on space applications (radiation hardened design) and data converters.

Dr. Leger has repeatedly served as a member of the Program Committee for several important conferences in the field of testing, like DATE or ETS. He has been an Analog Topic Chair and a Special Session Chair at ETS for several years, a General Chair and a Program Chair of the IMSTW workshop in 2017 and 2015, respectively.

Guido Di Patrizio Stanchieri (Member, IEEE) received the master's (cum laude) and Ph.D. degrees in electronic engineering from the University of L'Aquila, L'Aquila, Italy, in 2017 and 2021, respectively.

From 2016 to 2022, he joined an external scientific collaboration with the Department of Industrial and Information Engineering and Economics, University of L'Aquila. Since 2023, he has been an RTDa Assistant Professor with the Department of Information Engineering, Computer Science and Mathematics (DISIM), University of L'Aquila. His research interests include the design and implementation of digital electronic circuits and systems for signal processing and data communication in biomedical and robotics integrated applications.

Orazio Aiello (Senior Member, IEEE) received the B.Sc. and M.Sc. (cum laude) degrees from the University of Catania, Catania, Italy, in 2005 and 2008, respectively, the M.Sc. (cum laude) degree from Scuola Superiore di Catania, Catania, Italy, in 2009, and the Ph.D. degree from Politecnico di Torino, Turin, Italy, in 2013.

He was a Research Fellow with Politecnico di Torino, in a joint project with FIAT-Chrysler Automobiles, Turin. He was a Mixed Signal IC Designer and an EMC Consultant with STMicroelectronics, Castelletto, Italy, from 2008 to 2009, and NXP-Semiconductors, Nijmegen, The Netherlands, in 2014. He was a Visiting Ph.D. Student with Monash University, Melbourne, VIC, Australia, in 2013, and a Visiting Fellow with the University of Sydney, Sydney, NSW, Australia, and The University of New South Wales, Sydney, in 2015 and 2016, respectively. Since 2015, he has been with the Green IC Group, National University of Singapore, Singapore, where he has also been a Marie Skłodowska-Curie Individual and a Global Fellow. He is currently a tenure-track Assistant Professor with the University of Genoa, Genoa, Italy. His main research interests include energy-efficient analog-mixed signal circuits and sensor interfaces.

Dr. Aiello is a member of the IEEE CASS Microlearning AdHoc Committee. He is/was a Technical Program Committee Member of a number of conferences, such as NORCAS and APCCAS. He is an Associate Editor of *IET Electronics Letters*. He serves as a regular reviewer for several IEEE journals.

Andrea De Marcellis (Member, IEEE) received the Laurea degree in electronic engineering and the Ph.D. degree in microelectronics from the University of L'Aquila, L'Aquila, Italy, in 2005 and 2009, respectively.

He is currently an Associate Professor of Electronics at the Department of Information Engineering, Computer Science and Mathematics (DISIM), University of L'Aquila, and the Head of the Electronic and Photonic Integrated Circuits and Systems Laboratory (EPICS Lab) and the Digital Health Technologies Laboratory (DHT Lab). He has co-authored a book and two book chapters, and more than 170 scientific publications in international journals and conference proceedings. His main research activities concern the design of mixed-signal electronic and optoelectronic integrated circuits and systems for signal conditioning, data processing, optical sensing, and communication links (data and power) for biomedical applications.

Dr. De Marcellis is the Chair of the Technical Committee "Optoelectronic Sensing Systems" of the IEEE Italy Sensors Chapter and an Associate Editor of the IEEE ACCESS journal.