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MARIO TINARI

Coordinatore del corso

Ch.mo Prof. VITTORIO CORTELLESSA

Tutor

Ch.mo Prof. CARLO CECATI

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Multilevel Converters: Hardware Design, Advanced Modulation Techniques and Experimental Prototype Validation

Mario Tinari

PhD Coordinator
Prof. Vittorio Cortellessa

Supervisors
Prof. Carlo Cecati

Prof. Concettina Buccella

Prof. Maria Gabriella Cimoroni

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1 Abstract

During the last two decades, the need of reducing global warming, all forms of pollution and the need of increasing energy efficiency in all fields, is transforming the way the energy in produced, transmitted, distributed and utilized. In this scenario, power electronic converters represent a key element because of their "unique" capability to manipulate and/or transform, and/or control huge amounts of electric energy, according to simple or complex control laws implemented using digital computer device. Renewable energy, smart grids, electric transportation cannot be used without power converters, therefore, modern power converters are those unique devices driving the transition from conventional to clean energy.

The existing limits of semiconductor's technology conflict with the high values of power, voltages and currents required in a large amount of applications and for this reason multilevel converters have been proposed because their allow to overcome technological limits of power devices.

The whole Ph.D. activity, summarized in part with this thesis, has been developed in this context and mostly within the frame of the industrial research project titled: "CoMoDes", by DigiPower Ltd. L'Aquila, a "PMI Innovativa", born in 2007 as University of L'Aquila spin-off [1]. The grant, awarded by the Italian Ministry of Economic Development (MISE) with the number: F/050220/01-02-03/X32 - PON - H2020, Call 2016, has regarded the study and the development of modular multilevel converters (MMC) for the integration of renewable energy sources and for the electric mobility in the smart grid environment. The project, while using a methodology typical of applied scientific research, has addressed almost all main aspects of multilevel converters technology: topologies, applications, control, modulation, hardware and has involved the Author of this Ph.D. Thesis in a significant number of activities.

The project has dealt with the study, design and realization of a three-phase, 33-level converter with rated phase voltage: 10 kV @ 35 A_{rms}, resulting total power close to 1 MW. Some prototypes of the modular multilevel converter are now available at DigiPower Ltd Lab and utilized as R&D systems in relevant research branches, currently: smart grids and electric transportation.

The developed architecture is a cascade H-bridge (CHB) topology and it grants higher flexibility, modularity and fault tolerant characteristics with respect to other CHB-MC. Each H-bridge module is equipped with its own DSP unit, which collects module's information (current, voltage, error status, temperature etc.) and transmits them to the main control board, the latter equipped with a FPGA, a CPLD

and a DSP controllers. The main control board analyzes the state of each H-bridge and applies the required modulation signals to the system according to implemented control and modulation algorithms; it takes immediate decisions in case of incoming fault, thus improving the overall reliability and flexibility of the system. The local DSPs can be optionally programmed in order to implement distributed control algorithms, exploiting the unique true multiprocessing capability.

The advanced hardware (HW), combined with innovative fundamental frequency modulations developed in parallel with the HW and with control algorithms, offer high flexibility and efficiency, especially in high power applications; moreover they reduce switching losses and harmonic contents in output waveforms. Therefore, developed system significantly improves the power quality and grants a reduction in the average device switching frequency, while minimizing cost and size of the output power filter.

Author's main contributions to the above project can be found in the following parts:

- Hardware design of the power modules
- Hardware design of the system control board
- Implementation of the innovative modulation techniques for the harmonic content reduction
- Debug, tuning, and implementation of the control algorithms
- Prototype validation and experimental tests.

The design of such a kind of converters is an uncharted problem area and the completion of the whole project including the realization of a fully working experimental prototype and its SW companions has been a true challenge which has required almost three years of work and relevant skills in different areas of the power electronics; the realization of a high power prototype of this kind, requires a huge investment and relevant laboratory facilities: for the above mentioned reasons, the results achieved in this dissertation would not have been possible without the full support of DigiPower Ltd [1] and its very highly qualified staff.

The enhanced performance of the proposed HW is supported by results achieved with the advanced and innovative fundamental frequency modulation techniques, specifically developed and implemented as a part of this PhD thesis.

Operations and functionalities of the converter and of the presented algorithms have been extensively verified by simulation in MATLAB/Simulink framework [2] and then implemented and tested on the prototype. Several tests have been performed choosing different topologies and applications, in particular on a grid-connected three-phase static synchronous compensator (STATCOM) and a three-phase permanent magnet synchronous motor drive.

This work is a step towards studying the proposed topology and it provides a baseline for future analyses of the architecture and its possible improvements.

2 Introduction

2.1 Background

The smart grid (SG) is the new generation intelligent electricity network which optimizes the energy efficiency through exchanges real-time information between electric suppliers and customers. Two keys technologies fundamental in smart grids are the wide use of distributed renewable energy generators and the power conversion systems, needed by first one in order to rapidly and effectively adapt the values of voltage, current, power, and energy according to the requests.

Moreover, the wide use of such distributed systems requires the application of energy flow balancing techniques for end-user customers with high quality, stability and reliability. In this case, power electronic converters represent the power interfaces and such interconnection causes the electric grid to become the "load side" of the converter. The main role of the power converters in SG is even more evident if the fluctuating nature of the Renewable Energy Systems (RES) is considered, making it necessary the utilization of the energy storage units.

Majority part of renewable energy sources produce direct current (DC) electricity in the output, such as photovoltaic panels (PV) and Fuel Cells (FC). To use the produced DC energy in various kind of loads (AC and/or DC), the DC/DC and/or DC/AC converters should be utilized to adopt the unregulated DC voltage to the regulated and usable one. On the other hand, to connect this kind of renewable energies to the utility grid, DC/AC converters must be used.

In order to connect RES to electric grid, a high power ($> 100\,kW$); and high voltage converter is preferred because of their higher efficiency and because their use become economically convenient only above a certain amount of power.

Multilevel converters (MC) are converters that use more than two voltage levels in order to produce a staircase AC output waveform. They are suitable for applications which require high output voltage, low output harmonic distortion, high efficiency, and high volt-ampere ratings. Moreover, the diversity of voltage levels of renewable energy sources in distributed system makes multilevel inverters an interesting and innovative choice as the proper solution for interconnection of distributed energy sources and for the improvement of power quality and reliability. Thus, the MC topology is being exploited to replace the two-level VSI [3]. The salient features of this topology include:

1. Modularity and scalability, to fulfill high-voltage level requirements.

2. Feasibility of the direct connection to high-voltage networks without using transformers and therefore a reducing system size, cost, losses and footprint.
3. Superior harmonics performance, due to the high-level of the output voltage waveform, in which a large number of submodules with low rating switches are used, thereby allowing a significant reduction in the filtering requirement.
4. A huge number of degrees of freedom in terms of switching patterns and DC supply levels which allow the implementation of advanced modulation technique to increase the performances of the converter.
5. Low expense for fault tolerant operation due to utilization of standard, low voltage components, such as 600V-1200V IGBT even in high voltage applications.

There are four main multilevel topologies, which are deeply described in chapter 3: flying capacitor converter (FCC), neutral point clamped (NPC) converter, cascaded H-bridge converter (CHB), and the modular multilevel converter (MMC):

- The flying capacitor converter, uses capacitors to subdivide the output voltage of the converter, which allows multiple voltage levels to be produced.
- The NPC converter, utilizes diodes to produce a multilevel output voltage. To create additional voltage levels, the dc bus capacitor would consist of a string of capacitors with clamping diodes connected at regular intervals.
- The cascaded H-bridge converter is the multilevel topology that has, thus far, garnered the most interest for applications to renewable resources and electric drives. It is composed by a number of elemental H-bridge inverters N_{inv}, connected in series, that generates a number of voltage levels of the phase voltage L_{ph} equal to $L_{ph} = 2N_{inv} + 1$.
- The MMC was originally developed for medium and high voltage dc transmission and distribution applications. The MMC, consists of three phase legs, each with an upper and lower phase arm. A phase arm is composed of a series of submodules and a small inductor. The inductors are used to limit the rate of change of current during switching transitions in the phase arms and to provide filtering of both ac and dc output currents. The composition of the submodules may vary, but the most common submodule consists of a half-bridge converter.

Several renewable energy sources (batteries, fuel cells, solar cells, wind turbines or micro turbines) can be easily connected through a multilevel inverter to feed a load (off-grid) or interconnect to the ac grid (grid-connected) without voltage balancing problems. Moreover, multilevel inverters can have a lower switching frequency than standard Pulse Width Modulation (PWM) inverters and thus have reduced switching losses. Since the output waveforms of multilevel inverters are in a stepped form, resulting in reduced harmonics compared to a square-wave inverter, hence the the output filter size is reduced and the efficiency is high. Also, the voltage stress on the

power electronic switches such as power MOSFETs and/or IGBTs are less in such converters which makes it suitable in medium/high voltage applications.

Furthermore, the interest for multilevel converters in the recent year is exponentially growing also in high power motor drives, electric cars charging stations and in utility for high power applications such as Static Synchronous Compensator (STATCOM) to compensate the grid reactive power.

Multilevel converter topologies are also found suitable for PV applications since, due to the modular structure of PV arrays, different DC voltage levels can easily be provided. Such power converters should have a high reliability, high efficiency, good harmonic performance, low cost, and a small footprint.

Even if the advantages of the multilevel technology are obvious in high power fields, their presence on the market is still lacking. However, in recent years, especially because of the leap forward on the automotive business, also the world leaders in the power electronic field are moving their first steps towards the multilevel technologies.

2.2 Outline of Thesis

This dissertation is divided into nine chapters and is structured in four sections:

- **Part 1:** the first section presents an overview of the literature knowledge regards the multilevel converters. It particular:
  - chapter 3 presents the state of art of the multilevel converters topologies.
  - chapter 4 addresses the state of art of the multilevel modulation techniques.
- **Part 2:** In chapter 5 are presented some innovative modulation techniques which have been developed during my PhD studies. Also several experimental results and comparisons have been performed and are shown in this chapter.
- **Part 3:** The third part deals with the hardware design of an FPGA-CPLD-DSP based control board used to control the multilevel converter prototypes. All the functionalities of the control board have been described and analyzed.
- **Part 4:** The last section of this thesis presents the initial results obtained in two different applications fields:
  - A D-STATCOM application for the power grid stabilization.
  - A high power asynchronous motor drive application.
- **Part 5:** Finally, conclusions and the suggestions for future work are included in chapter 9.

2.3 Related Publications

All the publications and the activities related to the presented work are listed below:

1. C. Buccella, M. G. Cimoroni, M. Tinari and C. Cecati, "A New Pulse Active Width Modulation for Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7221-7229, Aug. 2019.
2. C. Buccella, M. G. Cimoroni, V. Patel, M. Tinari and C. Cecati, "Investigation about SHM-PAM procedure for grid connected CHB seven level inverters," 2019 International Conference on Clean Electrical Power (ICCEP), Otranto, Italy, 2019, pp. 413-418..
3. V. Patel, M. Tinari, C. Buccella and C. Cecati, "Analysis on Multilevel Inverter Powertrains for E-transportation," 2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Sonderborg, Denmark, 2019, pp. 1-6.
4. A.M. Saif, C. Buccella, V. Patel, M. Tinari and C. Cecati, "Design and Cost Analysis for STATCOM in Low and Medium Voltage Systems," IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, 2018, pp. 3938-3943.
5. C. Buccella, M. G. Cimoroni, V. Patel, A.M. Saif, M. Tinari, C. Cecati, E. Babaei, "Harmonic elimination procedure for cascaded multilevel inverters having a particular even number of dc sources," IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, 2018, pp. 1249-1254.
6. A. Raciti, A. Rizzo, N. Salerno, G. Susinni, C. Buccella, C. Cecati, M. Tinari "State of the art and emerging solid-state power devices in the perspective of more electric aircraft," 2018 AEIT International Annual Conference, Bari, 2018, pp. 1-6.
7. C. Buccella, M. G. Cimoroni , M. Tinari, C. Cecati, S. A. Rizzo, G. Susinnii, A. Raciti, "Single-Phase Chebyshev Algorithm for Harmonics Mitigation in CHB Five-Level Inverters," 2018 AEIT International Annual Conference, Bari, 2018, pp. 1-5.
8. V. Patel, C. Buccella, A. M. Saif, M. Tinari and C. Cecati, "Performance Comparison of Multilevel Inverters for E-transportation," 2018 International Conference of Electrical and Electronic Technologies for Automotive, Milan, 2018, pp. 1-6.
9. M. G. Cimoroni, M. Tinari, C. Buccella and C. Cecati, "A high efficiency Selective Harmonic Elimination technique for multilevel converters," 2018 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Amalfi, 2018, pp. 673-677.

10. C. Buccella, M. G. Cimoroni, H. Latafat, M. Tinari and C. Cecati, "Mixed harmonic elimination and reduction technique for single phase nine level converters," 2017 IEEE 26th International Symposium on Industrial Electronics (ISIE), Edinburgh, 2017, pp. 756-761.

3 State of Art: Multilevel Converter (MLC) Structures

3.1 Overview

With the diffusion of renewable energy systems, high power quality of power converters is fundamental for their successful integration within the grid. Therefore, the achievement of strict specifications imposed on harmonics content in order to fulfill grid code limits became one of the most demanding design issue, which can be accomplished only by suitable synthesis of modulation signals [4]. Multilevel Inverters (MLI) operating at frequency close to fundamental are nowadays considered leading topology for achieving such results, due to their capability to produce voltage waveforms with relatively low harmonic content even with reduced output passive filters. In particular, they appear very attractive in high power applications, in which low switching frequency operations are necessary to ensure that intrinsic losses in electronic devices do not affect converter operations and efficiency. Multilevel Converters (MLC) receive wide acceptance in industry and energy systems because they enable the design of medium and high voltage systems with excellent output voltage quality. Compared to the two-level voltage source converter, the simple realization of redundancy, low filter expense, and the reduction of power semiconductor losses and common mode voltages are important additional benefits [5].

The number of levels of an inverter, is the number of steps in the voltage of the output terminal with respect to any arbitrary internal reference point. One phase leg of a two-level inverter is shown in Fig. 3.1. The conduction states of the power switches (IGBT) determine the output voltage (v_{aN}) status. To avoid any short circuit in the phase leg, the switches must not be On simultaneously.

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 3.2 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. As shown in this figure, a two-level inverter generates an output voltage with two values (levels) with respect

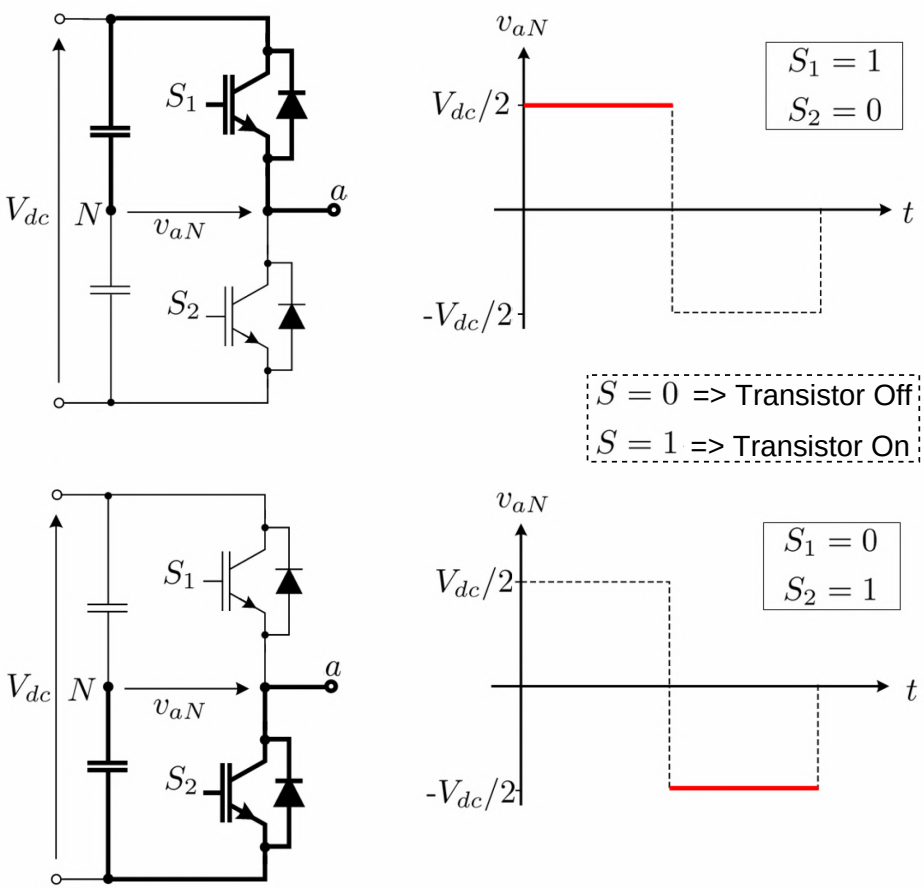


Figure 3.1: One phase leg of a two-level inverter and its output voltage [6].

to the negative terminal N, while the three-level inverter generates three voltages, and so on.

The first multilevel (three-level) inverter introduced by Nabae *et al.* [7] in 1981. By increasing the number of levels in the inverter, more steps can be achieved in the output voltages generating a staircase waveform, which results a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces capacitor voltage unbalance problems. Four successful different topologies have been proposed for multilevel inverters: diode-clamped (neutral point clamped) [7]; capacitor-clamped (flying capacitors) [8, 9, 10]; cascaded multicell (cascaded H-bridge) with separate dc sources [8, 11, 12]; and Modular Multilevel Converters (MMC) [13]-[16]. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM). The most attractive features of multilevel inverters are as follows.

1. They can generate output voltages with extremely low distortion and lower d_v/d_t.

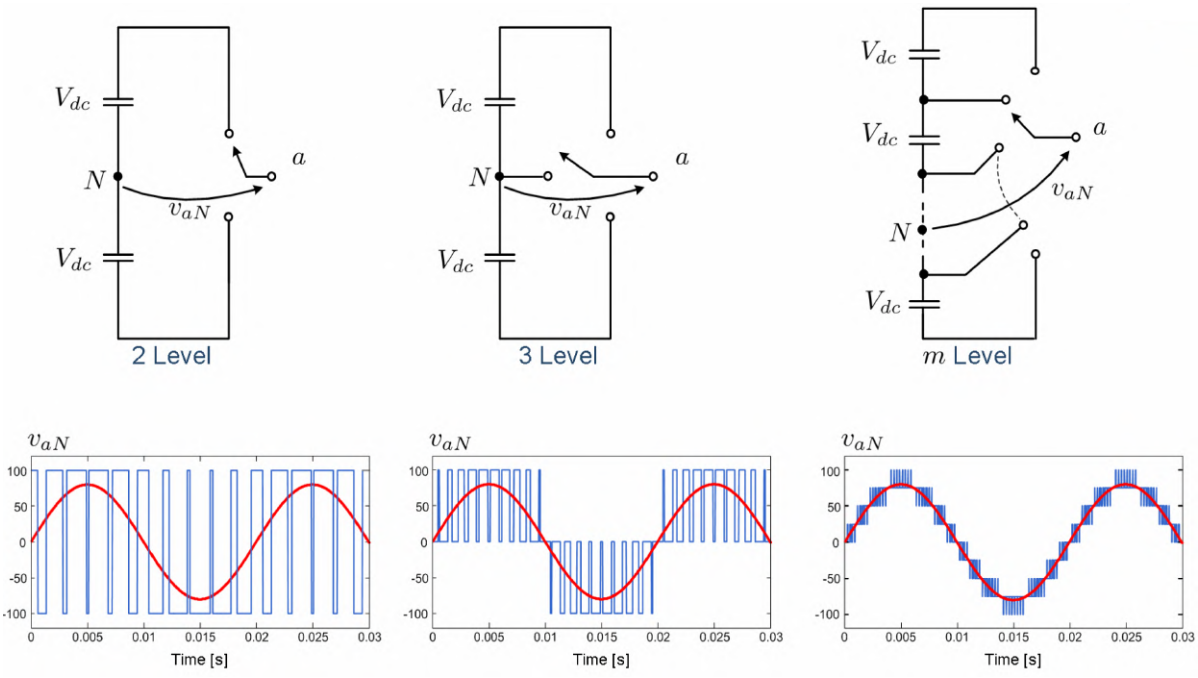


Figure 3.2: Schematic diagram of one phase leg of MLI for two, three and m levels [6].

2. They draw input current with very low distortion.
3. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated [12].
4. They can operate with a lower switching frequency.

Currently, three-level neutral point clamped (NPC) or flying capacitor (FC) converters seem preferred due to their cost, but Cascaded H-Bridges (CHB) are gaining interest and applications, due to their superior characteristics and simple modular structure. Therefore, as discussed in [17, 18], many researchers are addressing their attention to this topology. Both traditional NPC and FC multilevel inverters have a practical limit on the number of levels, because the number of respectively required clamping diodes and capacitors in both topologies becomes excessive when the number of levels is high [19].

Among multilevel inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology. Cascaded multilevel inverters are based on a series connection of several single-phase inverters. This structure is capable of reaching medium output voltage levels using only standard low-voltage mature technology components. Typically, it is necessary to connect three to ten inverters in series to reach the required output voltage. These converters also feature a high modularity degree because each inverter can be seen as a module with similar circuit topology,

control structure, and modulation [17]. The MMC is an advanced type of series cascaded converters in which half-bridge DC/DC modules with floating capacitor are used as a core module. This converter has a common DC link which makes this topology more useful in HVDC application. But capacitors voltage unbalance problem was also reported in literature for the MMC [20]-[24], [46, 47].

The CHB converter utilizes H-bridge AC/DC modules with separate dc links (capacitors), so its control and modulation is more simpler. The output voltage characteristics of CHB are intrinsically better in two level converters, but further enhancements can be achieved using specific modulation algorithms based on analytical, numerical or optimization methods and capable of harmonic elimination or mitigation [162, 177, 178, 195].

The application of the NPC inverter and its extension to multilevel converter was found in [25]. Although the cascade inverter was invented earlier, its applications did not prevail until the mid–1990s. Two major patents [26, 27] were filed to indicate the superiority of cascade inverters for motor drive and utility applications. Due to the great demand of medium-voltage high-power inverters, the cascade inverter has drawn tremendous interest ever since. Several patents were found for the use of cascade inverters in regenerative-type motor drive applications [28]–[30]. The last entry for U.S. multilevel inverter patents, which were defined as the capacitor-clamped multilevel inverters, came in the 1990s [31, 32]. Today, multilevel inverters are extensively used in high-power applications with medium voltage levels. The field applications include use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

In this chapter sec. 3.2, sec. 3.3, sec. 3.4 and sec. 3.5 present diode-clamped, capacitor-clamped, cascaded H-bridge and MMC multilevel structures, respectively. In **??** some other introduced topologies for multilevel converters are presented in brief. Finally, sec. 3.6 presents the summary of this chapter.

3.2 Diode-Clamped (Neutral Point Clamped) MLC

The diode-clamped inverter was also called the neutral-point clamped (NPC) inverter when it was first used in a three-level inverter in which the mid-voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s.

3.2.1 The Main Structure and Conduction States

A m-level diode-clamped inverter has $m-1$ capacitors in dc bus and produces m levels in output voltage. A three-level NPC is shown in Fig. 3.3. In this circuit,

the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors N can be defined as the neutral point. The output voltage v_{aN} has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S_3 and S_4 need to be turned on; and for the 0 level, S_2 and S_3 need to be turned on, as shown in Fig. 3.3a, Fig. 3.3c and Fig. 3.3b, respectively.

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and D_2. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both S_1 and S_2 turn on, the voltage across S_3 and S_4 (across a and the emitter of S_4) is V_{dc}. In this case, balances out the voltage sharing between S_3 and S_4 with S_3 blocking the voltage across C_1 and S_4 blocking the voltage across C_2.

Fig. 3.4 shows a five-level NPC converter in which the dc bus consists of four capacitors, C_1, C_2, C_3, and C_4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/2$ through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point N is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across a and N.

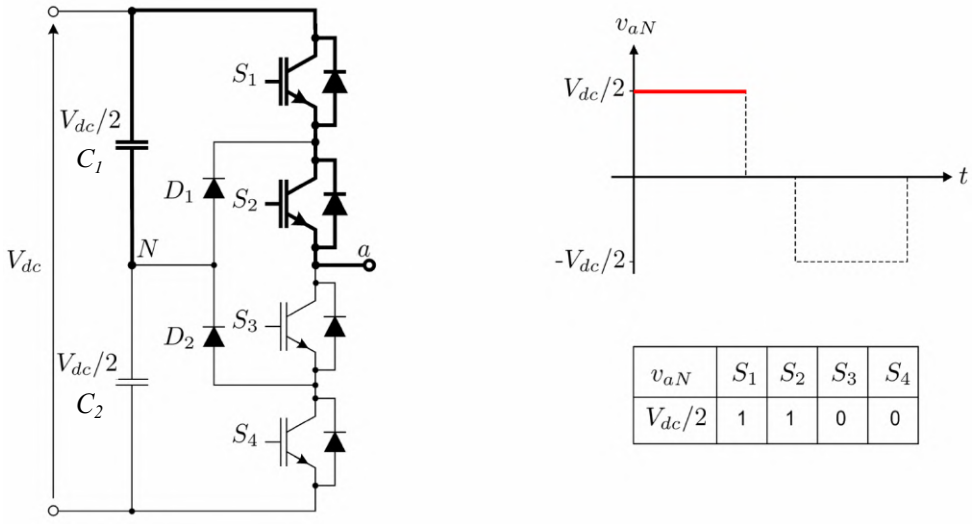
1. For voltage level $v_{aN} = V_{dc}/2$, turn on all upper switches S_1–S_4 .
2. For voltage level $v_{aN} = V_{dc}/4$, turn on three upper switches S_2–S_4 and one lower switch $\bar{S}_1$.
3. For voltage level $v_{aN} = 0$, turn on two upper switches S_3 and S_4 and two lower switches $\bar{S}_1$ and $\bar{S}_2$.
4. For voltage level $v_{aN} = -V_{dc}/4$, turn on one upper switch S_4 and three lower switches $\bar{S}_1$–$\bar{S}_3$.
5. For voltage level $v_{aN} = -V_{dc}/4$, turn on all lower switches $\bar{S}_1$–$\bar{S}_4$.

Generated voltage levels and the corresponding conduction states of the switches are given in Tab. 3.1. In this table, the state 1 means the corresponding switch is On, and state 0 means the corresponding switch is Off. It should be noticed that, each switch commutes only one time in each cycle.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are $\left(S_1, \bar{S}_1\right)$, $\left(S_2, \bar{S}_2\right)$, $\left(S_3, \bar{S}_3\right)$, and $\left(S_4, \bar{S}_4\right)$.

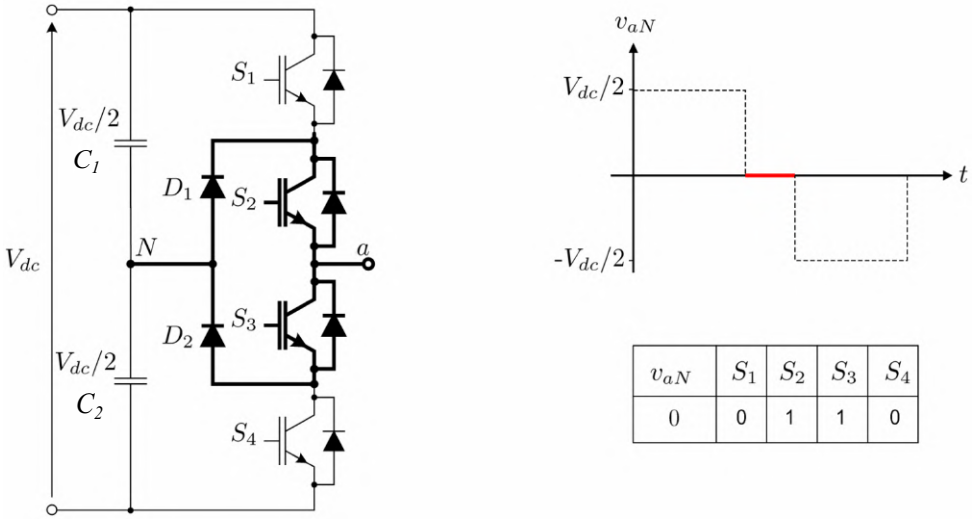
3.2.2 Characteristics of The NPC multilevel inverters

- **To block the clamping diodes, high voltage ratings is needed:** Although each active switching device is only required to block a voltage level of



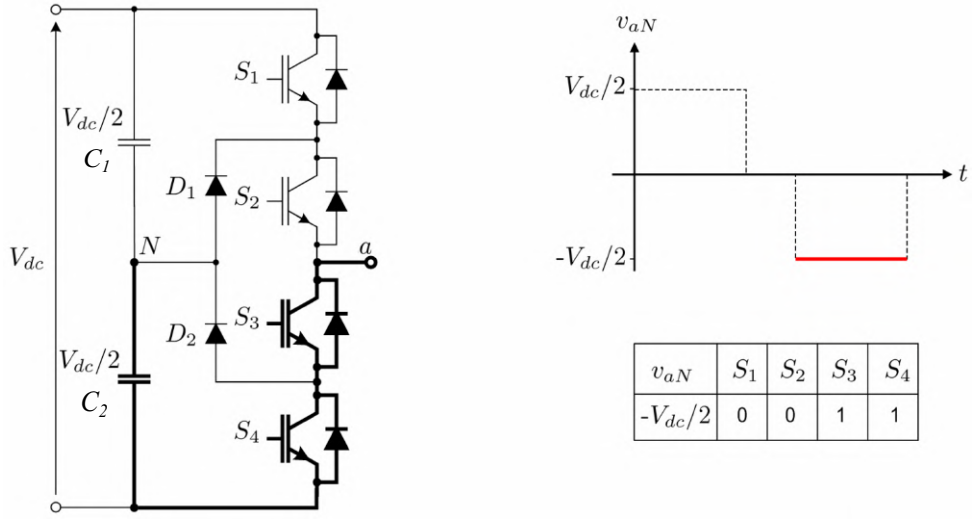
v_{aN}	S_1	S_2	S_3	S_4
$V_{dc}/2$	1	1	0	0

(a) Generating of a positive in output voltage v_{aN}



v_{aN}	S_1	S_2	S_3	S_4
0	0	1	1	0

(b) Generating of a zero in output voltage v_{aN}



v_{aN}	S_1	S_2	S_3	S_4
$-V_{dc}/2$	0	0	1	1

(c) Generating of a negative in output voltage v_{aN}

Figure 3.3: One phase leg of a three-level NPC with conduction states [6].

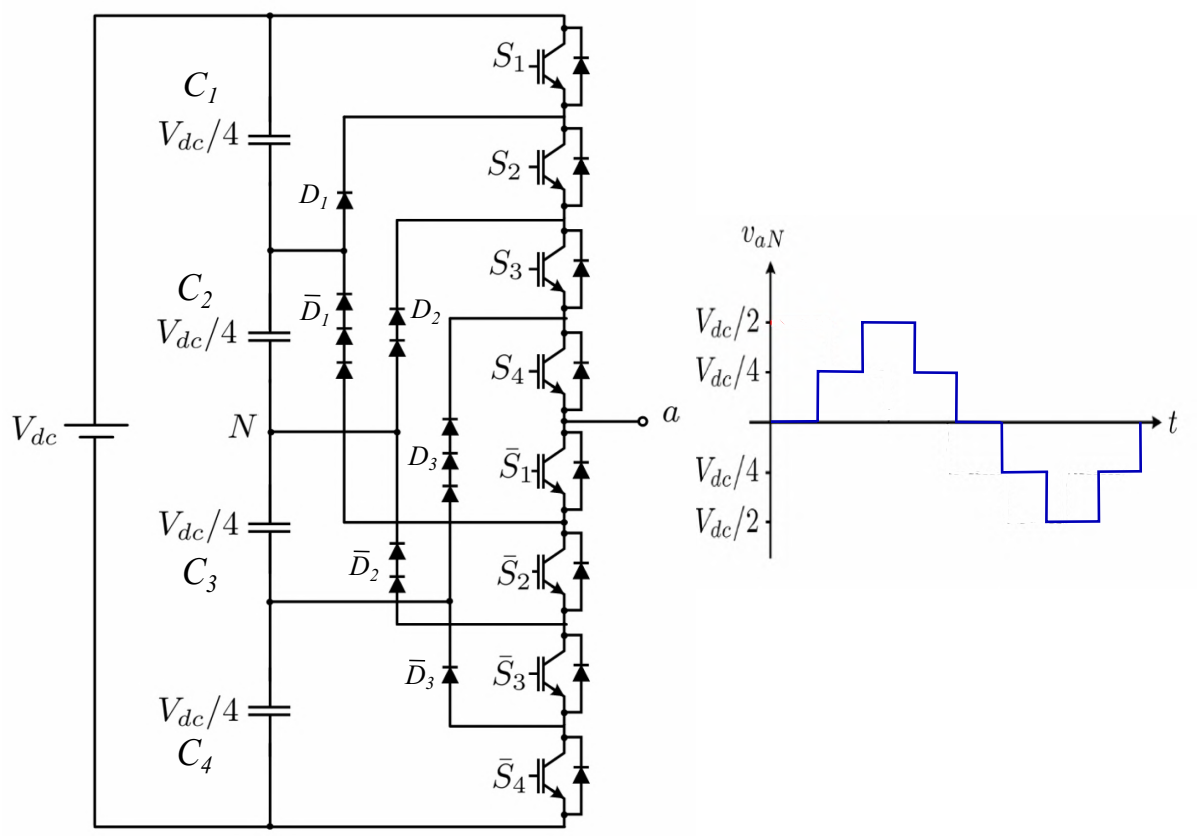


Figure 3.4: One phase leg of a five-level NPC and its output voltage [6].

$V_{dc}/(m-1)$, in which m is number of the levels of the multilevel inverter, the clamping diodes must have different voltage ratings for reverse voltage blocking. For example, by considering $\bar{D}_1$ of Fig. 3.4, when lower devices $\bar{S}_2$–$\bar{S}_4$ are turned on, $\bar{D}_1$ needs to block three capacitor voltages, or $3V_{dc}/4$. Similarly, D_2 and $\bar{D}_2$ need to block $2V_{dc}/4$, and D_3 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be $(m-1)\times(m-2)$. This number represents a quadratic increase in . When is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.

- **Unequal ratings of active switching devices:** As shown from Tab. 3.1, S_1 only conducts in $v_{aN} = V_{dc}/2$, whereas S_4 conducts in all of the cycle except in $v_{aN} = -V_{dc}/2$. Such unequal conduction cycle needs the switching devices with different current and power ratings. The outer switches may be over sized, while the average conduction of the switching devices are used for inverter designing, and the ratings of the inner switches may be under sized.

Table 3.1: Voltage levels and the corresponding conduction states in the 5-level NPC.

Voltage level (v_{aN})	Switches conduction states							
	S_1	S_2	S_3	S_4	$\bar{S}_1$	$\bar{S}_2$	$\bar{S}_3$	$\bar{S}_4$
$v_{aN} = V_{dc}/2$	1	1	1	1	0	0	0	0
$v_{aN} = V_{dc}/4$	0	1	1	1	1	0	0	0
$v_{aN} = 0$	0	0	1	1	1	1	0	0
$v_{aN} = -V_{dc}/4$	0	0	0	1	1	1	1	0
$v_{aN} = -V_{dc}/2$	0	0	0	0	1	1	1	1

This unequal condition would be an advantage in conventional transformer coupled multi-pulse converters with 6-pulse operation of each converter.

- **Capacitors unbalance problem:** In the most applications of power converters, active power transfer from ac side to dc (rectifier operation) and vice versa (inverter operation) is essential. When the NPC converter works with unity power factor, charging time for rectifying operation (inverter mode charging time) is different for each capacitor. This capacitor charging profile occurs in each cycle and results in capacitors voltage unbalance. For the diode-clamped multilevel inverter with a number of levels (m) greater than three (i.e., $m > 3$), each voltage level can be balanced only when used for var compensation [33]. For motor drives that involve real power transfer, the diode-clamped multilevel inverter require either isolated dc power sources, an additional voltage balancing circuit [34], or a back-to-back system with each voltage level connected back-to-back and voltage balancing control [35, 36]. In [37], dc capacitor voltage equalization control schemes of a five-level diode-clamped multilevel inverter-based DSTATCOM are presented with the dc–dc converter circuit for equalization.

3.3 Capacitor-Clamped (Flying Capacitor) MLC

Fig. 3.5 illustrates the fundamental building block of a phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor (FC) inverter [8, 10] with independent capacitors clamping the device voltage to one capacitor voltage level. As shown in this figure, flying capacitor inverter has a modular topology and also called the multicell converter. Each cell is composed by 2 switches and 1 capacitor. additional cells can be connected in series to increase the number of output levels of the inverter. The switches of each cell are complementary controlled (e.g.: $S_1 = \bar{S}_4$).

The inverter in Fig. 3.5 provides a three-level output across a and N, i.e., $v_{aN} = V_{dc}/2$, 0, or $v_{aN} = -V_{dc}/2$. One phase-leg of a three-level FC inverter and conduction states of switches corresponding to each voltage level in the output are shown in

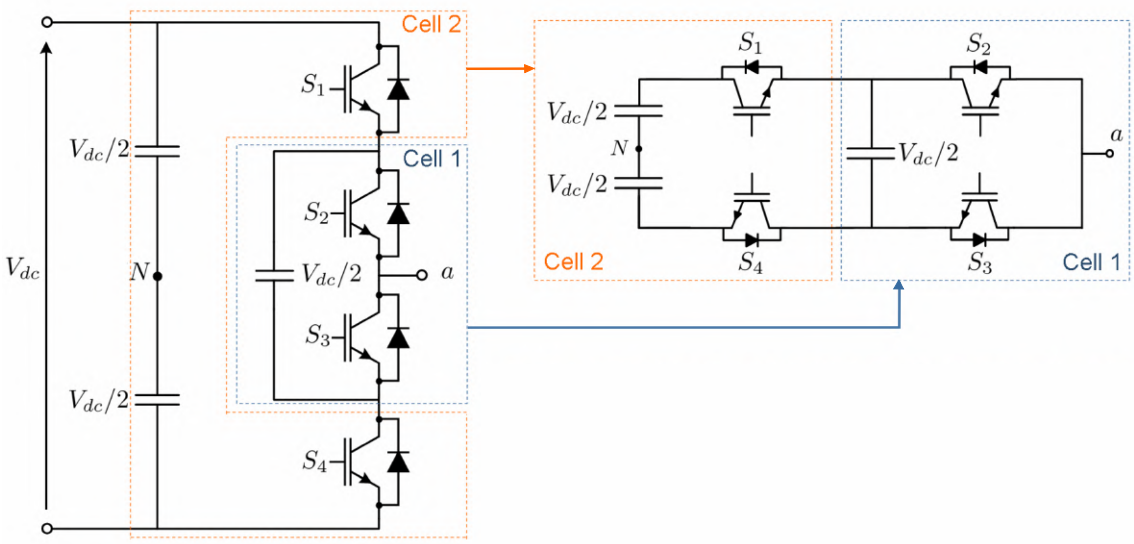
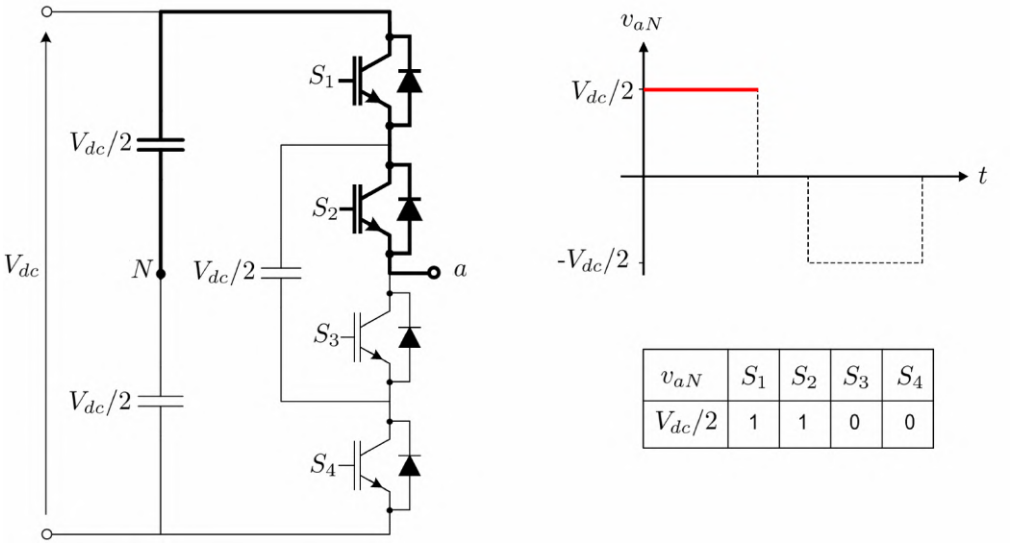


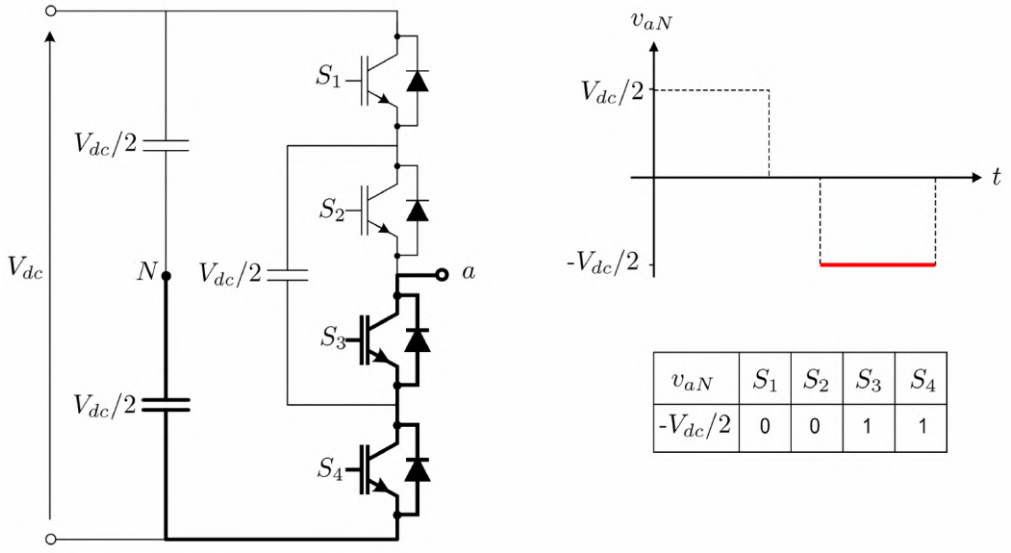
Figure 3.5: The fundamental building block of one phase-leg of a three-level FC inverter [6].

Fig. 3.6 and Fig. 3.7. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S_3 and S_4 need to be turned on; and for the 0 level, either pair (S_1, S_3) or (S_2, S_4) needs to be turned on. There are two possibilities for generating 0-level in the output, this property is called inverter output redundancy. Regarding to Fig. 3.7 and considering $i_a > 0$, clamping capacitor C_3 is charged (increase the voltage) and dc-bus capacitor C_1 is discharged (reduce the voltage) when S_1 and S_3 are turned on, and C_3 is discharged and C_2 is charged when S_2 and S_4 are turned on. The opposite charging status are occurred with the same switching condition when $i_a < 0$. The charge of C_1, C_2 and C_3 can be balanced by proper selection of the 0-level switch combination.



v_{aN}	S_1	S_2	S_3	S_4
$V_{dc}/2$	1	1	0	0

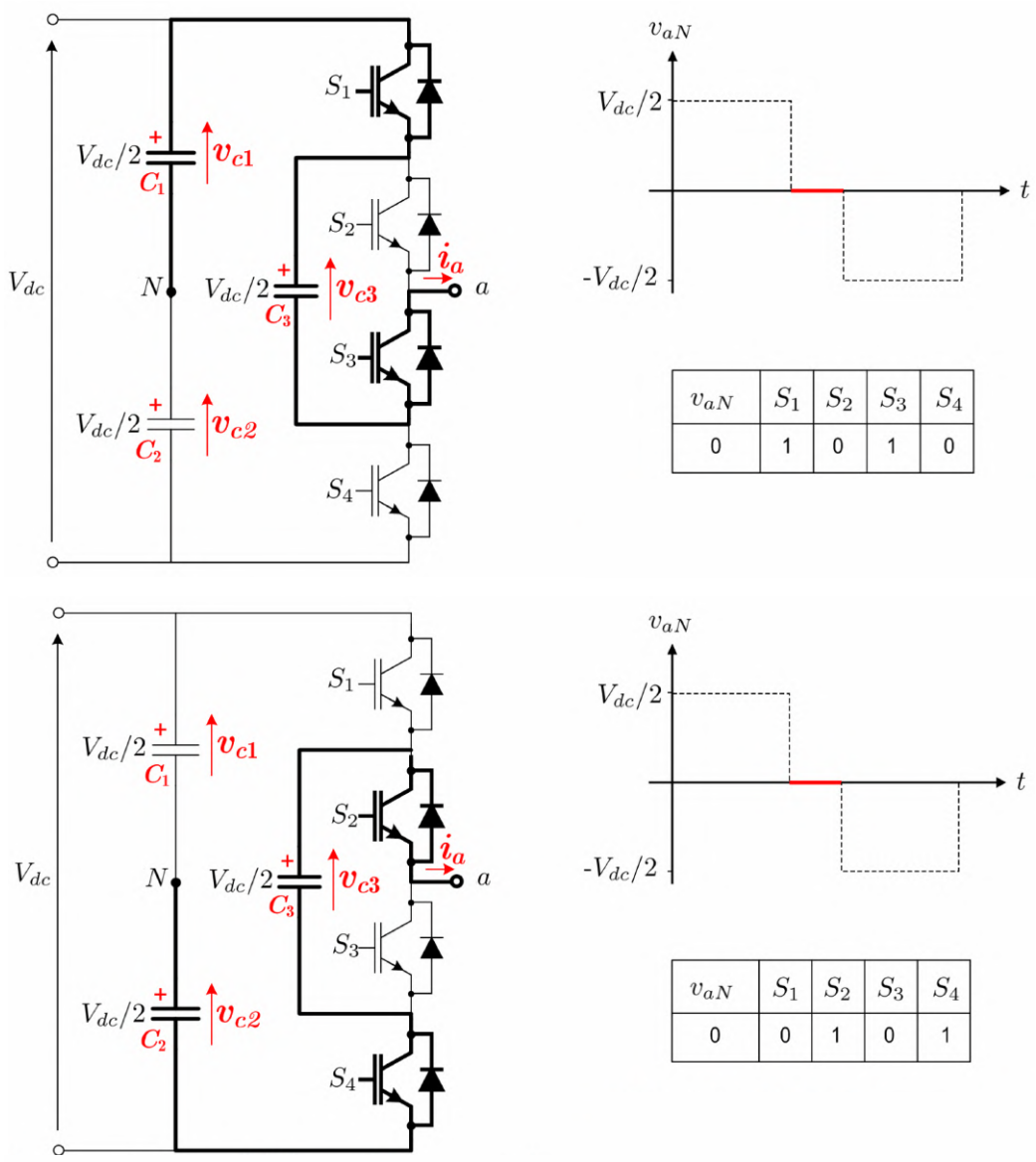
(a) Generating of a positive in output voltage v_{aN}



v_{aN}	S_1	S_2	S_3	S_4
$-V_{dc}/2$	0	0	1	1

(b) Generating of a negative in output voltage v_{aN}

Figure 3.6: One phase-leg of a three-level FC inverter and conduction states[6].



v_{aN}	S_1	S_2	S_3	S_4
0	1	0	1	0

v_{aN}	S_1	S_2	S_3	S_4
0	0	1	0	1

Figure 3.7: Generating of a zero level in FC inverter output voltage v_{aN} and conduction states [6].

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 3.8 as the example, the voltage of the five-level phase-leg a output with respect to the neutral point N, v_{aN} , can be synthesized by the following switch combinations.

1. For voltage level $v_{aN} = V_{dc}/2$, turn on all upper switches $S_1 - S_4$.
2. For voltage level $v_{aN} = V_{dc}/4$, there are three combinations:

a) S_1, S_2, S_3, S_1' ($v_{aN} = V_{dc}/2$ of upper C_4's $-V_{dc}/4$ of C_1);

b) S_2, S_3, S_4, S_4' ($v_{aN} = 3V_{dc}/4$ of C_3's $-V_{dc}/2$ of lower C_4's); and

c) S_1, S_3, S_4, S_3' ($v_{aN} = V_{dc}/2$ of upper C_4's $-3V_{dc}/4$ of C_3's $+V_{dc}/2$ of C_2's).

3. For voltage level $v_{aN} = 0$, there are six combinations:

a) S_1, S_2, S_1', S_2' ($v_{aN} = V_{dc}/2$ of upper C_4's $-V_{dc}/2$ of C_2's);

b) S_3, S_4, S_3', S_4' ($v_{aN} = V_{dc}/2$ of C_2's $-V_{dc}/2$ of lower C_4);

c) S_1, S_3, S_1', S_3' ($v_{aN} = V_{dc}/2$ of upper C_4's $-3V_{dc}/4$ of C_3's $+V_{dc}/2$ of C_2's $-V_{dc}/4$ of C_1);

d) S_1, S_4, S_2', S_3' ($v_{aN} = V_{dc}/2$ of upper C_4's $-3V_{dc}/4$ of C_3's $+V_{dc}/4$ of C_1);

e) S_2, S_4, S_2', S_4' ($v_{aN} = 3V_{dc}/4$ of C_3's $-V_{dc}/2$ of C_2's $+V_{dc}/4$ of C_1 $-V_{dc}/2$ of lower C_4's); and

f) S_2, S_3, S_1', S_4' ($v_{aN} = 3V_{dc}/4$ of C_3's $-V_{dc}/4$ of C_1 $-V_{dc}/2$ of lower C_4's).

4. For voltage level $v_{aN} = -V_{dc}/4$, there are three combinations:

a) S_1, S_1', S_2', S_3' ($v_{aN} = V_{dc}/2$ of upper C_4's $-3V_{dc}/4$ of C_3's);

b) S_4, S_2', S_3', S_4' ($v_{aN} = V_{dc}/4$ of C_1 $-V_{dc}/2$ of lower C_4's); and

c) S_3, S_1', S_3', S_4' ($v_{aN} = V_{dc}/2$ of C_2's $-V_{dc}/4$ of C_1 $-V_{dc}/2$ of lower C_4's).

5. For voltage level $v_{aN} = -V_{dc}/2$, turn on all lower switches, $S_1' - S_4'$.

In the preceding description, the capacitors with positive signs are in discharging mode, while those with negative sign are in charging mode. By proper selection of capacitor combinations, it is possible to balance the capacitor charge. Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level converter will require a total of $(m-1) \times (m-2)\,/2$ clamping capacitors per phase-leg in addition to $(m-1)$ main dc-bus capacitors.

Tab. 3.2 shows the corresponding conduction states of the switches for each voltage levels in a Five-level capacitor-clamped multilevel inverter.

3.4 Cascaded H-Bridge (CHB) MLC

A different converter topology is introduced here, which is based on the series connection of single-phase inverters with separate dc sources [11]. The basic building block (cell) of the cascaded multilevel inverter is a single-phase full-bridge (H-bridge)

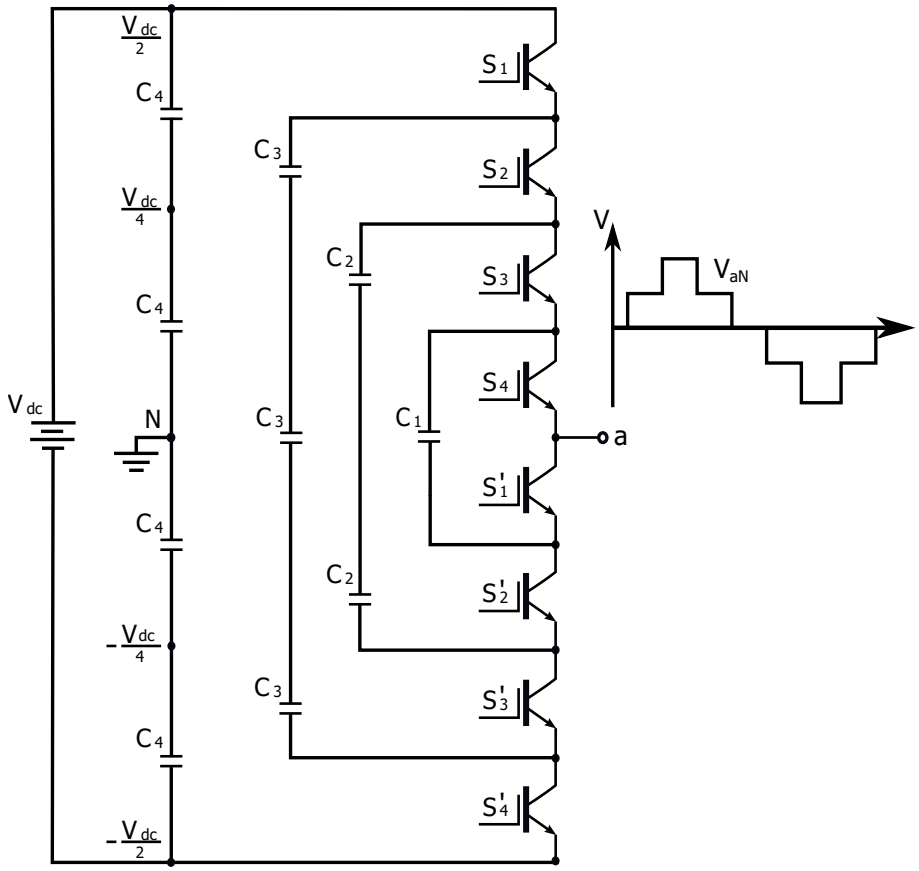


Figure 3.8: Five-level capacitor-clamped multilevel inverter circuit topology.

inverter which is shown in Fig. 3.9, and generates three voltages at the output: $+V_{dc}$, 0, and $-V_{dc}$. This is made possible by connecting the capacitors sequentially to the ac side via the four power switches. There are two possibility to generate 0-level in the output of the inverter.

A basic structure of a cascaded multilevel inverter is shown in Fig. 3.10 for five levels of output voltage. There are two cells in each phase. As mentioned before, each cell (H-bridge inverter) is able to produce three voltage levels at the output: $+V_{dc}$, 0, and $-V_{dc}$. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. The switching states corresponding to different voltage levels are shown in Fig. 3.10a, Fig. 3.10b and Fig. 3.10c. As shown from these figures there are more redundancy possibility in generating a specific voltage level except $-2V_{dc}$ and $+2V_{dc}$. The different voltage levels and the corresponding all possible switching states (redundancy) for a 5-level cascaded inverter are summarized in Tab. 3.3.

Fig. 3.11 shows the power circuit for one phase leg of a nine-level cascaded H-bridge inverter with four H-bridge inverter cells in each phase. Each H-bridge inverter uses a separate dc-link voltage to generate a modulated voltage at the output terminals.

Table 3.2: Voltage levels and the corresponding conduction states in a 5-level FC multilevel inverter.

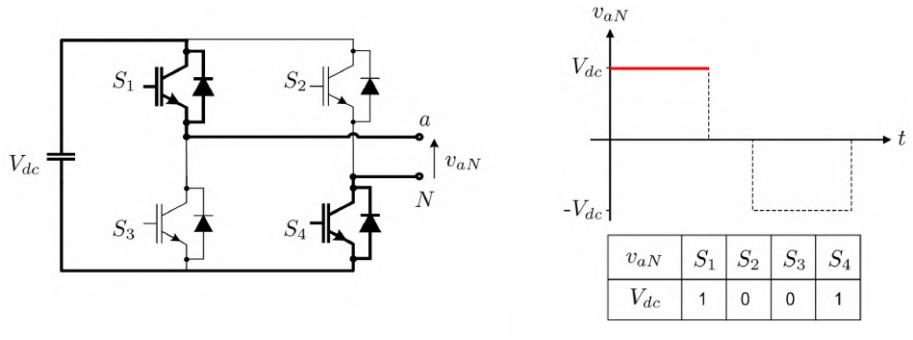
Voltage level (v_{aN})	Switches conduction states							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$v_{aN} = V_{dc}/2$	1	1	1	1	0	0	0	0
$v_{aN} = V_{dc}/4$	1	1	1	0	1	0	0	0
	0	1	1	1	0	0	0	1
	1	0	1	1	0	0	1	0
$v_{aN} = 0$	1	1	0	0	1	1	0	0
	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0
	1	0	0	1	0	1	1	0
	0	1	0	1	0	1	0	1
	0	1	1	0	1	0	0	1
$v_{aN} = -V_{dc}/4$	1	0	0	0	1	1	1	0
	0	0	0	1	0	1	1	1
	0	0	1	0	1	0	1	1
$v_{aN} = -V_{dc}/2$	0	0	0	0	1	1	1	1

The total output voltage is obtained by the sum of each individual output voltage as shown in right side of Fig. 3.11. The resulting output ac voltage swings from $-4V_{dc}$ to $+4V_{dc}$ with nine levels, and the staircase waveform is nearly sinusoidal, even without filtering. The maximum number of voltage levels of the phase voltage L_{ph} is given by:

$$L_{ph} = 2N_{inv} + 1$$

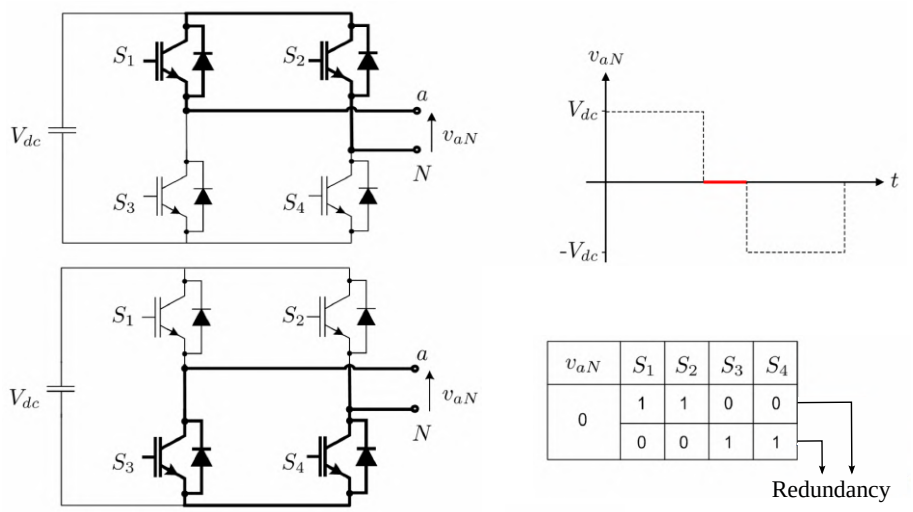
where N_{inv} is the number of H-bridge inverters.

Each inverter requires an isolated dc voltage which is usually obtained by an arrangement of three-phase or single-phase rectifiers [38], as shown in Fig. 3.12 , and a multi-pulse transformer which provides the electrical isolation. In some applications, these dc voltages can be obtained directly by isolated dc sources, for example, photovoltaic panels [39] or DC/DC isolated converters [40]. In another applications, like Static Compensator (STATCOM), which does not require the injection of active power, the dc voltages can be floating, and the control strategy keeps the dc-link voltage adjusted to the reference [41]. A further optimization in terms of input current harmonics can be done when a multi-pulse transformer is used to provide the isolated dc sources. By using a different phase angle for each group of secondaries, i.e., secondaries that fed the inverters of each output phase, it is possible to eliminate characteristic harmonics produced by the diode-based rectifiers [11].



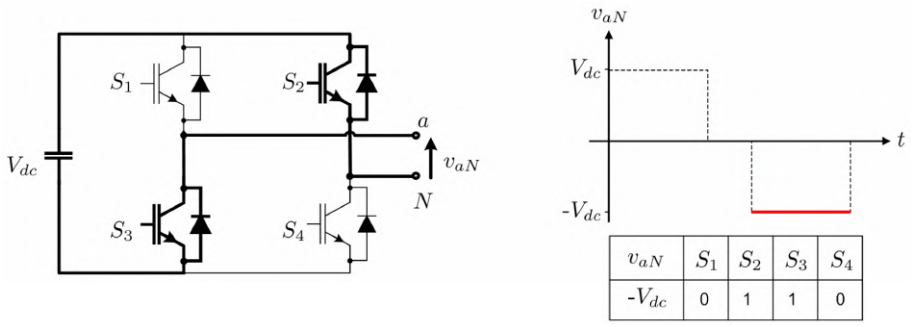
v_{aN}	S_1	S_2	S_3	S_4
V_{dc}	1	0	0	1

(a) Generating of $+V_{dc}$ in output voltage v_{aN} and switching states.



v_{aN}	S_1	S_2	S_3	S_4
0	1	1	0	0
	0	0	1	1

(b) Generating of 0-level in output voltage v_{aN} and switching states.

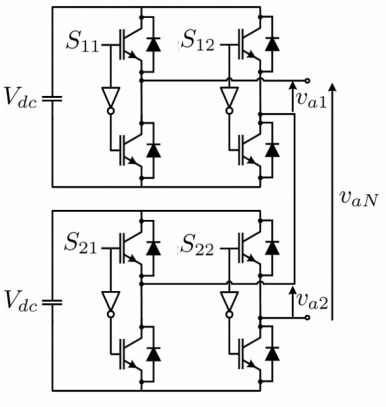


v_{aN}	S_1	S_2	S_3	S_4
$-V_{dc}$	0	1	1	0

(c) Generating of $-V_{dc}$ in output voltage v_{aN} and switching states.

Figure 3.9: H-bridge inverter, the fundamental cell of cascaded multilevel inverter [6].

Table 3.3: Output voltage redundancies in a 5-level cascaded inverter [6].



Total inverter output voltage	Switching state				Individual cell output voltage	
v_{aN}	S_{11}	S_{12}	S_{21}	S_{22}	v_{a1}	v_{a2}
$2V_{dc}$	1	0	1	0	V_{dc}	V_{dc}
V_{dc}	1	0	1	1	V_{dc}	0
			0	0		
	1	1	1	0	0	V_{dc}
	0	0				
0	0	0	0	0	0	0
	0	0	1	1		
	1	1	0	0		
	1	1	1	1		
	1	0	0	1	V_{dc}	$-V_{dc}$
	0	1	1	0	$-V_{dc}$	V_{dc}
$-V_{dc}$	0	1	0	0	$-V_{dc}$	0
			1	1		
	0	0	0	1	0	$-V_{dc}$
	1	1				
$-2V_{dc}$	0	1	0	1	$-V_{dc}$	$-V_{dc}$

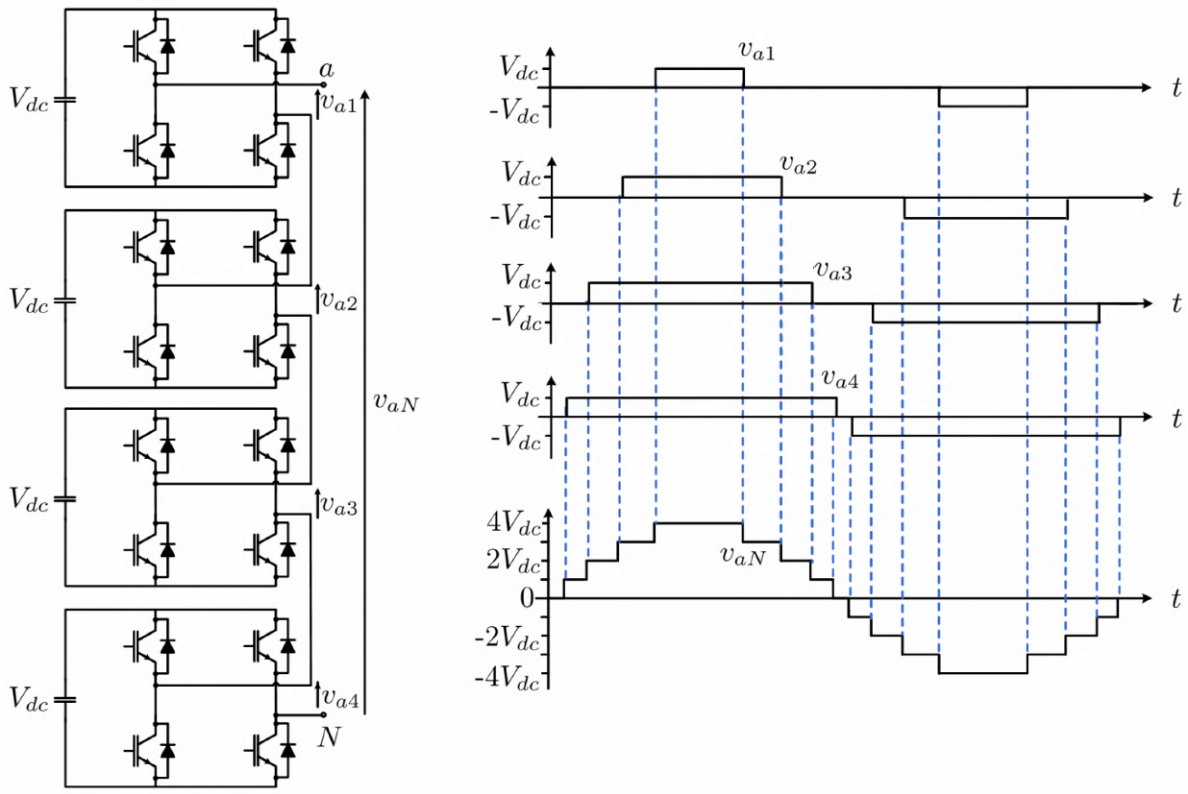


Figure 3.11: Nine-level CHB inverter circuit topology and its output voltage [6].

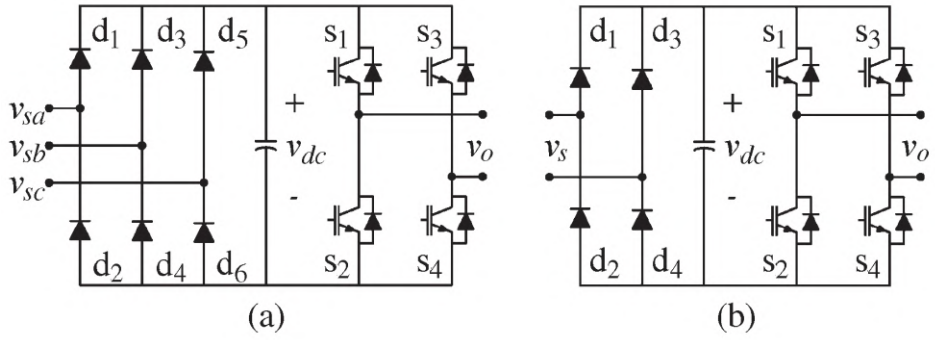


Figure 3.12: Diode-based rectifier power cell topologies. (a) Three-phase. (b) Single-phase.

3.5 Modular Multilevel Converter (MMC)

Another multilevel converter that has recently found industrial applications is the Modular multilevel converters (MMC) (also known as M2C), particularly for HVDC systems [42, 43]. MMCs are a subfamily of multicell converters which have additional features such as the option of a transformerless operation, a completely modular design, and a common DC-bus [16, 44]. The MMC was invented by Prof. R. Marquardt in 2001 [6].This topology was developed in 2001 [45] and received increased attention since then [13, 14, 46]. Three-phase ac–ac and also ac–dc topologies have been proposed. The basic three-phase/dc structure of a nine-level MMC is shown in Fig. 3.13. Each phase leg (also known as MMC valve) is divided into two equal parts: the upper valve or arm and the lower valve or arm. The MMC valves are composed by cells, which is so called sub-module (SM), connected in series. The number of cells must be even in each MMC valve to be able to generate an equal number of positive and negative levels at the ac side. Each sub-module is composed of one capacitor and a bypass switch as shown in Fig. 3.13.

Fig. 3.14 shows the operation of MMC valve and phase output voltage. In this figure all of SMs in upper valve are bypassed and all others in lower valve are activated to generate $+1/2U_d$ in output point AC with respect to the middle of dc-bus voltage U_d.

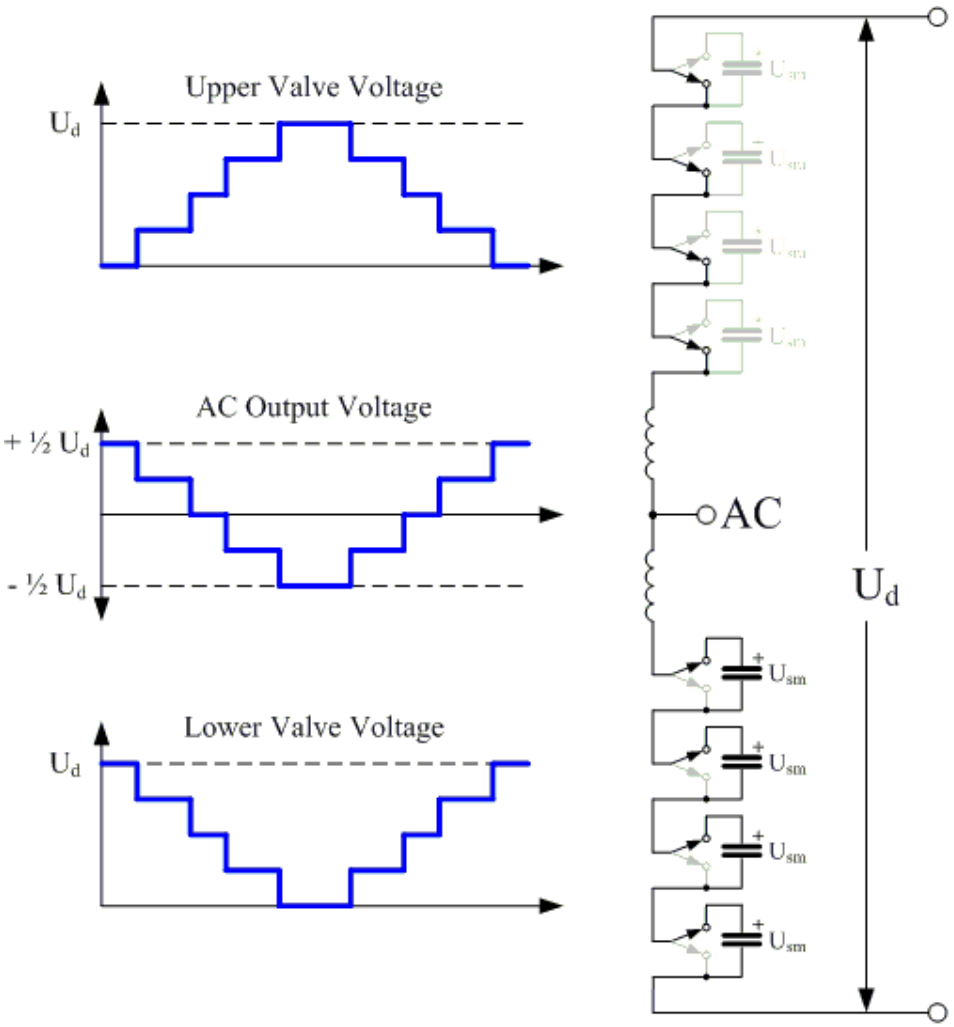


Figure 3.14: The operation of MMC valve and phase output voltage.

Basically, in HVDC applications, the MMC's sub-module is realized by a single-phase two-level voltage source converter leg, which is also known as half-bridges, as shown Fig. 3.15. The switching states of SM is also illustrated in this figure. The two switches of the power cell are controlled with complementary signals and produce two active switching states that can connect or bypass its respective capacitor to the total array of capacitors of the converter leg, generating, in this way, the multilevel waveform. There is a third switching state: both switches off during start-up or failure condition, allowing the current to freely circulate through the diodes (and through capacitors if so demanded by the current polarity).

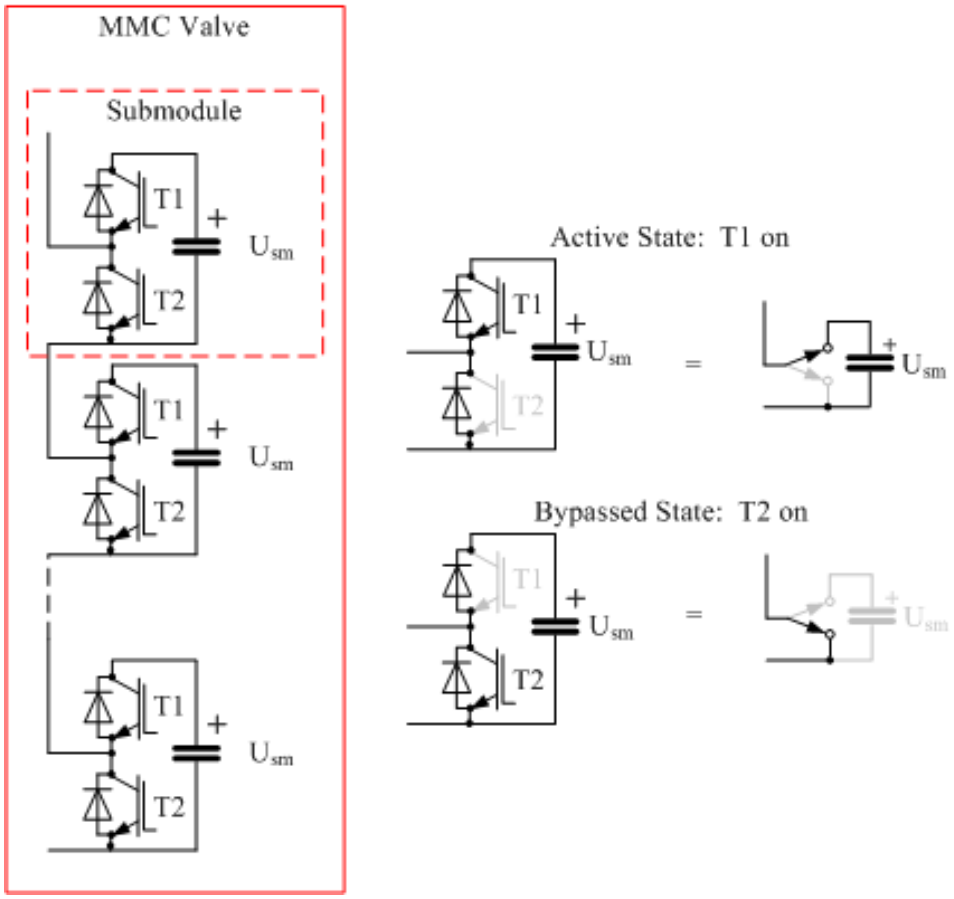


Figure 3.15: The MMC sub-module (SM) circuit diagram and switching states.

Fig. 3.16 shows a three-phase MMC and the corresponding cell circuit diagram which is actually realized for HVDC applications. Some inductors must be included in series within each leg in order to limit the current due to instantaneous voltage differences of the arms. In addition, H-bridge cells have been also proposed [14, 16, 47]. As mentioned before, the two switches of the power cell are controlled with complementary signals. In practical application, there is an additional bypass switch to fully isolate each cell for fault-tolerant operation [42].

Since the capacitors are floating, an appropriate voltage balance control is necessary to keep each one at a constant voltage level [46]. The total dc side will be the sum of all the capacitor voltages in one leg. The attractive feature of this topology is its modularity and scalability to easily reach medium- and high-voltage levels, meanwhile greatly improving ac side power quality, compared to the classic series connection of power switches in a two-level converter configuration used in HVDC. The MMC also has low filter requirements and, in addition, it does not require an input transformer. Moreover, the uneven voltage sharing problem between series-connected devices is solved. In addition, there is no need for high-voltage dc-link capacitors (or series connected) since the intrinsic capacitors of the cells perform

these tasks. The high number of levels enables a great reduction in the device average switching frequency without compromise of power quality. This topology can be found in practical applications reported with 200 power-cell/phase reaching up to 400 MW [42] and is commercialized up to 1 GW [43].

Beside HVDC applications, the MMC's cells can be connected in several configurations to utilize in different applications depending on the interconnection of the arms between the input and output terminals. In this regard, various MMC topologies can be driven: (a) single-phase/single-phase or single-phase/DC, (b) three-phase/single-phase or three-phase/DC, and (c) three-phase/three-phase (back-to-back) [48].

There are several power cell topologies proposed in the literature, the known ones are shown in Fig. 3.17. The most common cells are the full-bridge and half-bridge, of Fig. 3.17(a) and (b), respectively. The half-bridge cells can generate only zero and positive voltages, so there is inevitably a dc component in the arm voltage. This kind of cell thus only be used when the MMC is connected to a dc system. On the other hand, full-bridge cells can generate positive, zero, and negative output voltages, hence, they can be used when the MMC is connected to either ac or dc systems. One of the drawbacks to full-bridge cells is the higher number of components, compared to half-bridge cells. The unidirectional cell, shown in Fig. 3.17(c), has been proposed to reduce the number of semiconductors per cell, but the switching states are restricted depending on the current direction [49]. The efficiency of the cells can be improved, replacing the standard cell by multilevel structures, such as neutral point clamped or flying capacitor [50], as shown in Fig. 3.17(d) and (e), respectively, or by using a twin module [44].

The modularity of the MMC can be also used in photovoltaic applications, providing distributed energy sources which could reduce the fluctuation of energy in large scale PV plants [51].

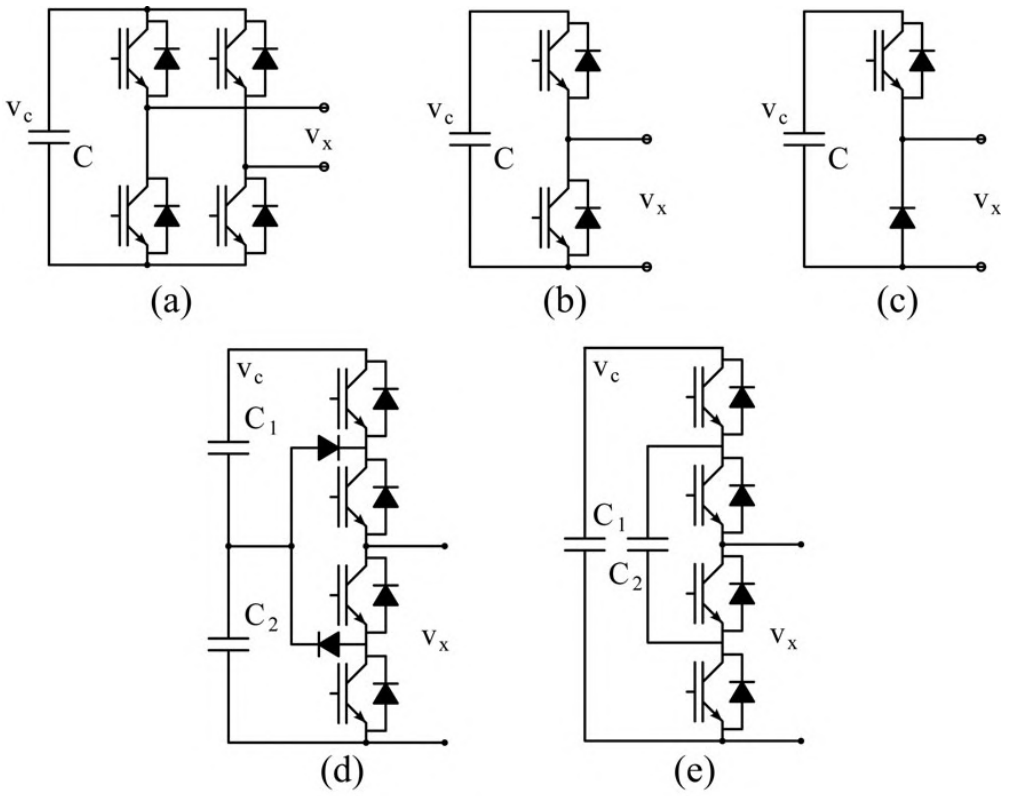
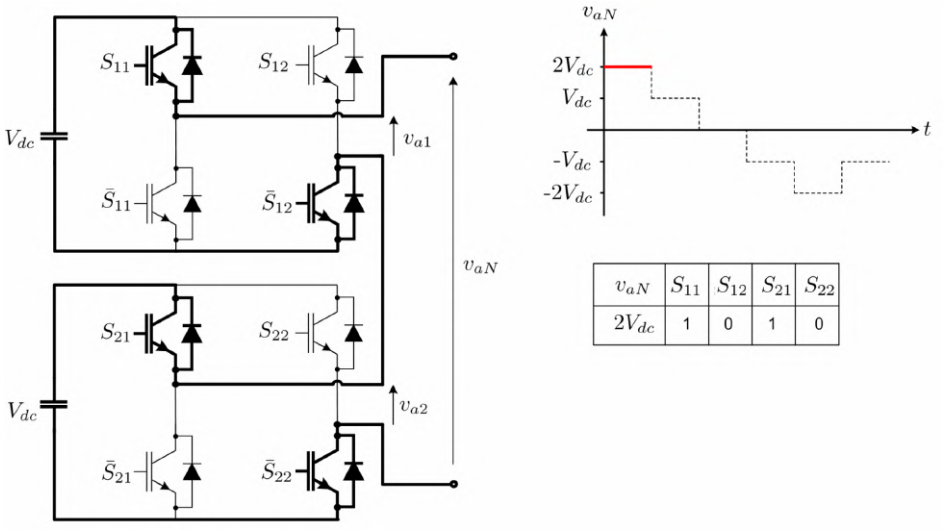


Figure 3.17: Various power cell topologies for MMC. (a) Full-bridge. (b) Half-bridge. (c) Unidirectional cell. (d) Multilevel NPC cell. (e) Multilevel flying capacitor cell.

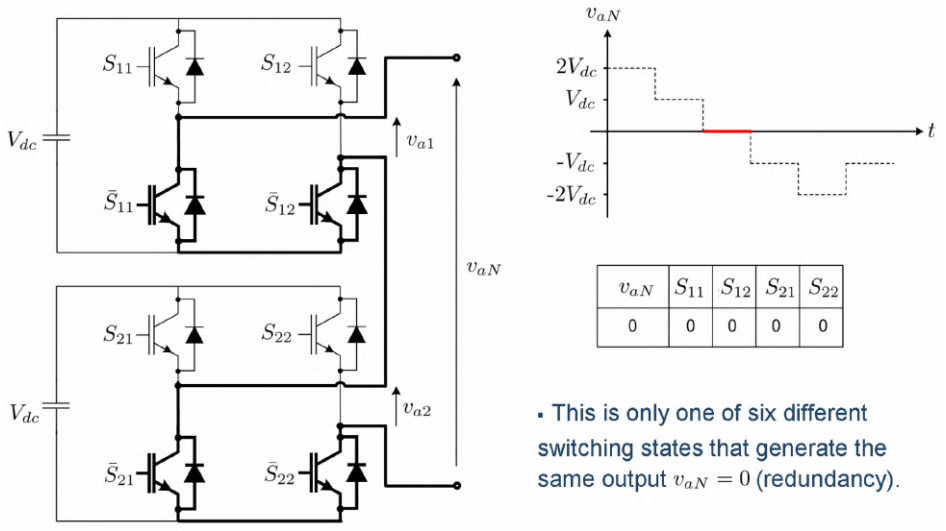
3.6 Summary

In this chapter, the most well-known and applicable topologies of multilevel converters were presented. In this regard, Neutral Point Clamped (NPC), Flying Capacitor Clamped (FC), Cascaded H-bridge (CHB) and Modular Multilevel Converters (MMC) are described in detail. Also, their benefits and drawbacks were discussed and their applications were noted.



v_{aN}	S_{11}	S_{12}	S_{21}	S_{22}
$2V_{dc}$	1	0	1	0

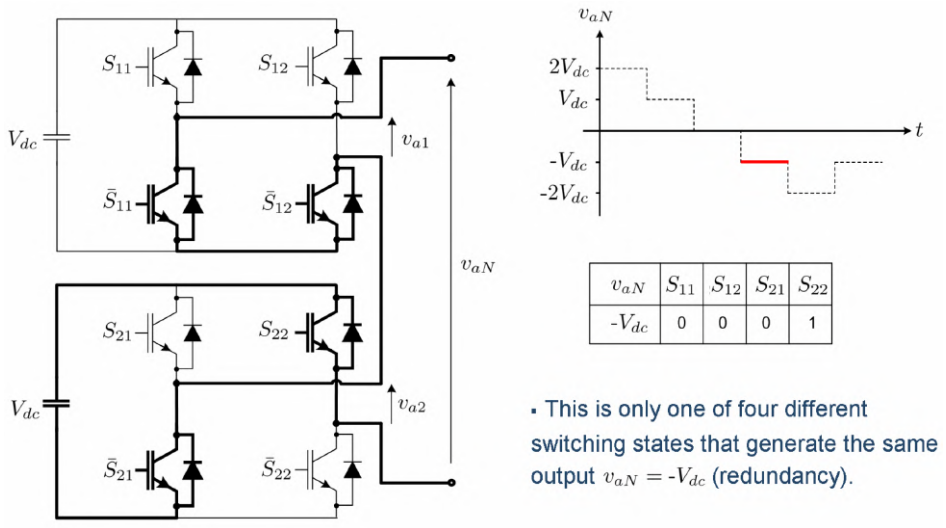
(a) Generating of $+2V_{dc}$ in output voltage v_{aN} and switching states.



v_{aN}	S_{11}	S_{12}	S_{21}	S_{22}
0	0	0	0	0

- This is only one of six different switching states that generate the same output $v_{aN} = 0$ (redundancy).

(b) Generating of 0-level in output voltage v_{aN} and switching states.



v_{aN}	S_{11}	S_{12}	S_{21}	S_{22}
$-V_{dc}$	0	0	0	1

- This is only one of four different switching states that generate the same output $v_{aN} = -V_{dc}$ (redundancy).

(c) Generating of $-V_{dc}$ in output voltage v_{aN} and switching states.

Figure 3.10: A 3-level cascaded multilevel inverter and switching states [6].

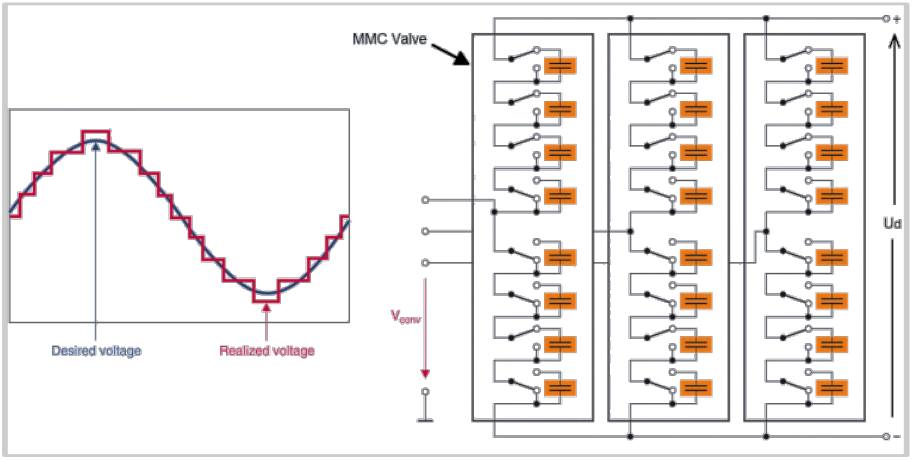


Figure 3.13: The basic structure of Modular Multilevel Inverter (MMC).

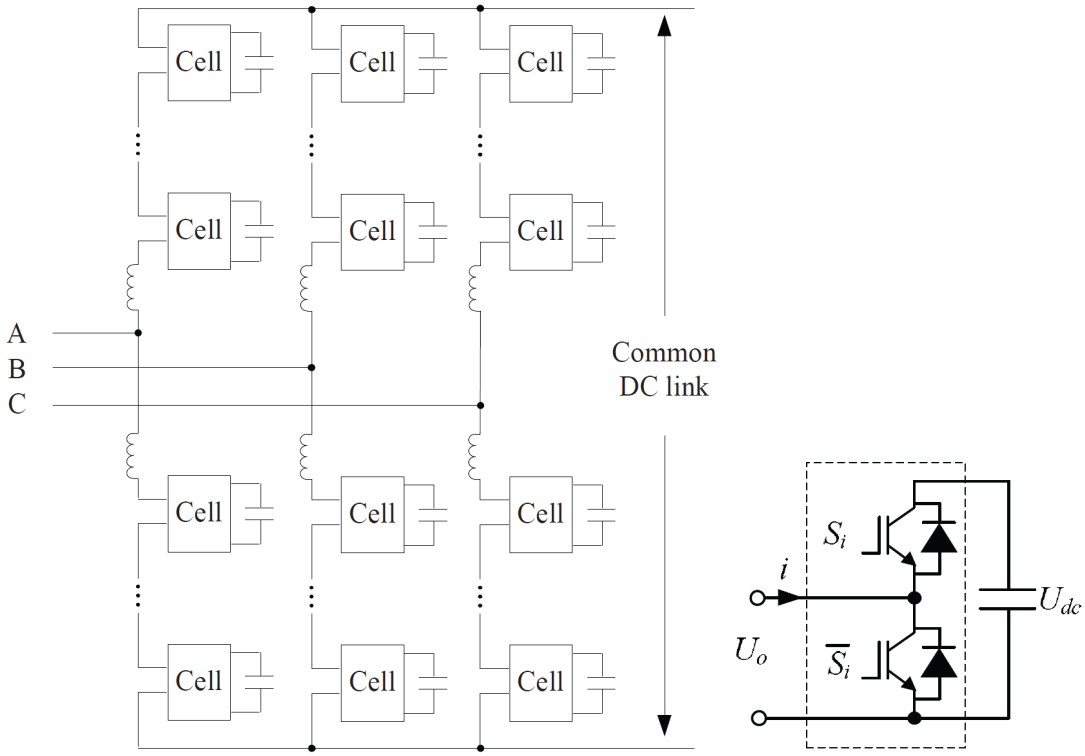


Figure 3.16: Three-phase/DC MMC circuit topology for HVDC applications.

4 State of Art: Modulation Techniques for Multilevel Converters (MLC)

4.1 Overview

Many new modulation techniques have been developed to cater the growing number of multilevel inverter topologies. They are aimed at generating a stepped switched waveform that best approximates an arbitrary reference signal with an adjustable amplitude, frequency, and phase fundamental component that is usually a sinusoidal in steady state. Since the modulation scheme is intended to be used in high-power converters, the main figures of merit pursued are high power quality and minimum switching frequency. These two requirements compete with each other, and therefore, it is considered one of the major challenges in multilevel converter technology. Despite this, some basic extensions of the classic modulation methods used for Two-level Voltage Source Inverter (2L-VSI) are the ones that have been used in commercial converters.

Together with the development of multilevel inverter topologies appeared the challenge to extend traditional modulation methods to the multilevel case. On one hand, there is the inherent additional complexity of having more power-electronics devices to control, and on the other the possibility to take advantage of the extra degrees of freedom provided by the additional switching states generated by these topologies. As a consequence, a large number of different modulation algorithms have been adapted or developed depending on the application and the converter topology, each one having unique advantages and drawbacks. A classification of the most common modulation methods for multilevel inverters is presented in Fig. 4.1. The modulation algorithms are here classified depending on the average switching frequency with which they operate, i.e., high or low. For high-power applications, high switching frequencies are considered those above $1\,kHz$.

Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular methods in industrial applications is the classic carrier-based Sinusoidal PWM (SPWM) that use the phase-shifting and level-shifting techniques to reduce the harmonics in the load voltage [11, 71], [73, 74]. Another interesting alternative

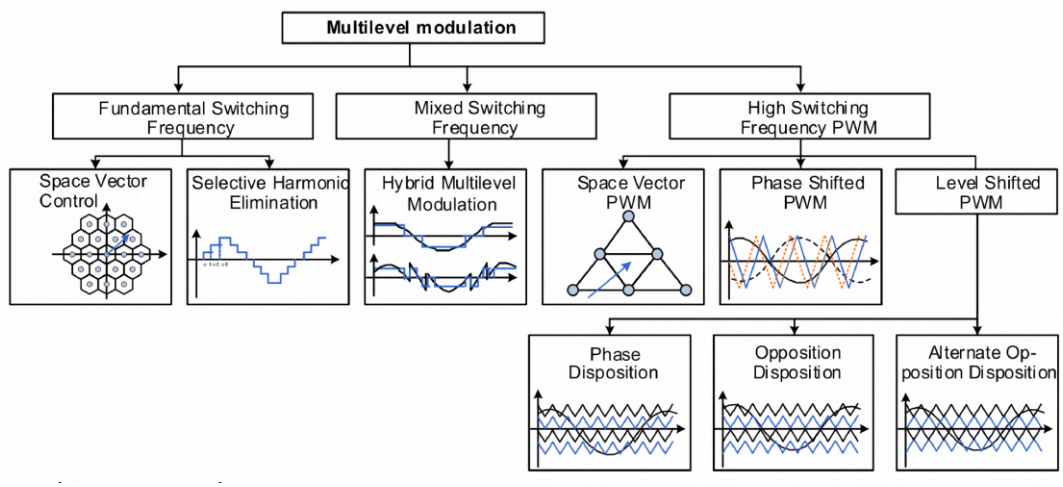


Figure 4.1: Classification of multilevel converters modulation methods [6].

is the Space Vector Modulation (SVM) strategy, which has been used in three-level inverters [75]. SVM has also been extended and even generalized for n-level multilevel converters using 2-D and 3-D algorithms [76]–[87].

The Level-Shifted PWM (LS-PWM) and Phase-Shifted PWM (PS-PWM) techniques have been the natural extensions of carrier-based SPWM for the NPC and for multicell converters (CHB and FC), respectively [17, 88]. The LS-PWM, which is also known as Phase-Disposition PWM (PD-PWM), and other carrier disposition variants [74] are a simple way to relate each carrier with the gating signals of NPCs and therefore are one of the two modulations schemes used in the industry and commonly referred to simply as SPWM. The PS-PWM associates a pair of carriers to each cell of the CHB and FC, and a phase shift among the carriers of the different cells introduces asynchronism, which generates the stepped waveform. In this case, the advantage lies in that power being evenly distributed among the cells across the entire modulation index, which enables correct operation of the multipulse rectifier configuration of the CHB and a natural balancing of the capacitors in the FC [88]. Therefore, PS-PWM is also the only real commercial modulation scheme used in CHB and FC. Although it has been reported that PD-PWM has better output voltage harmonic profile than PS-PWM [74], these are very small differences in the high-frequency harmonic content, which are filtered by the load. Therefore, from a practical point of view, the operational advantages of PS-PWM for CHB and FC are far more relevant than the superior harmonic content of PD-PWM, explaining the trend followed by the industry.

Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination [89, 90] and the Space Vector Control (SVC), also is known as Nearest Vector Control (NVC) [91]-[93]. Another low switching frequency

modulation method is Nearest Level Control (NLC) [94].

Multilevel Selective Harmonic Elimination (SHE) is commercially available modulation method that also comes from the two-level version is [88, 76, 96]. This method is the second one available for 3L-NPCs. The main feature is that, unlike carrier-based PWM methods, the switching angles are computed offline and are designed in such a way that arbitrary harmonics (usually of low order) are eliminated. This method has the advantage of having very few commutations per cycle and is therefore the one that achieves better efficiency and enables air cooling. On the negative side, the SHE angles are computed based on the Fourier series and the assumption of steady-state sinusoidal voltages; hence, for variable-speed operation, these angles will not fully eliminate the harmonics, which, through feedback, can greatly be amplified by the closed-loop controller, degrading overall performance, and therefore is limited in practice to low-dynamic-performance demanding drive applications (pumps, fans, etc.).

Modulation at high switching frequencies modulations based on triangular-wave carrier signals with phase shifting [97] and level shifting [98] can be modified for use in MMCs. Both of these types of carrier-based modulation are established, well-known techniques, but they have the disadvantage of high switching losses compared to, e.g., fundamental frequency modulation. Space vector modulation can be also adapted to multilevel converters, but as the number of levels increases, the complexity of the algorithm grows exponentially. Low-frequency modulation is preferred in MMCs, due to the high number of output levels of this converter. SHE can be applied to MMCs [99], but the process of finding the switching angles becomes complex as the number of level increases. Staircase or nearest level modulation are particularly useful for the MMC, because, compared to SHE, the performance is comparable and the implementation is more simple [100].

In this chapter, sec. 4.2 presents traditional sinusoidal pulse width modulation method (SPWM) for two- and three-level converters. At the following, PS-PWM, LS-PWM, SVM, Hybrid PWM (H-PWM), NVC, NLC and SHE multilevel converters modulation methods are presented in sec. 4.3, sec. 4.4, sec. 4.5, sec. 4.6, sec. 4.7, sec. 4.8 and sec. 4.9, respectively. sec. 4.9 describes the available methods to solve the selective harmonic elimination problem, as well.

4.2 Sinusoidal Pulse Width Modulation (SPWM)

In sinusoidal pulse width modulation the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the center of the same pulse. The distortion factor and lower order harmonics are then reduced significantly. There are two control ways to generate SPWM pulses. They are bipolar modulation and unipolar modulation. The bipolar SPWM has been widely used in the digitally controlled H-bridge inverter system because of its simple implementation. However, the

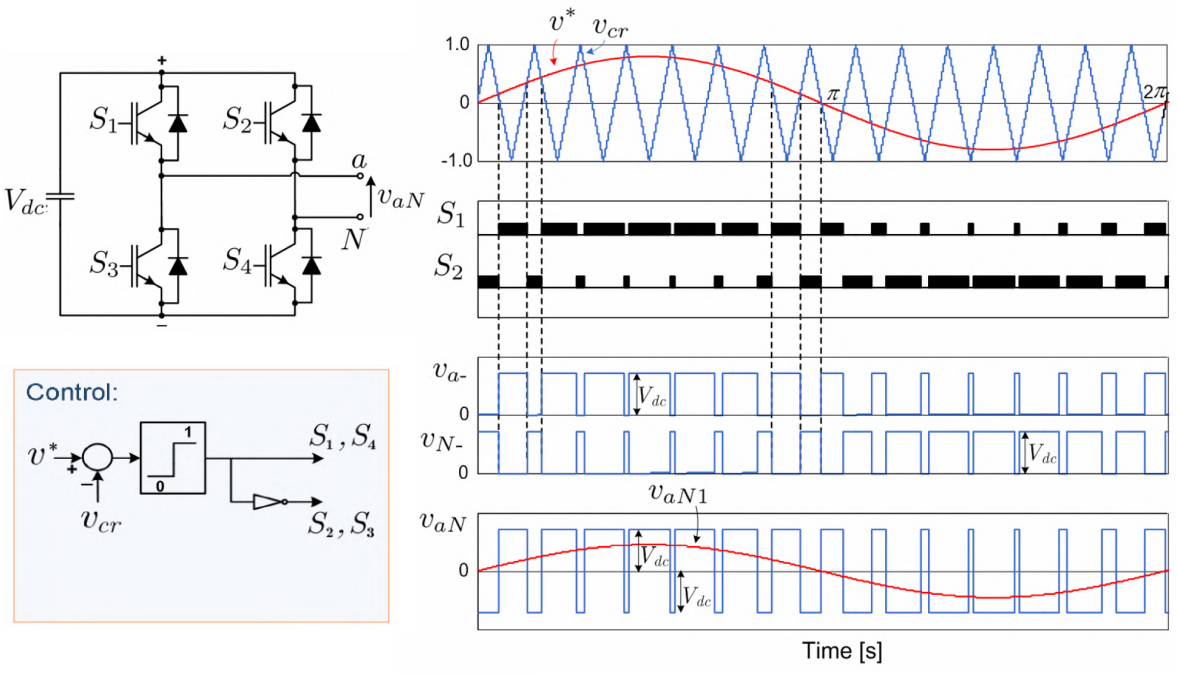


Figure 4.2: Bipolar SPWM for a two-level inverter and its control [6].

number of output voltage pulses and the frequency of the lowest harmonic voltage, which can also be named equivalent switching frequency, in the unipolar SPWM are twice those in the bipolar SPWM with the same switching frequency. The advantage of this method is that the filter elements needed are much less due to the fact that the equivalent switching frequency of the output voltage is twice the switching frequency. Therefore, the unipolar SPWM facilitates the choice of filter and has better output waveforms.

Fig. 4.2 shows bipolar SPWM for a two-level inverter (H-Bridge) and gate signal generation procedure. The gating signals are generated by comparing a sinusoidal reference signal v^* with a triangular carrier waveform v_{cr}. The frequency of reference signal, determines the inverter output frequency and its peak amplitude controls the modulation index M, and output voltage V_{aN} rms value. The number of pulses per half cycle depends on carrier frequency and the inverter uses the frequency of the triangle wave as the switching frequency.

In three-level inverters, unipolar PWM can be achieved by phase shifting of reference signal and carrier signal in bipolar PWM as illustrated in Fig. 4.3 and Fig. 4.4, respectively. In Fig. 4.3, the triangular carrier waveform v_{cr} is compared with two reference signals v^* and $-v^*$, which are positive and negative signal (180° phase shift). The basic idea to produce SPWM with unipolar voltage switching is shown in Fig. 4.3. The difference between the bipolar SPWM is that the generator uses another comparator to compare between the inverse reference waveform $-v^*$. The other method to generate unipolar PWM is achieved by applying 180° phase shift in

carrier signal v_{cr} as shown in Fig. 4.4. As shown in this figure, the reference signals v^* is compared with two triangular carrier waveform v_{cr} and $-v_{cr}$.

In unipolar SPWM the output voltage swings from 0 to $+V_{dc}$ or from 0 to $-V_{dc}$. This is in contrast to the bipolar SPWM strategy in which the output voltage swings between V_{dc} and $-V_{dc}$. So, the output voltage pulse amplitude is reduced in the unipolar from $2V_{dc}$ to V_{dc}. The effective switching frequency seen by the load is also doubled in the unipolar case. Due to these, the harmonic content of the output voltage waveform is reduced compared to Bipolar switching. Also in unipolar SPWM method, the amplitude of the significant harmonics and its sidebands is much lower for all modulation indexes thus makes filtering easier, and results in significantly smaller filter size.

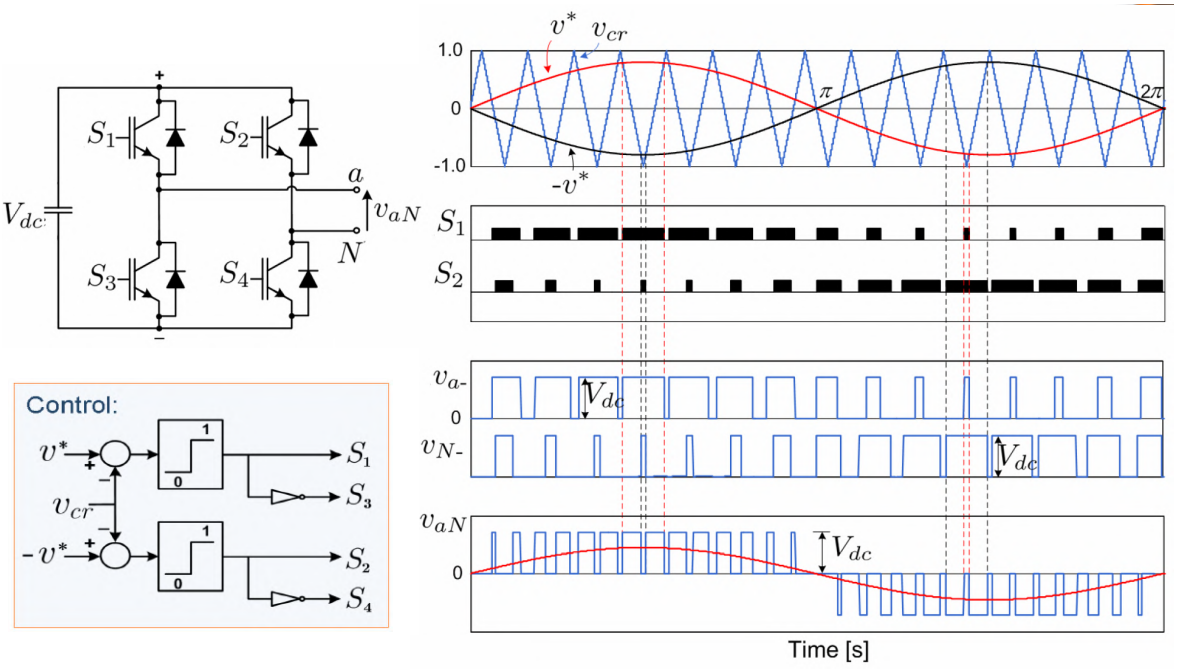


Figure 4.3: Unipolar SPWM and its control in a three-level inverter with extra phase shifted reference signal [6].

4.3 Phase Shifted PWM (PS-PWM)

Phase-shifted PWM (PS-PWM) is a natural extension of traditional PWM techniques, specially conceived for FC [32] and CHB [11] converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal. A phase shift is introduced between the carrier signals of contiguous cells, producing a phase-shifted switching pattern between them. In this

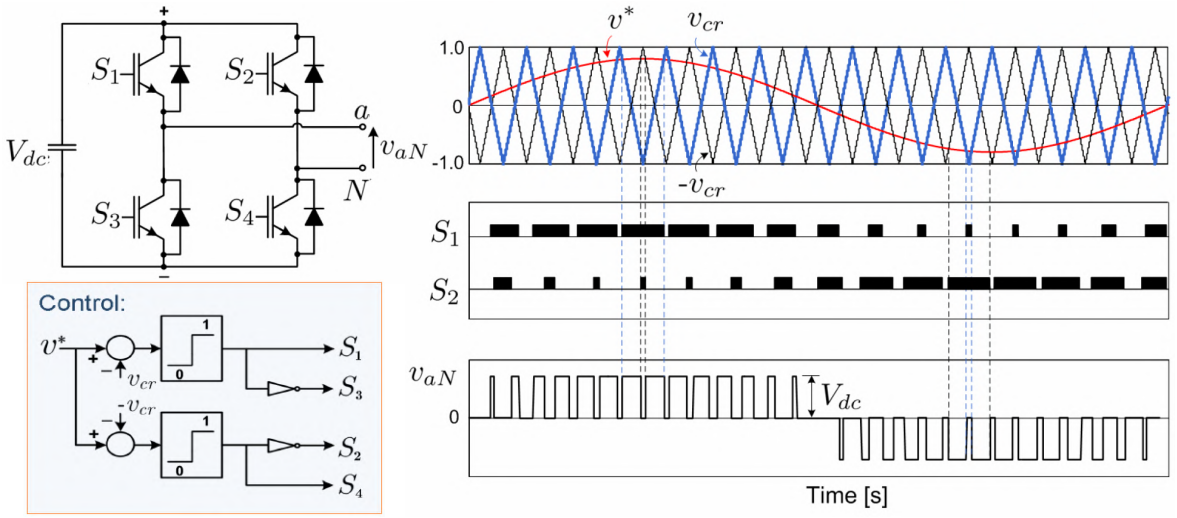


Figure 4.4: Unipolar SPWM and its control in a three-level inverter with extra phase shifted carrier signal [6].

way, when connected together, a stepped multilevel waveform is originated. It has been demonstrated that the lowest distortion can be achieved when the phase shifts between triangular carriers (θ_{cr}), are $180°/k$ or $360°/k$ for a CHB or FC converter, respectively (where k is the number of power cells). This difference is related to the fact that the FC and CHB cells generate two and three levels, respectively. A seven-level CHB example of the operating principle is illustrated in Fig. 4.5.

Since all the cells are controlled with the same reference and same carrier frequency, the switch device usage and the average power handled by each cell is evenly distributed. For the case of the CHB, this means that multipulse diode rectifiers can be used to reduce input current harmonics. For the FC, the advantage of the even power distribution is that once the flying capacitors are properly charged (initialized to their corresponding values), no unbalance will be produced due to the self-balancing property of this topology [101, 102]; hence there is no need to control the dc-link voltages. Another interesting feature is the fact that the total output voltage has a switching pattern with k times the frequency of the switching pattern of each cell. This multiplicative effect is produced by the phase-shifts of the carriers. Hence, better total harmonic distortion (THD) is obtained at the output, using k times lower frequency carriers. The corresponding implementation diagram is illustrated in Fig. 4.6.

Fig. 4.7 shows output voltage THD of PS-PWM for different values of θ_{cr} in a seven-level CHB inverter. As shown from this figure, optimum phase shift between carriers is achieved when $\theta_{cr} = 180/3 = 60°$, in which the lower THD is gained.

4.4 Level Shifted PWM (LS-PWM)

Level-shifted PWM (LSPWM) is the natural extension of bipolar PWM for multilevel inverters. Bipolar PWM uses one carrier signal that is compared to the

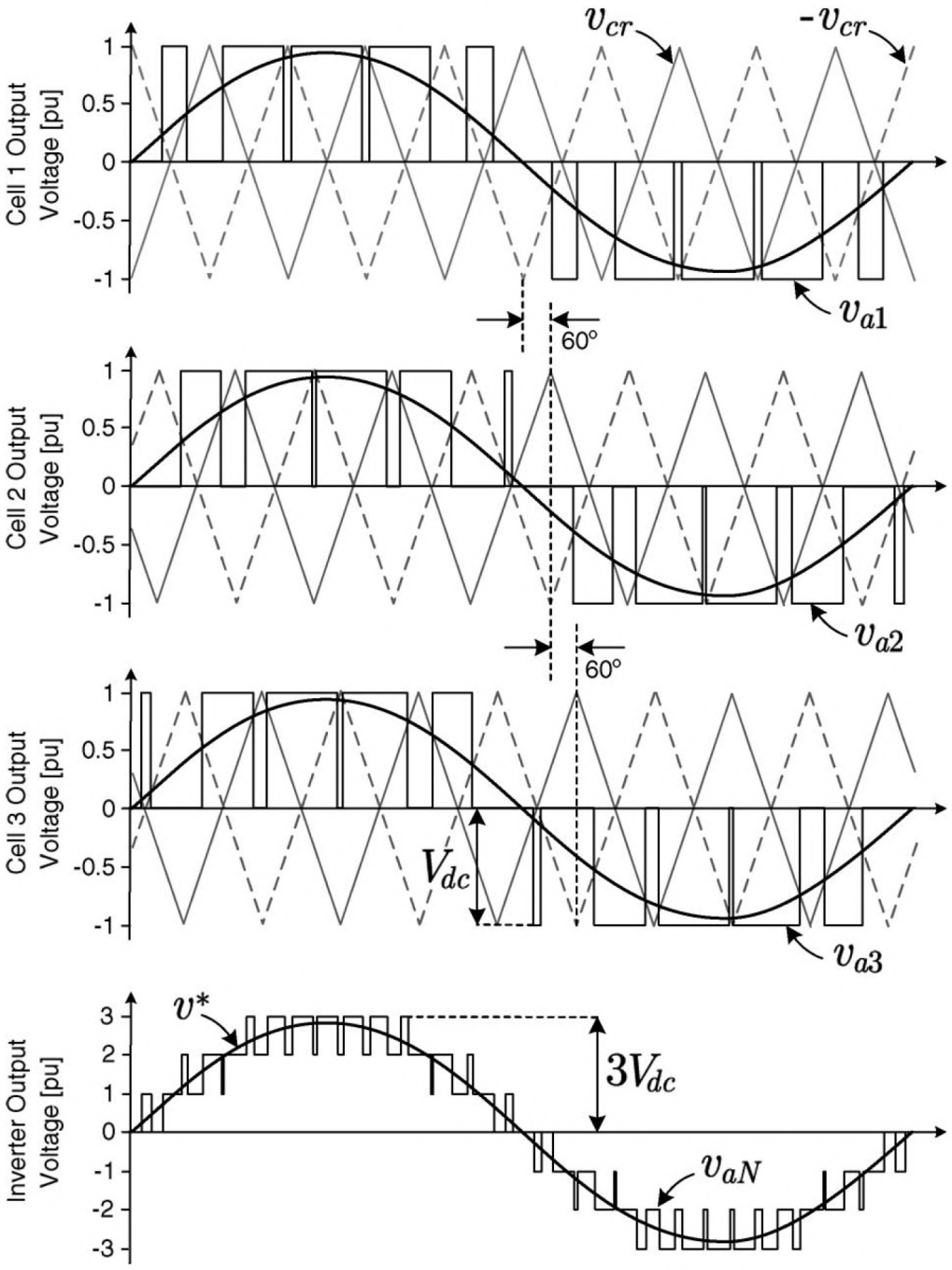


Figure 4.5: Three-cell (seven-level) PS-PWM waveform generation for CHB [88].

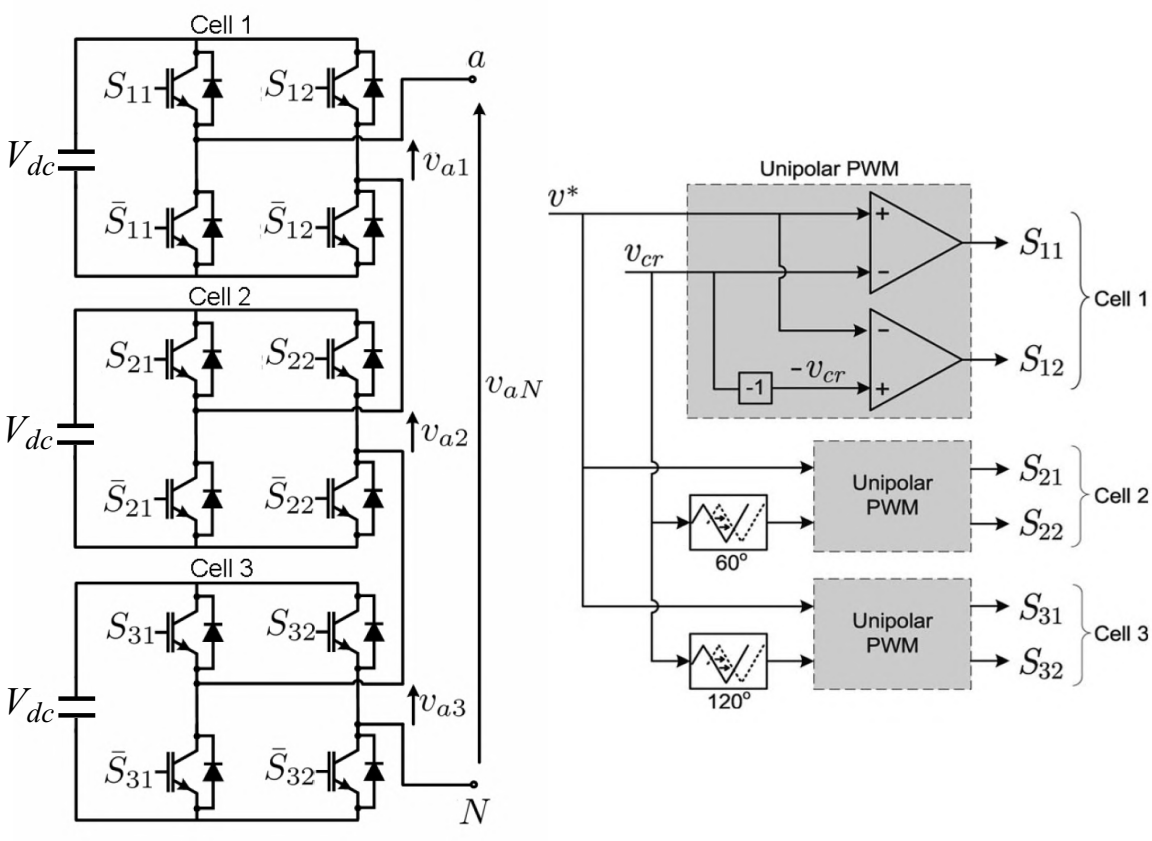


Figure 4.6: Three-cell (seven-level) PS-PWM control diagram for CHB [88].

reference to decide between two different voltage levels, typically the positive and negative busbars of a VSI. By generalizing this idea, for a m-level multilevel inverter, $m-1$ carriers are needed. They are arranged in vertical shifts instead of the phase-shift used in PS-PWM.

Each carrier is set between two voltage levels; hence the name "level shifted." Since each carrier is associated to two levels, the same principle of bipolar PWM can be applied, taking into account that the control signal has to be directed to the appropriate semiconductors in order to generate the corresponding levels. The carriers span the whole amplitude range that can be generated by the converter. They can be arranged in vertical shifts, with all the signals in phase with each other, called phase disposition (PD-PWM); with all the positive carriers in phase with each other and in opposite phase of the negative carriers, known as phase opposition disposition (POD-PWM); and alternate phase opposition disposition (APOD-PWM), which is obtained by alternating the phase between adjacent carriers [73]. An example of these arrangements for a five-level inverter (thus four carriers) is given in Fig. 4.8(a)–(c), respectively.

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. In Fig. 4.9, a

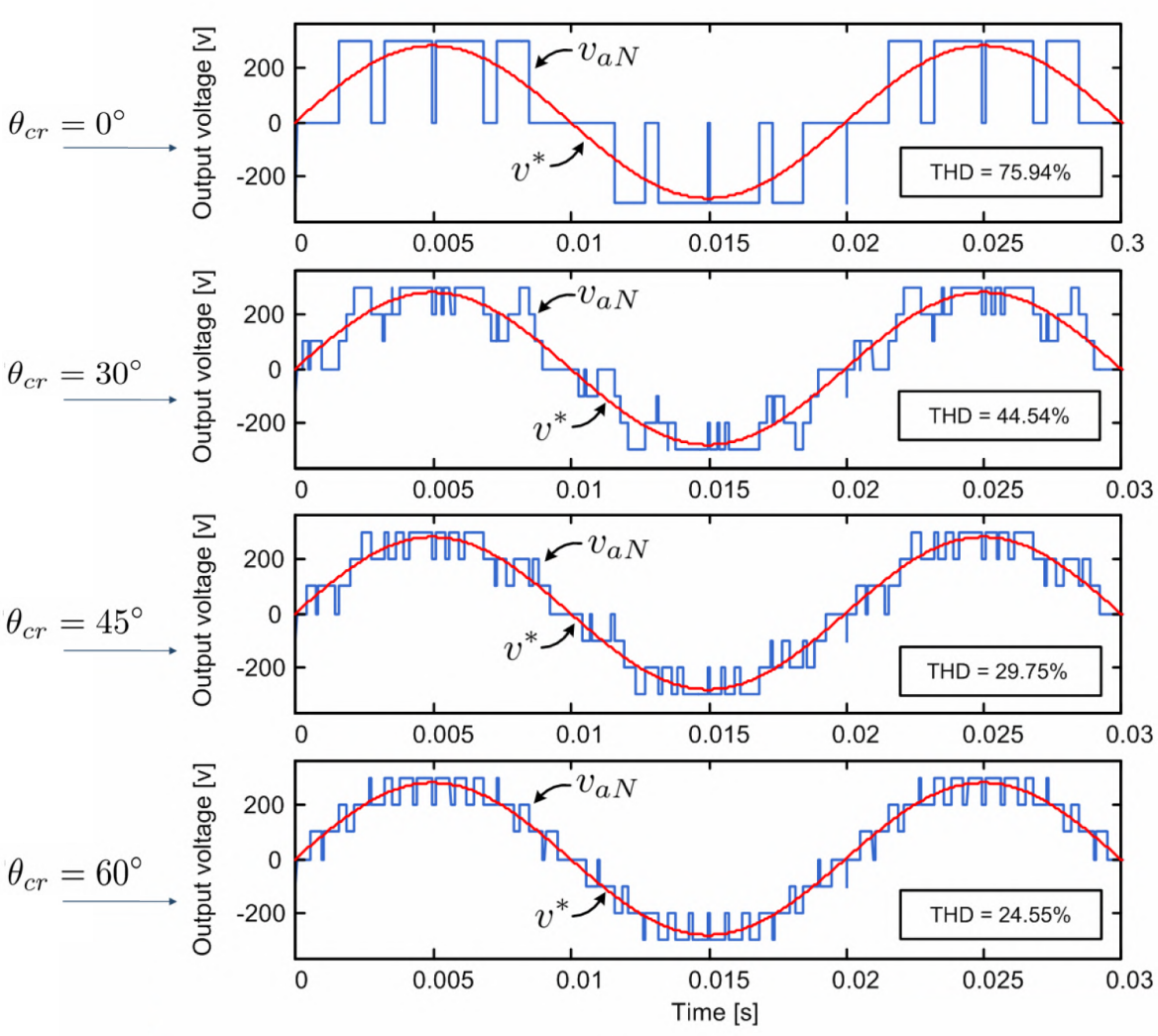


Figure 4.7: THD of Three-cell CHB (7-level) PS-PWM for different values of θ_{cr} [6].

qualitative example for a three-level NPC is illustrated. From Fig. 4.9(a), it can be observed that the times during which the value of the reference is greater than the value of both carriers, the upper switches are turned on connecting the load to the positive busbar. During the times the reference value is between both carriers ($v_{cr2} \leq v^* \leq v_{cr1}$), the output is connected to the neutral point N. Finally, the times in which the reference value is lower than both carriers, the lower switches are turned on, connecting the load to the negative busbar. The control diagram that performs this algorithm is shown in Fig. 4.9(b). Note that the gating signals of Fig. 4.9(b) are defined for the three-level NPC, as shown in Fig. 3.3.

LS-PWM leads to less distorted line voltages since all the carriers are in phase compared to PS-PWM [103]. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topol-

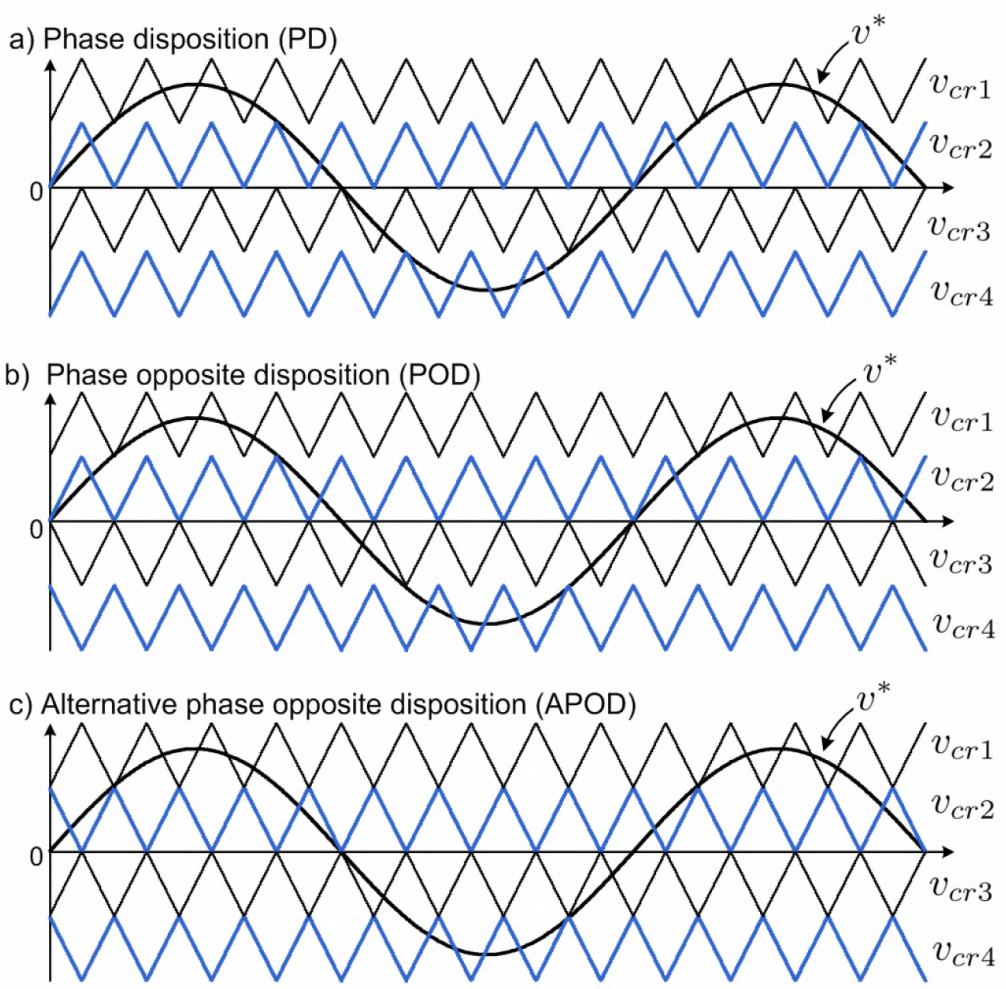


Figure 4.8: LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD [88].

ogy. However, this method is not preferred for CHB and FC, since it causes an uneven power distribution among the different cells. This generates input current distortion in the CHB and capacitor unbalance in the FC compared to PS-PWM.

Fig. 4.10 shows waveform generation and control diagram of LS-PWM for two-cell CHB (5-level) multilevel inverter. As shown in this figure, for 5-level inverter 4 carriers are needed and two carriers are used for each cell. The two internal carriers are used for Cell 1 and the other two outer carriers are used for Cell 2.

Advantages of PS-PWM and disadvantages of LS-PWM can be summarized as follows.

Advantages of PS-PWM:

- All cells are equally loaded.
- The cells have same switching losses.
- Semiconductor use among cells are equal.

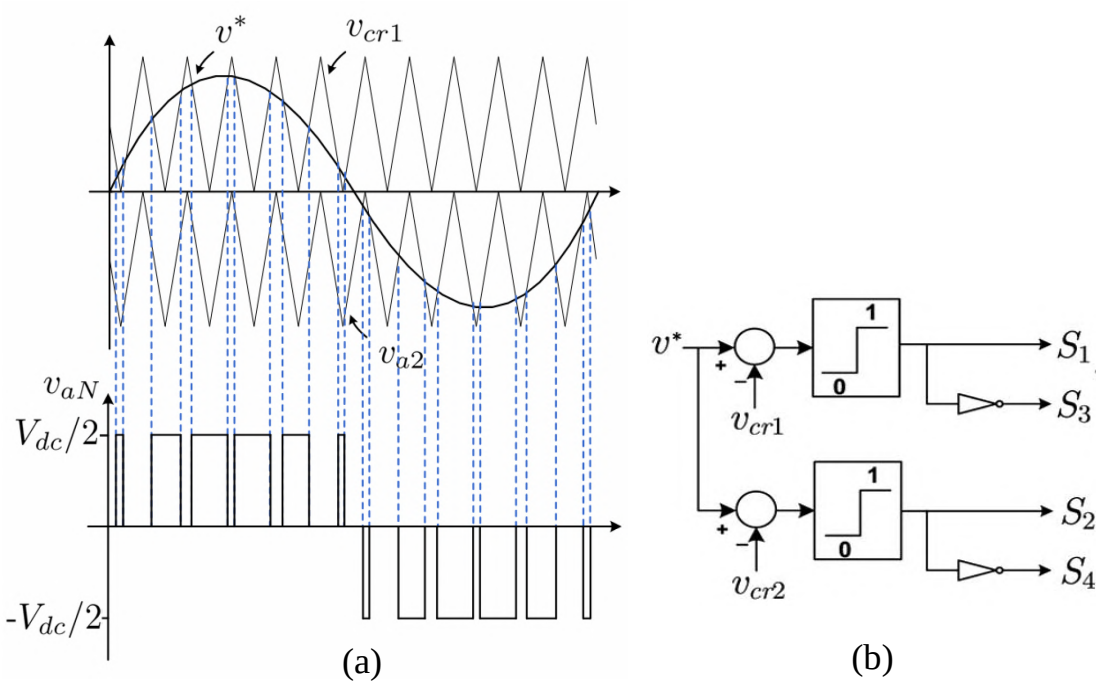


Figure 4.9: LSPWM for 3-level NPC inverter: (a) waveform generation and (b) control diagram (refer to Fig. 3.3) [6].

- capability of input current harmonic cancellation.

Disadvantages of LS-PWM:

- Different power distribution among cells.
- Different switching losses.
- Only the use of some semiconductors.
- The most used semiconductors operate at high switching frequency.
- No input current harmonic cancellation.

4.5 Space Vector Modulation (SVM)

In contrast with the high amount of recently introduced multilevel topologies, no new multilevel modulation schemes have made their way to industrial applications, despite the great amount of recent contributions and advances on this topic. The main reason could be that manufacturers favor the proven technology and simplicity of carrier-based PWM schemes over new methods that have advantages but usually at the expense of more complex implementation. Nonetheless, multilevel converters have many additional degrees of freedom, compared with two-level converters: more voltage levels, zero common-mode voltage vectors, switching-state or voltage-level

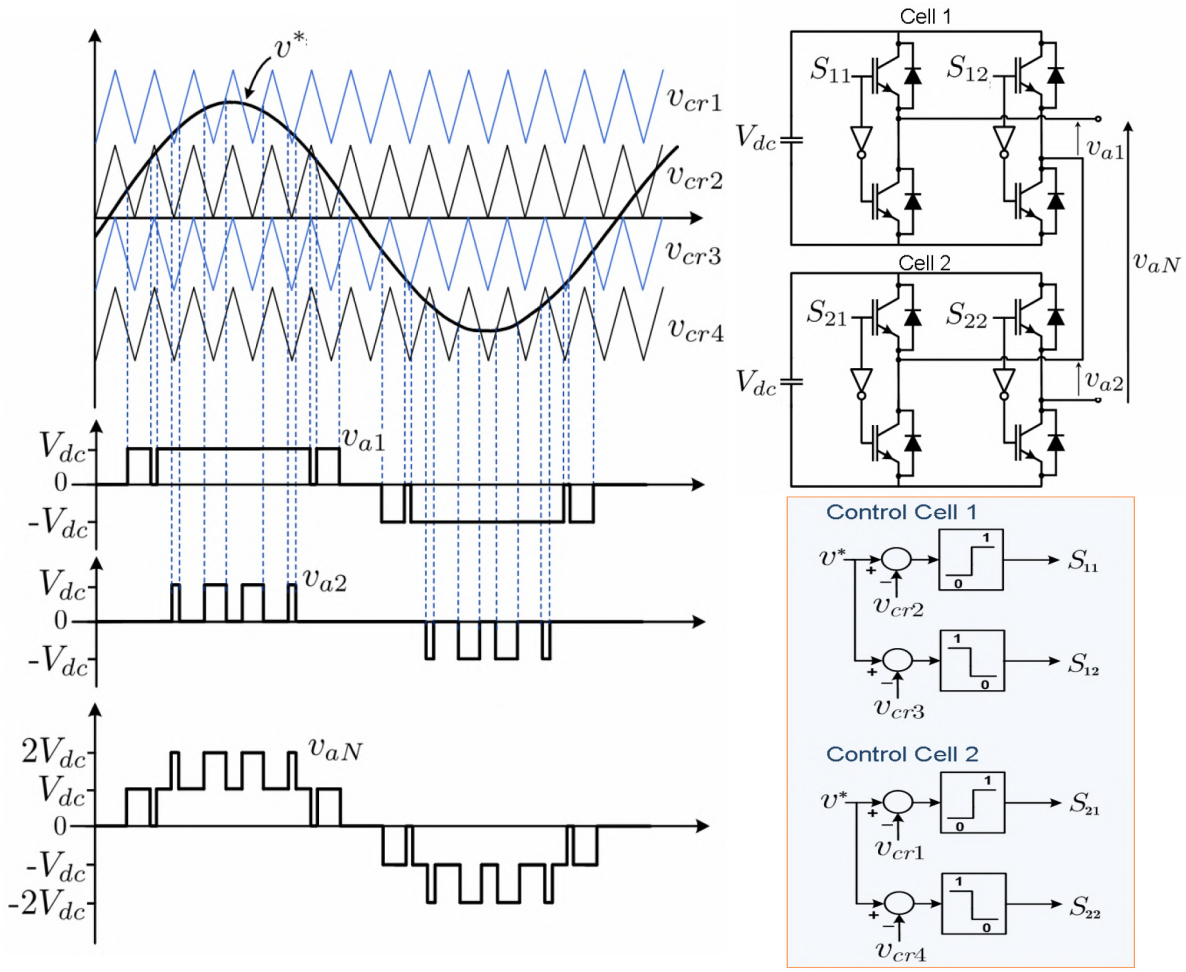


Figure 4.10: LS-PWM for 5-level CHB inverter: waveform generation and control diagram [6].

redundancy, and space vector redundancy, which are not always fully exploited by carrier-based PWM schemes, which, in turn, together with the appearance of new converter topologies, are the main drivers for the development of new modulation strategies.

One of the modulation methods that have the potential to more effectively use these new degrees of freedom is space vector modulation (SVM). SVM has also been extended and even generalized for n-level multilevel converters using 2-D and 3-D algorithms [76]–[87]. A common characteristic to all SVM-based schemes is that the modulation algorithm is divided into three stages: in the first, a set of switching states or vectors needs to be selected for modulation, which usually are the three closest vectors to the reference [76]; the second stage computes the duty cycles (or On and Off times) of each vector to achieve the desired reference over a time average; and the final third stage is the sequence in which the vectors are generated. Usually, center-distributed or symmetric sequences are favored due to synchronous digital

sampling of the current. The different contributions that report variations on the three basic stages of SVM pursue different goals, which, in many cases, are one or more of the following: switching frequency reduction, lower computational cost, common-mode voltage elimination or reduction, lower THD, SVM for multiphase systems, unbalanced system operation, capacitor voltage balance, feed forward of dc-link ripple, etc.

Despite all these reported improvements, SVM-based multilevel algorithms are not the dominant modulation scheme found in industrial applications to this date. A probable reason is that carrier-based PWM requires only the reference and carrier signal and a simple comparator to deliver the gating signals, whereas even very low complexity and low-computational-cost SVM methods require an algorithm with at least the three stages mentioned before.

Recently, it has been demonstrated that the same voltage waveform generated by the most common SVM algorithms can be obtained in a much simpler way using a single-phase modulator [86]. The advantages are that it can easily be extended to converters with any number of phases and any number of levels, hereby reducing the design, implementation, and computation complexity usually associated to SVM algorithms.

Cascaded converters feeding both sides of an open-end winding stator can generate (depending on the voltage ratio between them) non conventional voltage space vector distributions that follow a different pattern than the traditional concentric hexagonal layout in the $\alpha - \beta$ complex plain. In fact, they generate 12- and 18-sided polygonal space vector distributions [104, 105]. As the number of sides of the polygon increases, the space vector distribution for the same magnitude becomes closer to a circle. As such, the instantaneous error between the reference vector and the switching-state space vectors decreases. This further reduces dv/dts and improves the harmonic content in the output voltage without need to increase the device switching frequency. SVM schemes for these polygonal distributions are presented in [104] and [105].

The space vector modulation (SVM) algorithm is basically also a PWM strategy with the difference that the switching times are computed based on the three-phase space vector representation of the reference and the inverter switching states rather than the per-phase in time representation of the reference and the output levels as in previous analyzed methods.

4.5.1 State-Space Vector Representation of the Inverter

voltage state-space vector vs combines simultaneously the values of the three-phase variables and maps them into a unique vector in the α–β complex plane by

$$v_s = \frac{2}{3}\left[v_a + a v_b + a^2 v_c\right] \tag{4.1}$$

where $a = -(1/2) + j\left(\sqrt{3/2}\right)$. By replacing in (4.1) the phase output voltages of the inverter (v_a, v_b, v_c) for each possible switching state, the inverter state-space vectors can be obtained. An example for a three-phase three-level NPC inverter is given in Fig. 4.11. Note that the NPC has three phases and three output levels or switching states, resulting in 33 possible combinations; hence 27 state-space vectors (in general, the number of state vectors of a three-phase N-level converter is N^3). However, only 19 are different, and eight are redundant. There is triple redundancy in the zero state vector and double redundancy in the six short state vectors (internal vectors). For example, the zero vector can be obtained in three ways: 1) connecting the three-phase outputs to the positive busbar ($v_a = v_b = v_c = +V_{dc}$), corresponding to the switching state $(+,+,+)$ or to the neutral point ($v_a = v_b = v_c = 0$), corresponding to the state $(0,0,0)$; or to the negative busbar ($v_a = v_b = v_c = -V_{dc}$), corresponding to the state $(-,-,-)$.

From the load point of view, redundant vectors have the exact same influence, and it makes no difference which one is used. From the inverter point of view, they are different switching states, and this can be used as an additional degree of freedom for other control purposes, as will be discussed later in Section VI-A. It is worth mentioning that, since the possible output levels of the inverters are fixed ($-V_{dc}$, 0, *and* $+V_{dc}$), the state-space vectors are also fixed. Note that for a traditional two-level VSI, only seven different space vectors are obtained [106], while by just adding a third level like in NPC, 19 different can be generated. This increases over proportionally in relation to the numbers of levels and is in direct accordance with the output power quality, as a more dense state-space vector representation in the α–β plane is obtained, in the same way more levels are a more dense coverage of the amplitude range in the per-phase time representation.

The three-phase reference can also be mapped to the α–β plane using the same transformation (4.1) but replacing the phase reference voltages instead of the phase output voltages. Since the references are not switched variables with fixed voltage values as the output phase voltages of the inverter, the reference space vector v_s^* can be mapped anywhere in the α–β plane and not necessarily coincide with any of the inverter space vectors, analogous to the per-phase time representation, where the reference signal does not necessary match an inverter output level. For balanced three-phase sinusoidal references, as is usual in power-converter systems, the resulting reference vector v_s^* is a rotating space vector, with the same amplitude and angular speed (ω) of the sinusoidal references, with an instantaneous position with respect to the real axis given by $\theta = \omega t$ as the one illustrated in Fig. 4.11.

SVM techniques can be classified into algorithms for balanced or unbalanced systems, depending on the application. It is important to know if the reference vector also contains harmonics or if the control technique must compensate harmonics or zero sequence components in three-phase four-wire systems with neutral. In case of generating purely sinusoidal reference voltages, the use of balanced algorithms is enough; however, for the other cases, three-dimensional techniques should be considered.

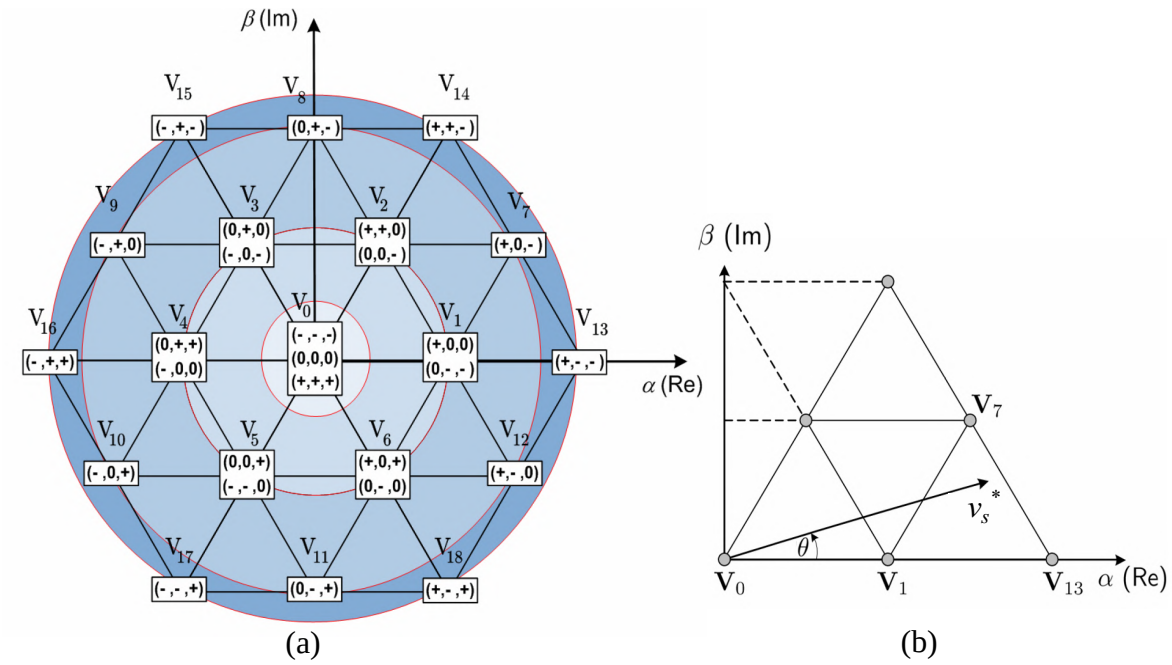


Figure 4.11: Space Vector Modulation: (a) Three-phase three-level converter state-space vectors (b) The reference space vector v_s^* mapped in the α–β plane [6].

4.5.2 SVM Algorithms for Multilevel Balanced Systems

The basic idea of SVM is to use the state-space vector representation introduced earlier to combine or modulate three state-space vectors of the inverter, so that their time average equals the reference space vector, in the same way PWM combines the levels to obtain a time average of the reference in the per-phase representation. The modulation principle of SVM can be summarized by

$$v_s^* = \frac{1}{T_s}\left(t_1 v_1 + t_2 v_2 + t_3 v_3\right) \tag{4.2}$$

where $T_s = t_1 + t_2 + t_3$ is a fixed modulation period (analogous to the carrier period in PWM), v_1, v_2, and v_3, and the three closest vectors to the reference (V_1, V_7, and V_{13} in the qualitative example shown in Fig. 4.11b). The problem is then reduced to finding an algorithm capable of finding the closest vectors to the reference and computing the ON times of each vector t_1, t_2, and t_3. Once these are computed, each vector is generated during the corresponding time, achieving the desired time average over T_s that equals the reference.

There are additional challenges, like the use of the vector redundancies for other purposes like switching frequency reduction by using a particular sequence in which the vectors are generated or to use the redundancies for dc-link voltage unbalance control [107].

Many SVM algorithms based on the previous concept have been reported. They

differ in how the three nearest vectors are chosen, how the times are computed, the sequence used to generate the vectors, and the computational effort necessary for implementation. In [75], a coordinate transformation is introduced to the α–β plane, shifting the complex axis β from 90° to 60° with respect to the α-axis, also called hexagonal coordinates or h–g plane. The advantage is that, when normalized, each vector can be expressed by two integer values in the h- and g-axis, instead of fractional complex components of the β-axis. This greatly simplifies the determination of the three closest vectors to the reference, since they can be located using round functions (floor and ceil). In addition, the ON times can be easily obtained as the fractional parts of the reference in the h- and g-axis.

Another very low computational cost method is presented in [75]. This method is based on the decision-based pulse-width modulation developed for conventional two-level converters [106]. This iterative algorithm is based on the determination of the switching sequence and the duty cycles only considering a sextant of the inverter state-space region shown in Fig. 4.11. This is achieved by rotating the space vector reference to its equivalent in the first sextant in order to facilitate the calculations. This algorithm presents the advantage compared with other methods of eliminating complex mathematical calculations in the switching sequence determination. In addition, the numeric computation of the ON times is reduced to a simple addition.

The geometrical modulation algorithm uses as input the normalized reference voltage vector in order to be independent of the dc-link voltage and the numbers of levels of voltages of the converter. In this way, the states-pace vectors of the converter are placed in the control region in geometrical positions denoted by entire values between zero and $n_p - 1$, where n_p is the number of levels of the multilevel converter. Also, this reference voltage is normalized again, scaling the imaginary part and dividing it by $\sqrt{3}$ [108]. By doing this, the control region is defined by 45° slope triangular regions and allows using very simple online computations to determine the switching sequence and the ON times.

4.5.3 SVM Algorithms for Multilevel Unbalanced Systems

In power converters with neutral connection (usually also named unbalanced systems), the two-dimensional α–β plane is not enough to fully represent the converter system, since the common-mode voltages and currents through the neutral are not considered. An additional γ component (third dimension) is introduced

$$\gamma = (v_a + v_b + v_c)\,. \tag{4.3}$$

The reference vector and the converter switching states are now mapped into this three-dimensional (3-D) region, originating 3D-SVM methods.

a) 3-D SVM algorithm for multilevel converters: The α–β–γ representation offers interesting information about the zero sequence component of currents

and voltages, but the additional dimension adds complexity to the modulation algorithm [84]. Therefore, the natural Cartesian coordinates are used for 3-D multilevel converter modulations to facilitate these calculations. An extension of the geometrical α–β algorithm introduced in the previous section has been reported for the three-dimensional Cartesian a–b–c plane in [84]. In the 3D-SVM method, the nearest four space vectors to the reference vector are considered (four because now the reference voltage vector is mapped into the 3-D space). After a normalization of the reference voltage vector, the control region is defined by a cube with vertexes in positions from zero to $n_p - 1$ in each axis a, b, and c. This cube is formed by a certain number of sub-cubes depending on the number of the levels of the converter. As an example, the state-space vectors of a three-phase three-level converter are shown in Fig. 4.12. In this space vector representation, the switching states are defined as 0, 1, and 2 corresponding to previously defined states −, 0, and +, respectively. This 3D-SVM algorithm considers the sub-cube where the reference vector is located. Thanks to the normalization of the desired reference voltage vector, the closest vector of this sub-cube to the origin is easily calculated as the integer part of each component of the reference voltage vector.

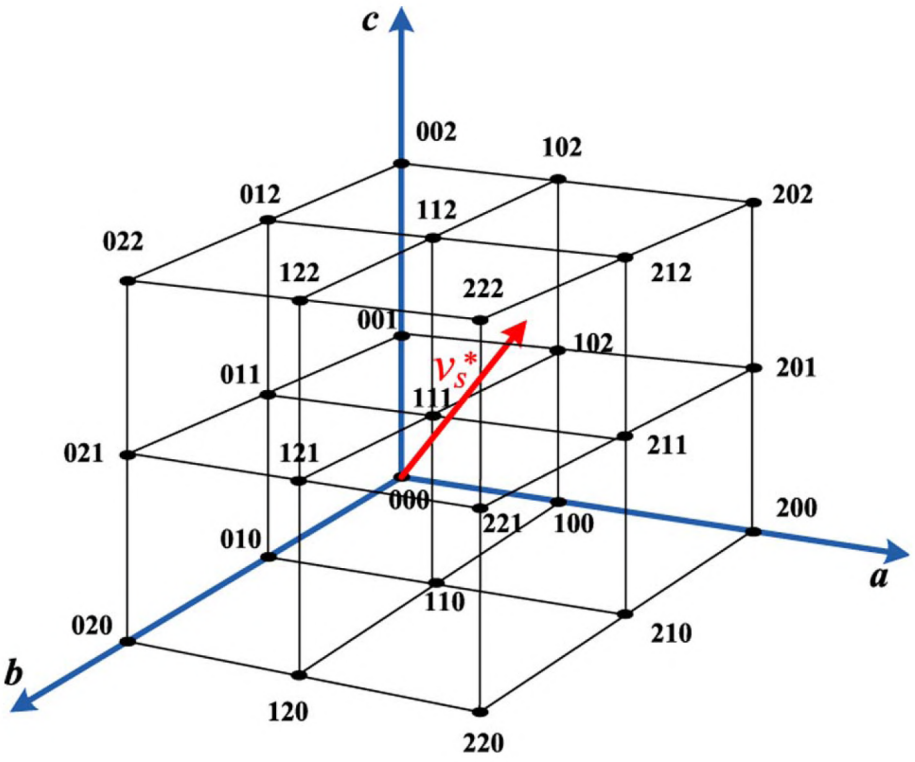


Figure 4.12: State-space vectors of a three-phase three-level converter using the 3-D Cartesian coordinates. This control region is plotted using the normalized phase-to-neutral voltages [88].

In each sub-cube, the four nearest state-space vectors to the reference vector must

be identified [84]. The sub-cubes are divided in six regular tetrahedrons, so the 3D-SVM has to find out the tetrahedron where the reference vector is located, because the vertexes of this tetrahedron are the state-space vectors, which will be used for modulation and form the switching sequence. The determination of the tetrahedron is a very fast algorithm with low computational cost because it implies simple comparisons. Finally, in [84], a table summarizing the switching sequence and the duty cycles corresponding to each tetrahedron is presented. The numeric calculations of the ON times are reduced to simple additions. This reduces significantly the computational requirements and enables this technique to be used as a modulation algorithm in those applications where a 3-D vector region is required (systems with or without neutral, with unbalanced load, with triple harmonics), and it is independent of the number of levels of the converter. Finally, it is important to notice that the 3D-SVM can also be applied to multilevel balanced systems achieving zero common-mode voltage.

b) SVM algorithms for multilevel four-leg four-wire inverters: A wide range of industrial applications use four-leg and four-wire converters (4L-4W) since they provide more zero-sequence control capability. This can be applied to active power filters or neutral current compensator applications for compensating harmonics and zero sequence. Four-leg converters have voltage vectors with γ component different from zero leading to the use of 3-D representations.

A generalized 3D-SVM algorithm with low computational cost for four-leg multilevel converters was proposed in [85]. This 3-D algorithm is a generalization of that proposed in [84]. Compared with [84], as the topology changes, the state-space vectors of the converter also change. However, once the sub-cube is known, almost all the necessary calculations to determine the switching sequence and the duty cycles are exactly the same. This 3D-SVM technique optimizes the switching sequence, minimizing the number of commutations for 4L-4W converters. As for the 3L-3W case, the low computational cost of this method is always the same, and it is independent of the number of levels of the converter.

In general, one of the advantages of SVM techniques for multilevel converters is the reduction of computation and implementation complexity compared to carrier-based PWM algorithms because the number of carriers does not increase as the number of converter levels increases. This advantage makes the digital implementation of the algorithms easier. In addition, the vector redundancies and the switching sequences can be used for other control purposes and can be designed according to a specific criterion depending on the application. It has to be noticed that in order to achieve a proper time average, the modulation period T_s is small, leading to high switching frequencies, comparable to carrier-based PWM (above $1\,kHz$), and therefore not useful for very high-power applications.

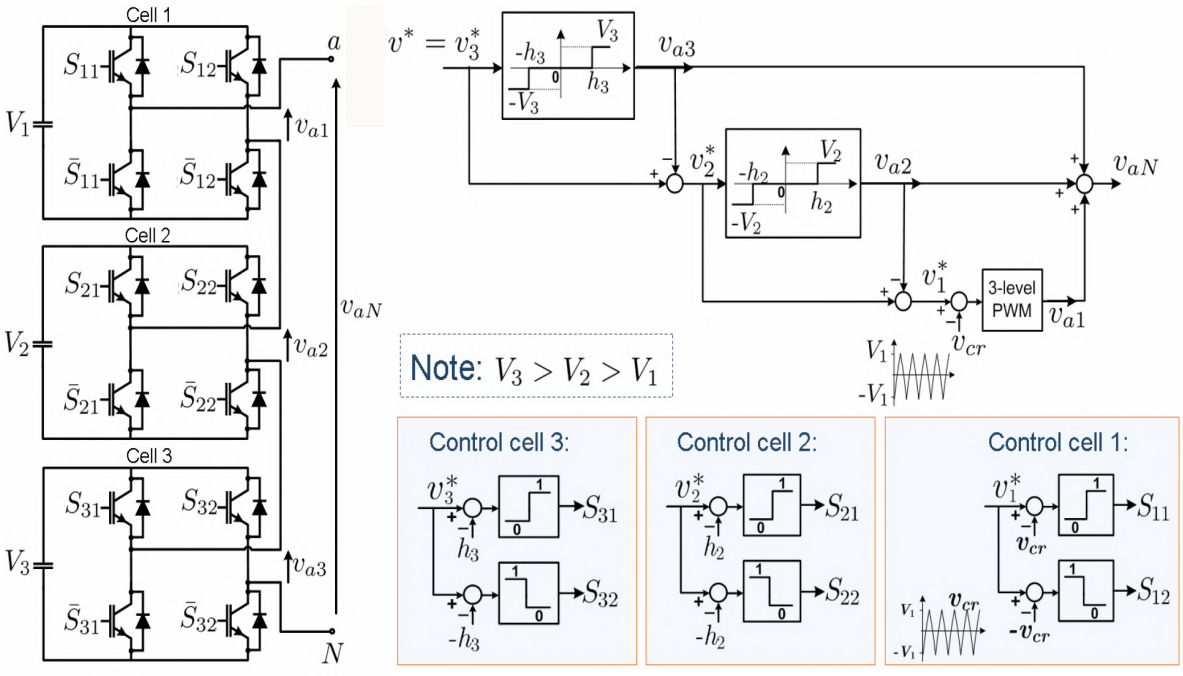


Figure 4.13: Hybrid modulation operating principle for 3-cell CHB with unequal dc sources [6].

4.6 Hybrid PWM Modulation (H-PWM)

Hybrid PWM (H-PWM) is an extension of PWM for CHB with unequal dc sources [109]. The main challenge is to reduce the switching losses of the converter by reducing the switching frequency of the higher power cells. Therefore, instead of using high frequency carrier-based PWM methods in all the cells, the high-power cells are operated with square waveform patterns, switched at low frequency, while only the small power cell is controlled with unipolar PWM.

Consider, for example, a three-cell (in each phase) CHB inverter with $V_1 < V_2 < V_3$ as the three unequal dc source voltage values. Then, the square wave operation for cell 3 can be obtained by simply comparing the reference to $\pm h_3 = (V_1 + V_2)$, as shown in the control diagram in Fig. 4.13. The output of this comparator indicates if this cell is generating $-V_3$, zero, or V_3 at the output. Considering a sinusoidal reference, the generated output voltage for cell 3 using this comparator is shown in Fig. 4.14(a), switching at fundamental frequency (each switch has a turn-on and turn-off during one cycle). The difference between the reference v^* and this output v_{a3} is the error or the unmodulated part of the reference, which is left for modulation to the other two cells. Hence, this difference can then be used as reference for cell 2.

Again, a comparator $\pm h_3 = \pm V_1$ is used to generate the output of cell 2 (note that, in general, the comparator level for cell k is $h_k = V_{k-1} + V_{k-2} + \cdots + V_1$, i.e., the sum of

the smaller dc sources (to avoid overmodulating references for the smaller cells). For example, the output waveform in Fig. 4.14(b) is obtained, with few commutations per cycle. In the same way as with cell 3, the square wave operation of cell 2 is a gross approximation of its reference; therefore this new error (difference between v_2^* and v_{a2}) becomes the reference for the last cell. Since there are no more cells left, and this is the one with the lowest power, the square waveform operation is replaced by traditional unipolar PWM, as shown in the control diagram of Fig. 4.13. The reference and output of cell 1 is given in Fig. 4.14(c).

The series connection of the cells delivers a total output voltage $v_{aN} = v_{a1} + v_{a2} + v_{a3}$, as the one illustrated in Fig. 4.14(d), which looks like a traditional high-frequency PWM multilevel waveform pattern, while in fact only the low-power cell is operating at higher switching frequencies, improving the converter efficiency. This method is only feasible if the dc-link voltages of the higher power cells are integer multiples of the small one, and $V_3 \leq 2\,(V_1 + V_2)$ and $V_2 \leq 2V_1$; otherwise overmodulation in the small power cell will occur. The optimal asymmetry that fulfills these conditions for a three-cell inverter is $V_1 \colon V_2 \colon V_3 = 1 \colon 2 \colon 6$ and is the example shown in Fig. 4.14, leading to 19 different voltage levels).

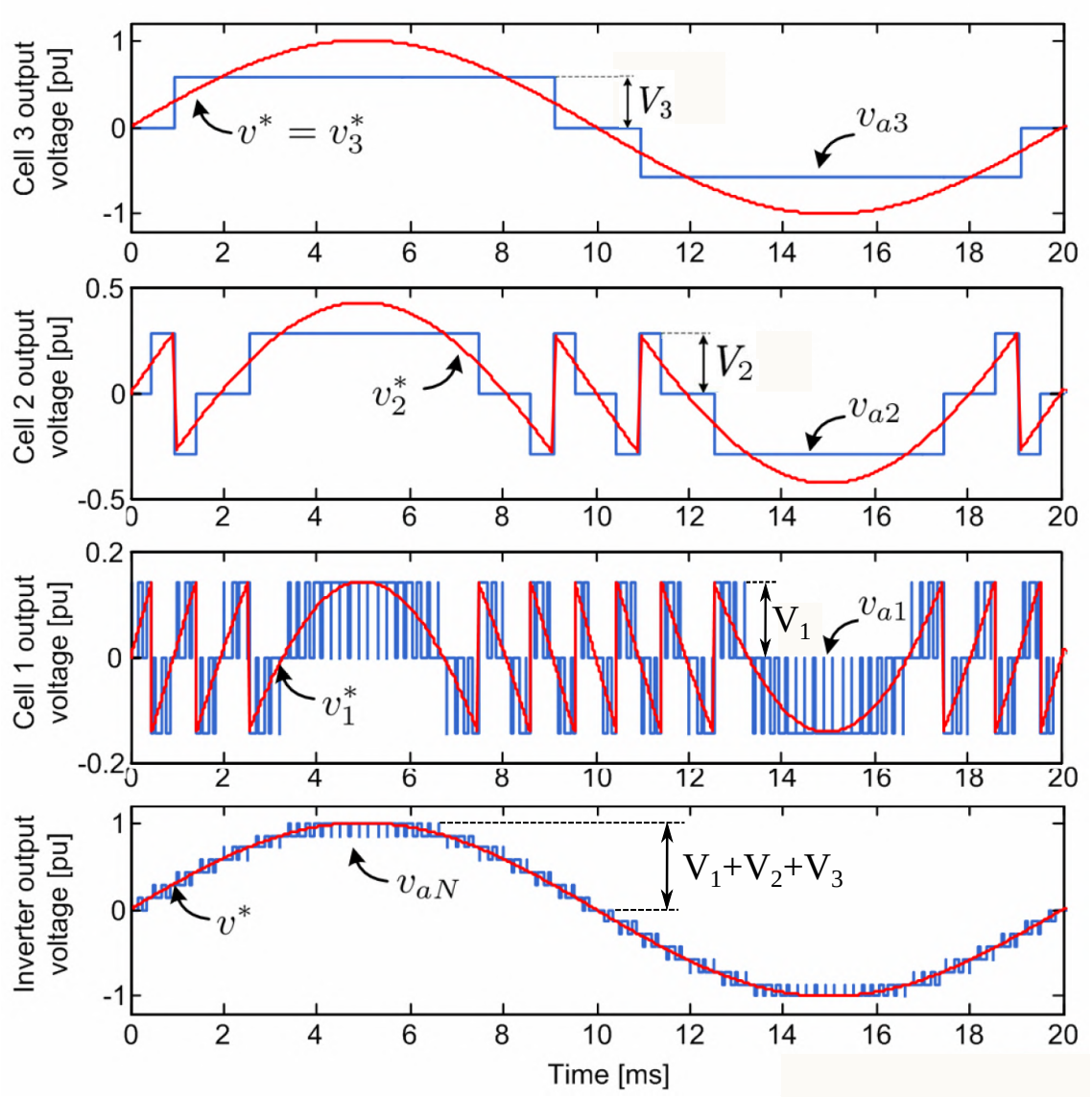


Figure 4.14: Output voltages for CHB with unequal dc sources for hybrid modulation [6].

4.7 Space or Nearest Vector Control (NVC)

A conceptually different modulation control method for multilevel inverters, based on the space-vector theory, is nearest vector control (NVC), which is also known as space vector control (not to be confused with the motor drive control technique with the same name). It was introduced in [92] as staircase modulation to provide a low switching frequency modulation method, with good dynamic performance. This control strategy works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval, as is the principle

of SVM.

The basic idea is to take advantage of the high number of voltage vectors generated by a multilevel converter by simply approximating the reference to the closest voltage vector that can be generated in the α–β plane, without even need of modulation. Therefore, this method is referred to as nearest vector control instead of modulation, since no time average approximation of the reference is performed. So, it is unnecessary to use a more complex modulation scheme involving the three vectors adjacent to the reference.

This operating principle is shown in Fig. 4.15, where the 311 different state-space vectors generated by an 11-level multilevel inverter are illustrated, with a zoom to the NVC operating principle. Each dot is one of the possible voltage vectors generated by the inverter; they are surrounded by hexagons that represent the boundary of the area in which they are the closest available vector. The red dashed line is the voltage space vector reference(v_s^*) trajectory through the complex plane. Hence, when the reference falls into a certain hexagon, the corresponding vector will be generated by the inverter. The selected vectors according to the illustrative example in Fig. 4.15 are highlighted in blue.

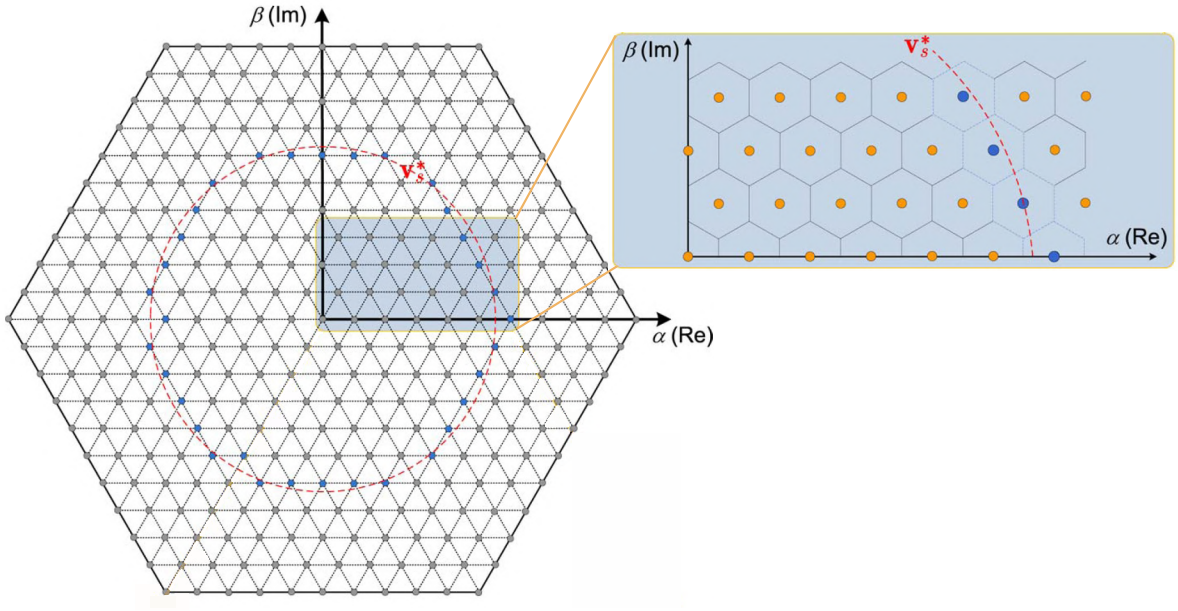


Figure 4.15: Multilevel nearest vector control operating principle [6].

Fig. 4.16 presents the voltage generated by one phase-leg in an eleven-level CHB inverter with five cells per phase and an output frequency of 50 Hz.

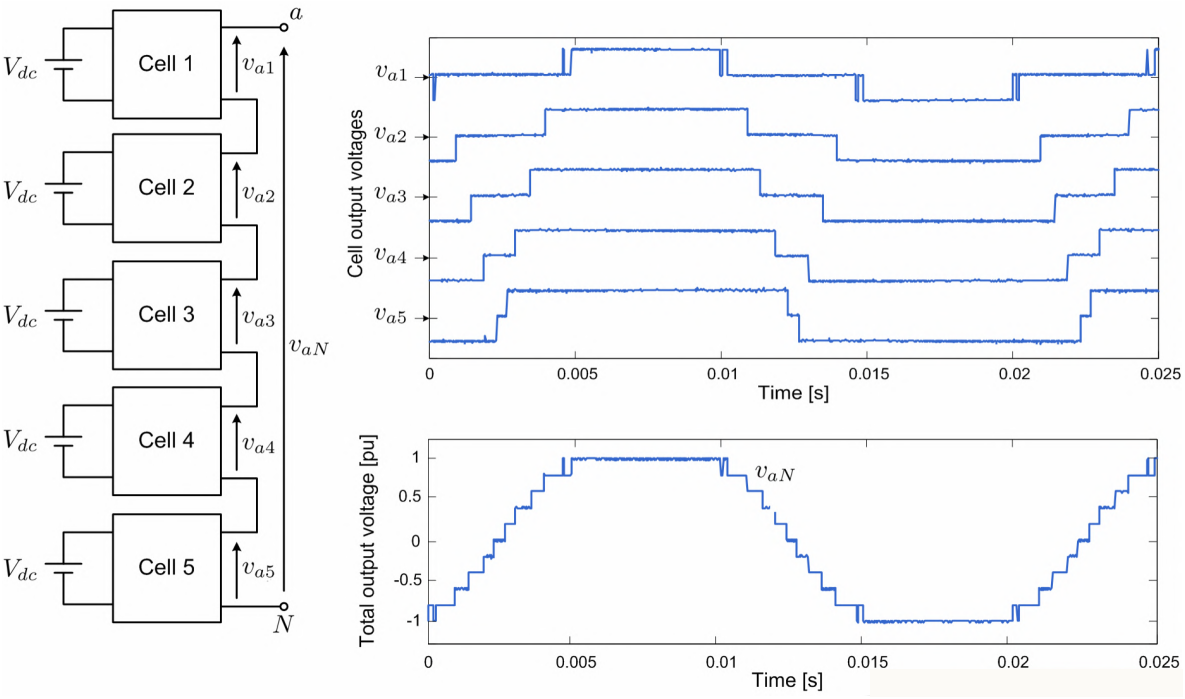


Figure 4.16: Voltages generated by an 11-level CHB inverter with NVC [6].

The natural selection of the closest vector produces a strong reduction in the number of commutations, since no commutations are forced by a modulator, reducing in this way the switching losses. This method, however, does not eliminate low-order harmonics (like SHE) and, due to its inherent low and variable switching frequency nature, can introduce low-order harmonics in the load voltage. This can be compensated by using multilevel converters with a high number of levels (usually above seven), which have a more dense state-space vector availability, resulting in a better vector approximation and smaller error. They also have an intrinsic low THD due to the small dv/dt, reducing the effect of the low-order harmonics. An alternative method that also reduces the common-mode voltages is presented in [93].

These methods have very simple operating principles; however, the implementation is not as straightforward, since an algorithm capable of finding numerically the closest vector needs to be programmed. This technical issue can be found in detail in [92] and [93].

4.8 Nearest Level Control (NLC)

The nearest level control (NLC), also known as the round method, is somehow the per-phase time-domain counterpart of NVC [94], [110]. Basically, the same principle is applied but to voltage levels instead of space vectors, thus selecting the nearest voltage level that can be generated by the inverter to the desired output voltage

reference. Unlike with SVC, where the three phases were controlled directly with the vector selection, here the three phases are controlled independently with their respective 120° phase-shifted references. The main advantage is that the algorithm is greatly simplified in relation to NVC, since it is much easier to find the closest level than the closest vector. In fact, the output voltage level selection is reduced to a unique simple expression per phase

$$\text{closest voltage level} = v_{aN} = V_{dc} \times f_{round} \tag{4.4}$$

where V_{dc} is the voltage difference between two levels (usually the dc-link voltage in CHB), which is used to normalize the phase output voltage reference v_s^*. The normalized value is then evaluated using the round function (or nearest integer function), which is defined such that $f_{round}\{x\}$ is the integer closest to x. Since this definition is ambiguous for half-integers, the additional convention is that half-integers are always rounded to even numbers, for example, $f_{round}\{1.5\} = 2$. This nearest integer multiplied by V_{dc} corresponds to the closest voltage level to the reference, and thus is generated by the inverter.

The operating principle is illustrated in Fig. 4.17(a) for the first quarter-cycle of a sinusoidal reference. Note that the maximum approximation error is $V_{dc}/2$. The implementation of the nearest voltage level generation is presented in Fig. 4.17(b). As can be seen in Fig. 4.17(a), the round function inherently produces only one commutation between two voltage levels and a maximum dv/dt of V_{dc}, unless the reference presents large step changes.

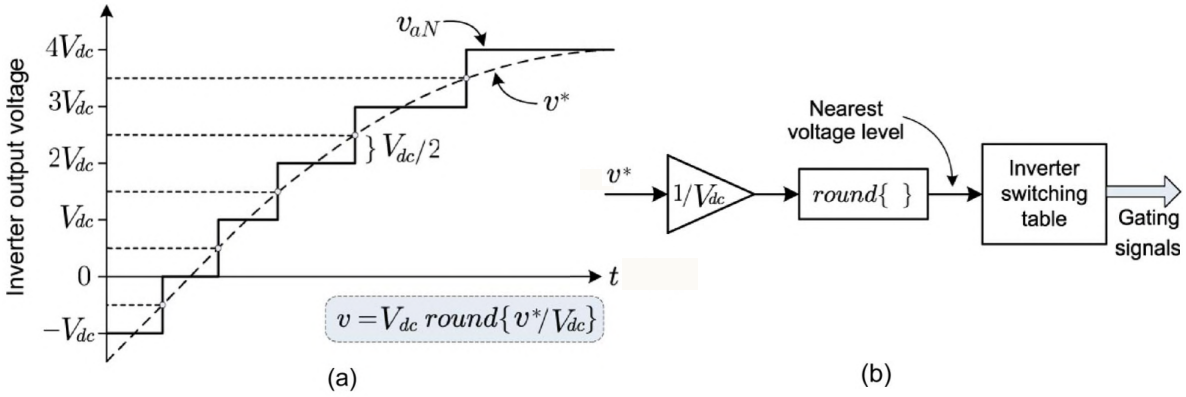


Figure 4.17: Nearest level selection: (a) waveform synthesis and (b) control diagram [88].

It is worth mentioning that this method is not a modulation technique, since there is no reference tracking by time average synthesis between two levels. Instead, the stepped waveform is generated as an approximation to the reference. Although the voltage waveform is very similar to the one obtained with staircase modulation, it does not eliminate specific harmonics because it is not really a modulation. There-

fore, this control method, like NVC, is not effective for converters with a reduced number of levels, since the approximation error becomes relevant. Hence it is aimed to be used in converters with a high number of levels to avoid important low-order harmonics at the ac side. The main advantage is its conceptual and implementation simplicity and the efficiency achieved with this method. An adaptive modulation method that solves this problem by introducing a duty-cycle calculation to NLC has been proposed [111], at the expense of a more advanced control algorithm.

It is also worth mentioning that there are other control algorithms that select the switching state and switching times of multilevel converters but are not a modulation or control stage dedicated to the converter; instead they are a direct consequence of the overall system controller. This is the case of direct torque control of ac motors, where the switching states and transitions are directly obtained from the torque and flux controller of the motor [112, 113]. Another method where the switching states and switching times are directly computed by the controller is finite control set model predictive control, which also has been applied to multilevel converters [114].

4.9 Selective Harmonic Elimination (SHE) Technique and Computation Methods

Converters for very high-power applications are usually controlled with low switching frequency algorithms, below $1\,kHz$. If traditional carrier-based PWM methods were used reducing the carrier frequency to these levels, low-order harmonics would appear in the output voltage, increasing distortion, which consequently will translate into performance problems. Selective harmonic elimination (SHE) is a low switching frequency PWM method developed for traditional converters in which a few (generally from three to seven) switching angles per quarter fundamental cycle are predefined and precalculated via Fourier analysis to ensure the elimination of undesired low-order harmonics [106]. Basically, in SHE, the Fourier coefficients or harmonic components of the predefined switched waveform with the unknown switching angles are made equal to zero for those undesired harmonics, while the fundamental component is made equal to the desired reference amplitude. This set of equations is solved offline using numerical methods, obtaining a solution for the angles.

This concept has also been extended for multilevel waveforms [89, 95, 96, 190]. The basic idea is kept, i.e., a previously defined voltage waveform with a fixed number of switching angles, like the one in Fig. 4.18, is generated by the converter. By precalculating appropriately these switching angles, a number of undesired low-order harmonics can be eliminated in the output voltage. With m switching angles in a quarter-cycle, m control degrees of freedom are obtained, from which $m-1$ can be used to eliminate undesired harmonics and the last one to control the amplitude

of the fundamental component for reference tracking. As with traditional SHE, this can be achieved by computing the corresponding Fourier coefficients of the predefined waveform with the switching angles as unknown variables

$$h_n = \frac{4V_{dc}}{n\pi} \sum_{k=1}^{m} \cos\left(n\alpha_k\right) \tag{4.5}$$

where h_n is the amplitude of harmonic n. Note that the switching angles within the quarter-period are constrained as

$$0 < \alpha_1 < \alpha_2 \ldots < \alpha_m < \pi/2. \tag{4.6}$$

It should be noted that, the corresponding Fourier coefficients for three-level waveforms as illustrated in Fig. 4.19 is as follows:

$$h_n = \frac{4V_{dc}}{n\pi} \sum_{k=1}^{m} (-1)^{k-1} \cos\left(n\alpha_k\right) \tag{4.7}$$

The harmonics that should be eliminated are set to zero. The set of equations is then solved using numerical methods several times to cover a wide range of modulation indexes (amplitudes for the fundamental component). The solutions (angles) are stored in a lookup table, which is then used to modulate the converter. As an example for a three-level converter, like the NPC, a typical waveform considering three switching angles $(\alpha_1, \alpha_2, \alpha_3)$ is given in Fig. 4.19. The corresponding Fourier series is given by

$$v_{aN} = \frac{4V_{dc}}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \left\{\cos\left(n\alpha_1\right) - \cos\left(n\alpha_2\right) + \cos\left(n\alpha_3\right)\right\} \times \sin\left(n\omega t\right). \tag{4.8}$$

From this equation, three coefficients of the Fourier series can be forced to a desired value. Naturally, the first coefficient corresponds to the fundamental component and is set to the desired modulation index, while usually the fifth and seventh coefficients are set to zero (for fifth and seventh harmonic elimination)

$$\begin{aligned} \tfrac{M\pi}{4} &= \cos\left(\alpha_1\right) - \cos\left(\alpha_2\right) + \cos\left(\alpha_3\right) \\ 0 &= \cos\left(5\alpha_1\right) - \cos\left(5\alpha_2\right) + \cos\left(5\alpha_3\right) \\ 0 &= \cos\left(7\alpha_1\right) - \cos\left(7\alpha_2\right) + \cos\left(7\alpha_3\right) \end{aligned} \tag{4.9}$$

where M is the modulation index.

The third harmonic and its multiples are usually not eliminated using SHE, since they are naturally eliminated by the three-phase load connection. Fig. 4.20 shows the angles obtained for this example, the implementation diagram, and the output voltage with its corresponding spectrum, from which can be appreciated that the fifth and seventh harmonic are effectively eliminated.

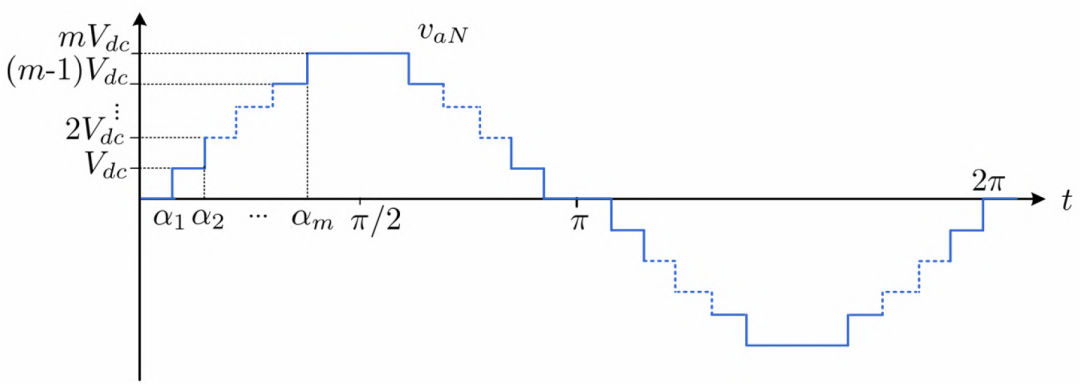


Figure 4.18: Multilevel selective harmonic elimination.

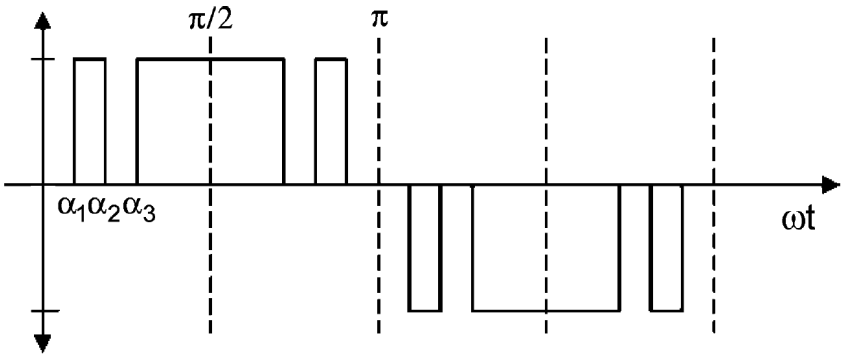


Figure 4.19: Three-level selective harmonic elimination.

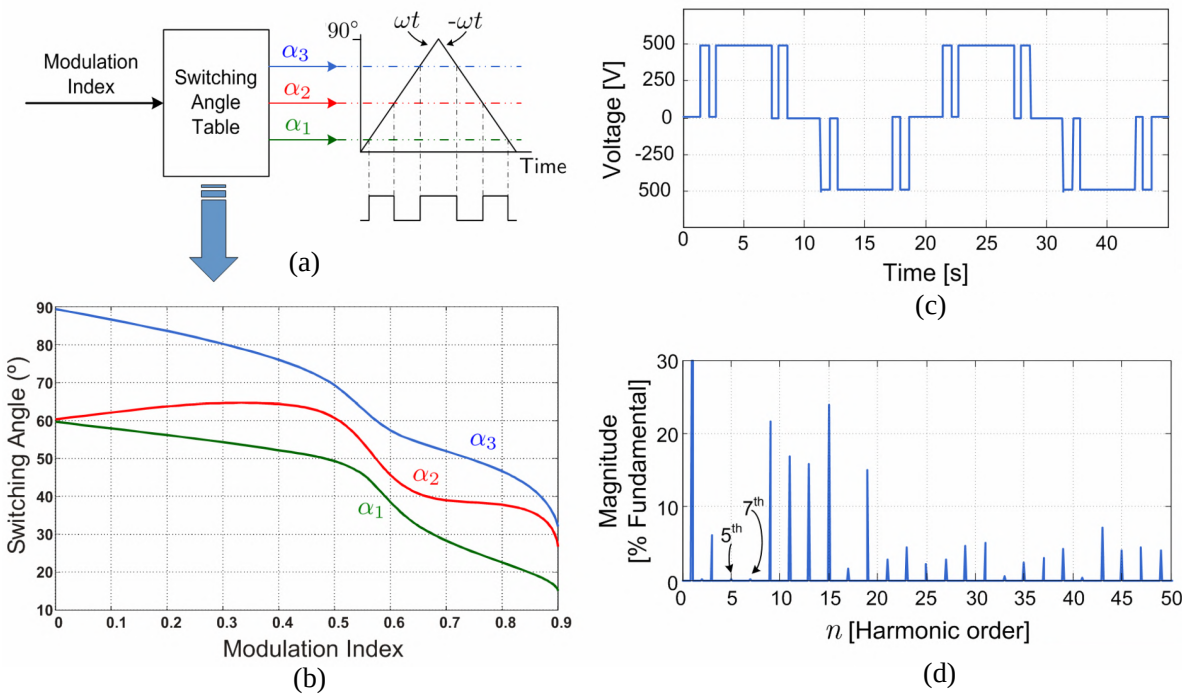


Figure 4.20: Three-level selective harmonic elimination: (a) implementation diagram, (b) angles solution, (c) output voltage, and (d) output voltage spectrum [6].

Note that there is no control over the non-eliminated harmonics, which usually tend to increase, since the eliminated harmonic energy present in the switched waveform is redistributed over the other ones. If these harmonic levels are not suitable for a particular application, additional angles can be introduced, eliminating more harmonics. For high power grid connected converters, there are very demanding grid codes making necessary several angles, which increases the switching frequency and losses or introduces the use of additional filters. In this case, a variation on SHE called selective harmonic mitigation technique (SHM) is more suitable. The main difference with SHE is that it does not force the angles to completely eliminate the harmonics by setting them to zero. Instead, inequalities are used to limit the harmonic content to acceptable values [222]. In this way, the harmonic spectrum of the obtained waveforms can fulfill current grid code regulations for the integration of energy systems into the distribution grid. The great advantage of SHM compared with SHE is the reduction (or even elimination) of the necessary grid connection filters, without sacrificing the power quality of the system. This leads to a reduction of the economical cost, volume, and weight of the overall power system.

For converters with a higher number of levels, like CHB, SHE is also known as staircase modulation because of the stair-like shape of the voltage waveform. The basic idea is identical to SHE; the difference is that each angle is associated to a particular cell. The operating principle of this technique is to connect each cell of the

inverter at specific angles to generate the multilevel output waveform, producing only a minimum of necessary commutations [107]. The operating principle is illustrated in Fig. 4.21; note that only one angle needs to be determined per power cell. These angles can be computed using the same principles of SHE exposed before. In these waveforms, it is possible to note that there is a high difference among the conducting times, which produces an unbalanced power distribution. If a multipulse transformer is used, this power unbalance can lead to a distorted input current. In [115], this effect is reduced by a simple change of conducting angles. This modulation technique can be applied to symmetrical inverters when the number of output voltage levels is high or when the inverter has non equal dc links [116].

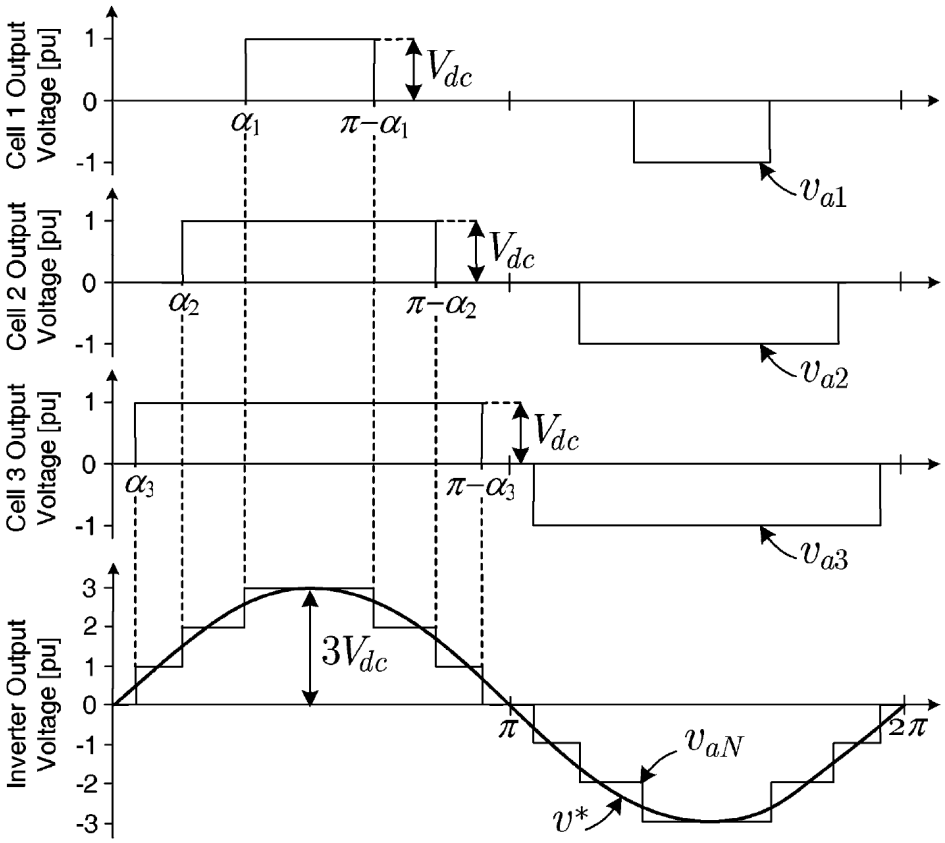


Figure 4.21: Seven-level staircase modulation for CHB (One angle per voltage level).

The second approach is to combine the original SHE with the multilevel version [117] as it can be seen on the waveform of Fig. 4.22 where there are several switching angles per voltage level. In this case, the number of harmonics eliminated is independent from the number of output voltage levels, and the switching frequency is higher than the fundamental. It is possible to note that there are several different possibilities to synthesize the output voltage, allowing a further optimization in terms of switching frequency. In Fig. 4.22, the seq.1 produces a high switching frequency in cell 2 but

a fundamental switching frequency in cell 1. Alternatively, seq.2 produces the same output voltage, but each cell has the same switching frequency.

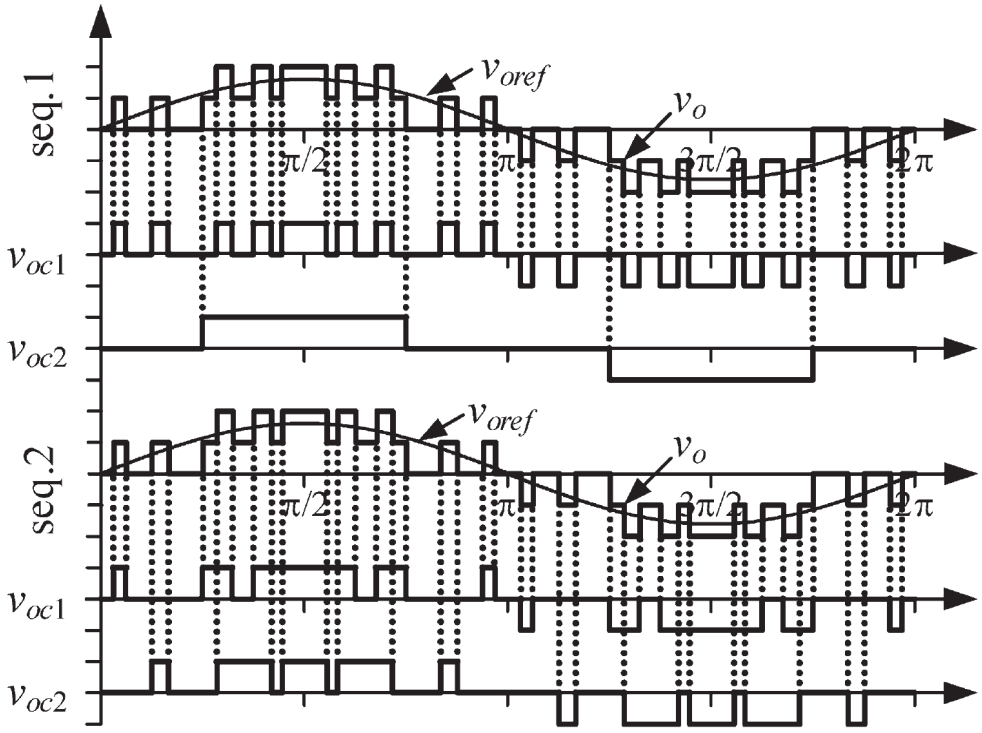


Figure 4.22: Five-level SHE technique for CHB (multiple angles per voltage level) [18].

The main advantage, like in SHE, is that the converter switches very few times per cycle, reducing the switching losses to a minimum. In addition, low-order harmonics are eliminated, facilitating the reduction of output filter volume, weight, and cost.

All these methods require numerical algorithms to solve this set of equations, which are performed for several modulation indexes, leading to important calculations that are impossible to run in real time with current microprocessors and thus are executed offline. Therefore, the solutions are stored in lookup tables, and interpolation is used for those unsolved modulation indexes. This makes SHE-based modulation algorithms not suitable for applications demanding high dynamic performance.

As an alternative to SHE, other low-switching-frequency modulation schemes have been proposed, such as selective harmonic mitigation (SHM) schemes [118], [222] and synchronized optimum PWM techniques [119, 120, 206]. These two techniques require important offline computations such as SHE, and the computations over proportionally increase with a higher number of levels. However, once the formulation of the equations and the numerical solving have finished, the results only need to be

stored in lookup tables in the digital interface control board. These methods have the same drawback as SHE, i.e., variable-speed operation in closed-loop operation will require a low bandwidth control loop, with the consequent low dynamic performance. SHM differs from SHE in the fact that the harmonic is not fully eliminated; instead, some content is allowed up to the grid code limits, which enables to control more harmonics with the same amount of angles (commutations). In this way, SHM achieves a reduced THD, which is in compliance with the grid code, whereas SHE fully eliminates low-order harmonics, which usually moves harmonic energy to the higher frequencies, increasing their amplitude even over grid code limits.

SHE has extensively been analyzed for a wide variety of converter topologies [76, 95, 117, 121, 193]. Recently, real-time (online) SHE methods have been proposed based on the total THD minimization rather individual harmonic analysis [122, 123]. Although the online part is an attractive feature, the fact that the overall THD is considered does not give any warranty that grid codes are always met, irrespective of the modulation index and operating condition. In fact, the THD could be minimized at the expense of having all the harmonic energy in the low-order harmonics. In [124], a predictive-control-based SHE method has been proposed, which is also performed online but considers the amplitude of each harmonic in real time due to a sliding discrete Fourier transform. A predictive model is used to select the switching state that minimizes all the desired harmonics. The predictive model, together with the sliding discrete Fourier transform, allows using this modulation method on closed-loop operation with higher dynamic performance capability.

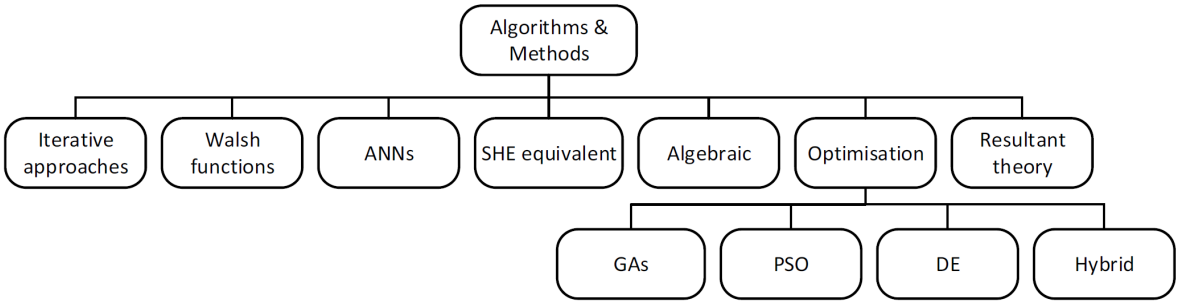


Figure 4.23: Classification of SHE-PWM algorithms and solving techniques [76].

4.10 Summary

In this chapter, the various modulation methods has been presented for multilevel converters. Level Shifted PWM (LS-PWM), kinds of Phase Shifted PWM (PS-PWM), Space Vector Modulation (SVM), Hybrid PWM, Nearest Vector and Nearest Level Control modulation (NVC and LVC), and selective harmonic elimination modulation were studied and their advantages and disadvantages were also expressed in this chapter.

5 Innovative Modulation Techniques for Multilevel Converters (MLC)

5.1 Overview: The power Quality Issue

Static power converters utilize power semiconductor devices for power conversion from AC to DC, DC to DC, DC to AC and AC to AC; and constitute the largest nonlinear loads connected to the electric power systems. These converters are used for various purposes in the industry, such as adjustable speed (or variable frequency) drives, uninterruptible power supplies, switch-mode power supplies etc. These static power converters used in a variety of applications draw non-linear (i.e. non-sinusoidal) currents and distort the supply voltage waveform at the point of common coupling (PCC). The PCC is a point between the system owner or operator and a user. The PCC is usually taken as the point in the power system closest to the user where the system owner or operator could offer service to another user. Frequently for service to industrial users (i.e., manufacturing plants) via a dedicated service transformer, the PCC is at the HV side of the transformer. For commercial users supplied through a common service transformer, the PCC is commonly at the LV side of the service transformer. In general, The PCC is a point on a public power supply system, electrically nearest to a particular load, at which other loads are, or could be connected and is located on the upstream of the considered installation. A single line diagram of the PCC connection in shown in Fig. 5.1.

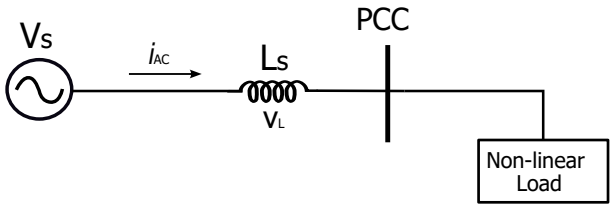


Figure 5.1: Single line diagram of power distribution system

The voltage at the PCC, v_{PCC} can be obtained by subtracting the voltage drop (v_L) across the system impedance due to the flow of non-linear current i_{AC}:

$$v_{PCC} = (v_S - v_L) = \left\{ v_S - L_S \frac{d(i_{AC})}{dt} \right\} \tag{5.1}$$

These non-sinusoidal quantities (voltages and currents) can be divided into sinusoidal components, the fundamental frequency (i.e. 50 or 60 Hz) component and the harmonic components.

Fig. 5.2 shows the distortion in the waveform of v_{PCC} due to the flow of non-linear current through the finite system impedance when only the third order harmonic is considered.

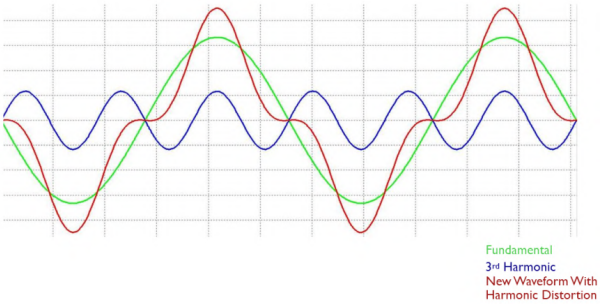


Figure 5.2: Harmonic distortion considering only the 3rd harmonic

The amount of distortion in the voltage or current waveform is quantified by means of an index called the total harmonic distortion (THD). According to IEEE 519-1992 [318], it is defined as a ratio of the root-mean-square of the harmonic content to the root-mean-square value of the fundamental quantity and expressed as a percent of the fundamental.

$$THD\% = \frac{\sqrt{\sum_{n=1,3,5,\ldots}^{\infty} v_n^2}}{v_1} * 100 \tag{5.2}$$

Typically, the harmonics up to the 50th order are used to calculate the %THD, however, the harmonic components of order greater than 50 may be included when necessary.

Nowadays, the harmonic distortion is the major problems in the electrical systems because of the several undesirable effects which are strictly related to the harmonic presence in the power grid. Typical examples ares huge power losses, high electromagnetic interferences and pulsating torque in AC motor drives. For this reason, in all industrial and consumer applications it is required to minimize the total energy consumption, improve efficiency and enhance the power quality [320].

Generally, at any point of common coupling (PCC), the measured value of total harmonic voltage distortion should not exceed 5% and that of any individual harmonic voltage distortion should not exceeding 3% of the fundamental value of the line voltage. Normally, in typical applications, the harmonics are measured up to 25th order, but in critical applications, those are measured up to 50th or 100th order.

In order to minimize the harmonic content of the output voltage and current of power converters, it is possible to act on their switching modulation patterns. In MC topologies, because of the several degrees of freedom offered by multilevel structures, the harmonic minimization procedure can be very effective . In particular, a low switching frequency modulation allows to limit the power converter switching losses and at the same time to carries out a high quality output waveform eliminating or/and mitigating low order harmonics.

Among all the multilevel converters structures presented in chapter 3, cascaded multilevel inverter (CHB) is the one which allows to reach the higher output voltage and higher power levels and reliability using only commercial low voltage components. The high modularity degree of these topology allows, in the case of a fault in one of its modules, to replace it quickly and easily. Moreover, with an appropriated control strategy, it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability [308, 309, 310, 311, 312, 313]. Multilevel converters (MC) are becoming very important because a high number of industrial applications require medium voltage and megawatt power apparatus and for these applications two level converters are not suitable [314, 315, 316, 317]. Moreover, MC present many advantages such as low distortion output voltage, dv/dt stresses reduction, semiconductor switches stresses reduction and common mode voltage reduction.

In chapter 4 was presented the state of the art of the modulation techniques for MC, introducing also some fundamental frequency modulations such as the selective harmonic elimination (SHE). In the next sections of this chapter, several modulation algorithm for the harmonic elimination and/or mitigation in MC will be described, introducing some innovative approaches to the problem and highlighting their advantages in comparison with the most well-known modulation techniques.

5.2 Mixed Harmonic Elimination and Reduction Technique for Single Phase Nine Level Converters

5.2.1 Introduction

The goal of this modulation technique is to carries out a high quality output waveform eliminating or/and mitigating low order harmonics [232]. The switching angles are obtained through the solution of a set of nonlinear transcendental equations. Many algorithms have been proposed in literature to solve these equations. These algorithms include iterative approaches, such as the Newton-Raphson method [233]. Another approach uses Walsh functions [8] solving linear equations, instead of non-linear transcendental equations, to find the switching angles. Optimization methods are also used based on the concept of ant colony [9] and on general genetic algorithm [10]. Hybrid genetic algorithm was applied to multilevel converters with equal and non-equal DC sources in [11]-[13]. Particle swarm optimization (PSO) technique was adopted for selective harmonic elimination (SHE) for fundamental switching output multilevel waveforms with equal [14]-[16] and non-equal DC sources [17]. In [18] a five level cascaded inverter with unequal DC sources is considered and SHE technique based on the graphical separation of functions zeros, is used to reduce total harmonic distortion in the inverter output waveform. In the paper [321] we proposed a procedure, working at fundamental frequency for a single phase nine level converter, shown in Fig. 5.3, able to carry out switching angles that:

- Eliminate third and all odd multiple of the third harmonic.
- Minimize the total harmonic distortion (THD).

The procedure assumes that the four DC voltages are equal, but variable. The obtained switching angles and THD don't depend on modulation index.

5.2.2 Mathematical Model

The Fourier decomposition of voltage waveform with quarter-wave symmetry, as the output voltage of 9-level inverter shown in Fig. 5.3, can be expressed as:

$$V_{out} = \sum_{n=1,3,5,\ldots}^{\infty} H_n \sin(n\omega t) \tag{5.3}$$

where H_n is the Fourier coefficient and indicates the amplitude of n-th voltage harmonic order:

$$H_n = \frac{4}{n\pi} \sum_{i=1}^{4} V_i cos(n\alpha_i) \tag{5.4}$$

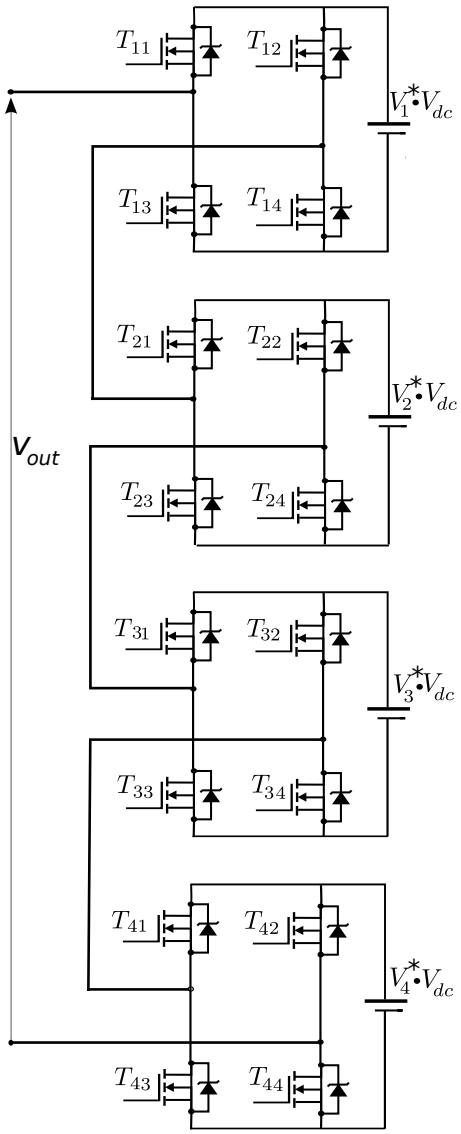


Figure 5.3: 9-level single phase inverter.

The proposed procedure starts from a mathematical system that:

- sets to zero the third and all odd multiple of the third harmonic
- imposes the mitigation of low order harmonics.

Introducing the p. u. quantities, the following system can be defined:

$$\begin{cases} \sum_{i=1}^{4} V_i^* cos\left(\alpha_i\right) = 4m \\ \sum_{i=1}^{4} V_i^* cos\left(3k\alpha_i\right) = 0 \quad k = 1, 3, 9, ... \\ \frac{1}{4n}\sum_{i=1}^{4} V_i^* cos\left(n\alpha_i\right) \leq mL_n \quad n = 5, 7, ... \end{cases} \tag{5.5}$$

where $V_i^* = \frac{V_i}{V_{dc}}$; $m = \frac{\pi H_1}{16 V_{dc}}$ is the modulation index, L_n are the wished levels (in percentage to the fundamental) for odd non-triple harmonics. Assumed that the voltages $V_1^* = V_2^* = V_3^* = V_4^* = V^*$ depending on a positive coefficient C, such that $V^* = Cm$ the previous system can be written as

$$\begin{cases} V^* \left[\cos\left(\alpha_1\right) + \cos\left(\alpha_2\right) + \cos\left(\alpha_3\right) + \cos\left(\alpha_4\right)\right] = 4m \\ V^* [\cos\left(3k\alpha_1\right) + \cos\left(3k\alpha_2\right) + \cos\left(3k\alpha_3\right) + \\ + \cos\left(3k\alpha_4\right)] = 0 \\ V^* [\cos\left(n\alpha_1\right) + \cos\left(n\alpha_2\right) + \\ + \cos\left(n\alpha_3\right) + \cos\left(n\alpha_4\right)] \leq 4nmL_n \end{cases} \tag{5.6}$$

$k = 1, 3, 9, ...$ $\quad$ $n = 5,\ 7,\ 11, ...$

The switching angles α_1,..., α_4 have to satisfy the following conditions

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \frac{\pi}{2}. \tag{5.7}$$

From (5.6), it is possible to observe that

$$\frac{1}{k}\left|\frac{\cos\left(k\alpha_1\right) + \cos\left(k\alpha_2\right) + \cos\left(k\alpha_3\right) + \cos\left(k\alpha_4\right)}{\cos\left(\alpha_1\right) + \cos\left(\alpha_2\right) + \cos\left(\alpha_3\right) + \cos\left(\alpha_4\right)}\right| \leq L_k \tag{5.8}$$

$k = 5,\ 7,\ 11,\ ...$

$$C = \frac{4}{\cos\left(\alpha_1\right) + \cos\left(\alpha_2\right) + \cos\left(\alpha_3\right) + \cos\left(\alpha_4\right)} \tag{5.9}$$

To solve the second equations of (5.6), the proposed procedure sets to zero the

following pairs of cosines

$$\begin{cases} \cos(3\alpha_1) + \cos(3\alpha_3) &= 0 \\ \cos(3\alpha_2) + \cos(3\alpha_4) &= 0 \end{cases} \tag{5.10}$$

Applying Prosthaphaeresis formulas, it is possible to obtain

$$\begin{cases} 2\cos\left(\frac{3}{2}(\alpha_1+\alpha_3)\right)\cos\left(\frac{3}{2}(\alpha_1-\alpha_3)\right) &= 0 \\ 2\cos\left(\frac{3}{2}(\alpha_2+\alpha_4)\right)\cos\left(\frac{3}{2}(\alpha_2-\alpha_4)\right) &= 0 \end{cases} \tag{5.11}$$

Since $\cos\left(\frac{3}{2}(\beta \pm \gamma)\right) = 0$ when $\beta \pm \gamma = \frac{\pi}{3} + \frac{2}{3}r\pi$, $r = 0, \pm1, \pm2, ...$, the switching angles representing the solutions of (5.10), satisfy the following conditions

$$\begin{cases} \alpha_1 + \alpha_3 = & \frac{\pi}{3} \\ \alpha_4 - \alpha_2 = & \frac{\pi}{3} \end{cases} \tag{5.12}$$

Previous conditions allow to eliminate third and odd triple harmonics, as demonstrate in Appendix.

By applying Prosthaphaeresis formulas and equations (5.12), (5.8) can be rewritten as

$$\frac{1}{k}\left|\frac{\cos\left(k\left(\alpha_1 - \frac{\pi}{6}\right)\right) + \cos\left(k\left(\alpha_2 + \frac{\pi}{6}\right)\right)}{\cos\left(\alpha_1 - \frac{\pi}{6}\right) + \cos\left(\alpha_2 + \frac{\pi}{6}\right)}\right| \leq L_k \tag{5.13}$$

$k = 5, 7, 11, ...$

Introducing the new variables

$$\begin{cases} \alpha = \alpha_1 - \frac{\pi}{6} \\ \beta = \alpha_2 + \frac{\pi}{6} \end{cases} \tag{5.14}$$

the following inequality is obtained

$$\frac{1}{k}\left|\frac{\cos(k\alpha) + \cos(k\beta)}{\cos(\alpha) + \cos(\beta)}\right| \leq L_k \qquad k = 5, 7, 11, ... \tag{5.15}$$

It represents a set of inequality of two variables.

5.2.3 Proposed Procedure

To obtain the angles α and β satisfying the previous set of inequality in the form (5.15) is difficult. For this reason a simple procedure based on the least squares method (LSM) is applied. It minimizes the sum of the square values of the errors (differences between harmonics amplitude and zero). This means minimize the THD^2. The procedure finds all valid pairs (α, β) that return relative minimum $THD^2\,(\alpha,\,\beta)$ values and between them it chooses the pair that returns the smallest value.

The square value of THD to minimize is

$$THD^2\,(\alpha,\,\beta) = \sum_{k=5,\,7,\,11,\,13,\,\ldots} \left[\frac{1}{k}\frac{\cos\,(k\alpha)+\cos\,(k\beta)}{\cos\,(\alpha)+\cos\,(\beta)}\right]^2 \tag{5.16}$$

It is possible to observe that the THD is independent on the modulation index and on V^*.

The stationary points are obtained by solving the following system

$$\begin{cases} \frac{\partial THD^2}{\partial \alpha} = 0 \\ \frac{\partial THD^2}{\partial \beta} = 0 \end{cases} \tag{5.17}$$

that means

$$\begin{cases} \sum\limits_{k=5,\,7,\,11,\,13,\,\ldots} \frac{h_k(\alpha,\beta)[-k\sin(k\alpha)h_1(\alpha,\beta)+\sin(\alpha)h_k(\alpha,\beta)]}{kh_1^3(\alpha,\beta)} = 0 \\ \sum\limits_{k=5,\,7,\,11,\,13,\,\ldots} \frac{h_k(\alpha,\beta)[-k\sin(k\beta)h_1(\alpha,\beta)+\sin(\beta)h_k(\alpha,\beta)]}{kh_1^3(\alpha,\beta)} = 0 \end{cases} \tag{5.18}$$

where $h_s\,(\alpha,\beta) = \cos\,(s\alpha)+\cos\,(s\beta)$

$s = 1,\,5,\,7,\,11,\,13,\,\ldots$

Defining

$$\begin{cases} F_1\,(\alpha,\,\beta) = \sum\limits_k \frac{h_k(\alpha,\beta)[-k\sin(k\alpha)h_1(\alpha,\beta)+\sin(\alpha)h_k(\alpha,\beta)]}{k} \\ F_2\,(\alpha,\,\beta) = \sum\limits_k \frac{h_k(\alpha,\beta)[-k\sin(k\beta)h_1(\alpha,\beta)+\sin(\beta)h_k(\alpha,\beta)]}{k} \end{cases} \tag{5.19}$$

$k = 5, 7, 11, 13, ...,$ the solutions of system (5.18) (stationary points) are given by the intersections of the two curves $F_1(\alpha, \beta) = 0$ and $F_2(\alpha, \beta) = 0$ in the plane (α, β).

To find the relative minimum points of the function $THD^2(\alpha, \beta)$ between the stationary points, the classical analytical procedure that uses the Hessian matrix is laborious. In order to avoid this, a graphical procedure (GP) is introduced.

The GP overlaps, in the plane (α, β), the curves $F_1(\alpha, \beta) = 0$ and $F_2(\alpha, \beta) = 0$ to the level curves of the surface $z = THD^2(\alpha, \beta)$, given by (5.16), obtained varying the quote z of a regular step p. The minimum points are situated at the inner of Jordan level curves (closed continuous curves) characterized by lower z quotas.

Based on the relations (5.12) and (5.14), the switching angles are

$$\begin{cases} \alpha_1 = \left|\alpha + \frac{\pi}{6}\right| \\ \alpha_2 = \left|\beta - \frac{\pi}{6}\right| \\ \alpha_3 = \left|\frac{\pi}{6} - \alpha\right| \\ \alpha_4 = \left|\frac{\pi}{6} + \beta\right| \end{cases} \tag{5.20}$$

They have to satisfy conditions (5.7). The valid angles domain is the interval $\left[-\frac{\pi}{3}, \frac{\pi}{3}\right]$ for both α and β.

Fig. 5.4 shows the surface of $THD^2(\alpha, \beta)$. It is possible to observe that the maximum value of THD is about 30%. Fig. 5.5 shows the curves $F_1(\alpha, \beta) = 0$ and $F_2(\alpha, \beta) = 0$. The intersections of them are the stationary points. For this calculation harmonics up to the seventeenth are considered. By adding higher order harmonics in the calculation, the result remains similar.

Fig. 5.6 shows the level curves of equation 5.16 and overlapped to them the curves $F_1(\alpha, \beta) = 0$ and $F_2(\alpha, \beta) = 0$ for $\alpha \in [-2\pi, 2\pi]$ and $\beta \in [-2\pi, 2\pi]$. It is possible to observe the periodicity of all curves. Fig. 5.7 shows a zoom of the previous graph for $\alpha \in \left[-\frac{\pi}{3}, \frac{\pi}{3}\right]$ and $\beta \in \left[-\frac{\pi}{3}, \frac{\pi}{3}\right]$. The level curves of equation (5.16) are drawn for different z quotas. For the more close curves (at lower quotas), z varies between $5 \cdot 10^{-4}$ and $2 \cdot 10^{-2}$ with step 10^{-3}: this means that $THD\%$ varies about between 2% and 14%. The minimum values are the intersections of $F_1(\alpha, \beta) = 0$ and $F_2(\alpha, \beta) = 0$ situated inside the level curves defined for z varying between $5 \cdot 10^{-4}$ and $2 \cdot 10^{-2}$ as shown in Fig. 5.8.

Changing α with β the same solution $[\alpha_1, \alpha_2, \alpha_3, \alpha_4]$ is obtained, but with different components order. From Fig. 5.7, it is possible to observe the symmetries respect to bisector and to the straight lines $\alpha = 0$ and $\beta = 0$. For these reasons the domains for the angles are reduced to $\alpha = \left[0, \frac{\pi}{3}\right]$ and $\beta = \left[0, \frac{\pi}{3}\right]$ as shown in Fig. 5.8 where $'\mathrm{X}'$ symbol identifies the minimum points.

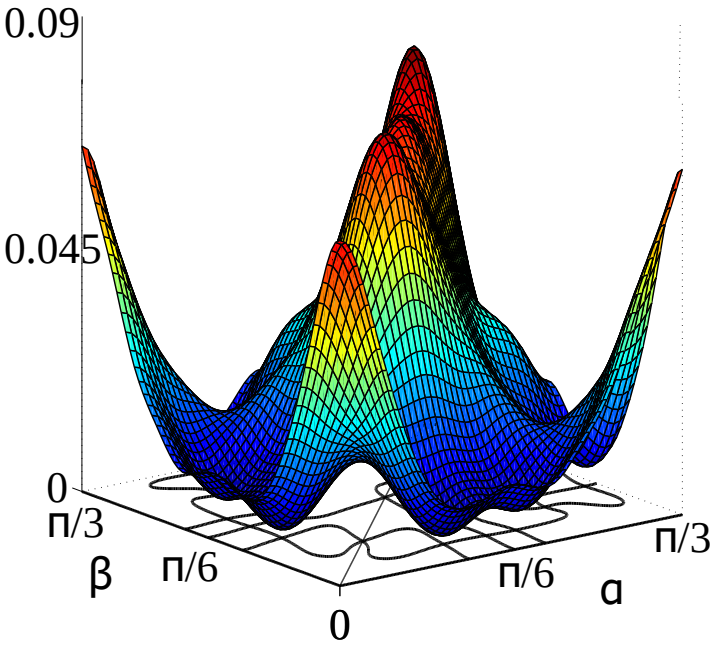


Figure 5.4: Surface of equation (5.16) and graphs of the curves (5.17) on the plane (α, β).

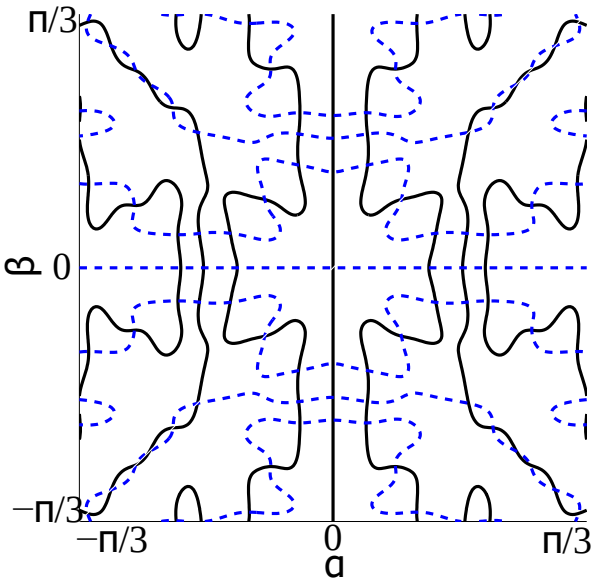


Figure 5.5: Curves $F_1(\alpha, \beta) = 0$ (continuous line) and $F_2(\alpha, \beta) = 0$ (dotted line).

5.2.4 Application and Results

Table Tab. 5.1 shows:

1. the pairs of $[\alpha, \beta]$ and the corresponding computed angles $[\alpha_1, \alpha_2, \alpha_3, \alpha_4]$ related to THD relative minimum points, in radians;

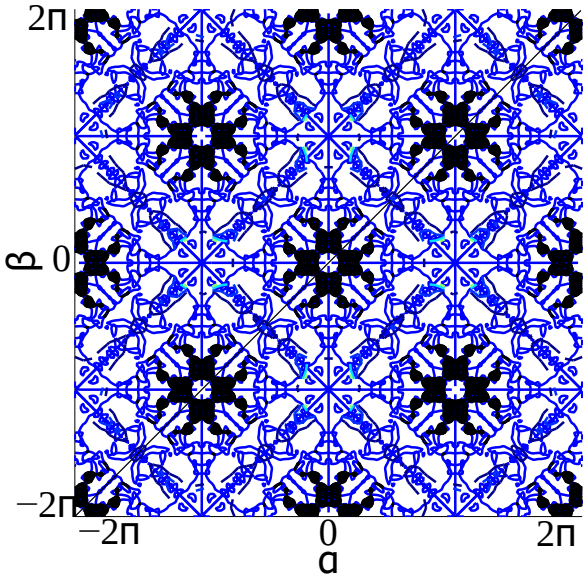


Figure 5.6: Level curves of equation (5.16) and overlapped to them the curves $F_1(\alpha, \beta) = 0$ and $F_2(\alpha, \beta) = 0$ for $\alpha, \beta \in [-2\pi, 2\pi]$.

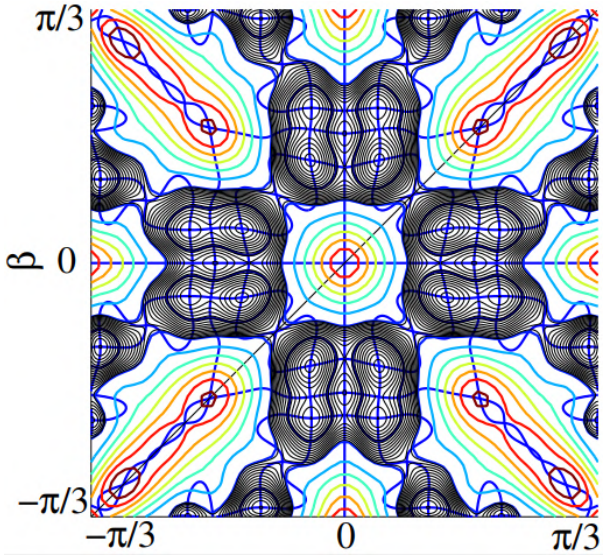


Figure 5.7: Zoom of Fig. Fig. 5.6.

2. the corresponding THD evaluated considering until 49^{th} harmonic.

Considering the best choice of switching angles regarding THD (the values in bold characters in Table Tab. 5.1, corresponding to the THD absolute minimum), the evaluated parameter C is equal to 1.2806 and the maximum value that the modulation index can assume is $m_{max} = 0.78$. Figures Fig. 5.9 and Fig. 5.10 show the voltage V^* and the considered switching angles as a function of m, respectively.

The application shown in Fig. 5.11, where the proposed modulation technique is

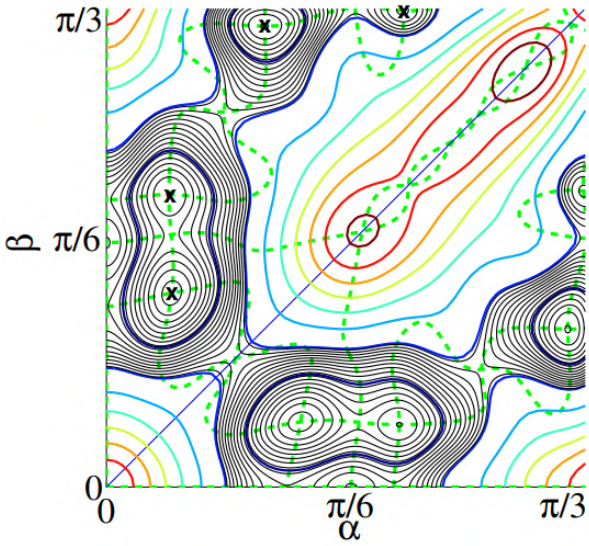


Figure 5.8: Zoom of Fig. Fig. 5.7, used for minimum points identifications. Dotted lines represent the curves $F_1(\alpha, \beta) = 0$ and $F_2(\alpha, \beta) = 0$.

Table 5.1: Switching angles in radians and corresponding THD obtained graphically solving (5.18).

α	β	α_1	α_2	α_3	α_4	THD
0.1424	**0.4244**	**0.0992**	**0.3812**	**0.6660**	**1.1464**	**8.27**
0.1366	0.6405	0.1169	0.3870	0.6602	1.1641	9.58
0.3455	1.0089	0.1781	0.4853	0.8691	1.5325	11.31
0.6477	1.0437	0.1241	0.5201	1.1713	1.5673	15.31

applied, is presented as example. Four DC sources are used to supply the DC/DC boost converters. Each DC output voltage is connected with one H-bridge of the 9-level inverter that is modulated with the technique discussed in the previous section, in order to obtain high quality output waveform. The switching angles, in radians, used in the simulation are $\alpha_1 = 0.0992$, $\alpha_2 = 0.3812$, $\alpha_3 = 0.6660$, $\alpha_4 = 1.1464$. They don't depend on modulation index. Variable supply voltages $V_{si}, \quad i = 1, 2, 3, 4$ are considered and voltage control loops on the boost converters are designed in order to keep a constant output voltage v_{out} and balanced inverter input voltages V_i.

The Proportional Integral (PI) controllers have different gains, their values are shown in Tab. 5.2.

The output voltage of the multilevel inverter and the corresponding harmonic spectrum are shown in Fig. 5.12. Harmonic amplitudes in percentage respect to fundamental are shown until the nineteenth since higher order harmonics are less important.

The response of the system to sudden DC supply voltage variations is depicted in Fig. 5.13. It can be seen that the controller is able to keep the AC output voltage

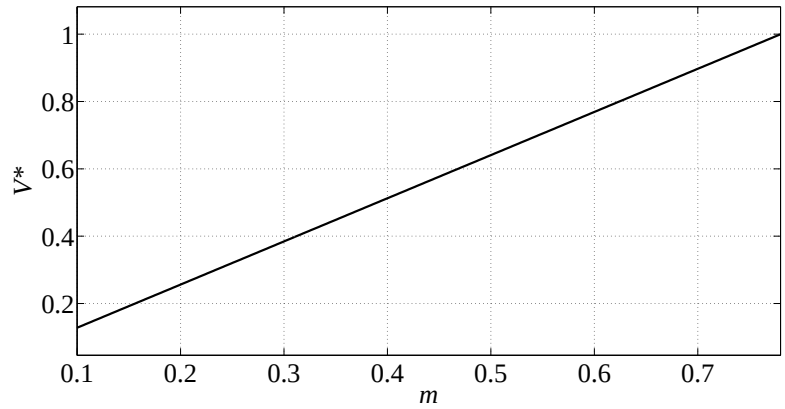


Figure 5.9: DC voltage amplitude in p. u..

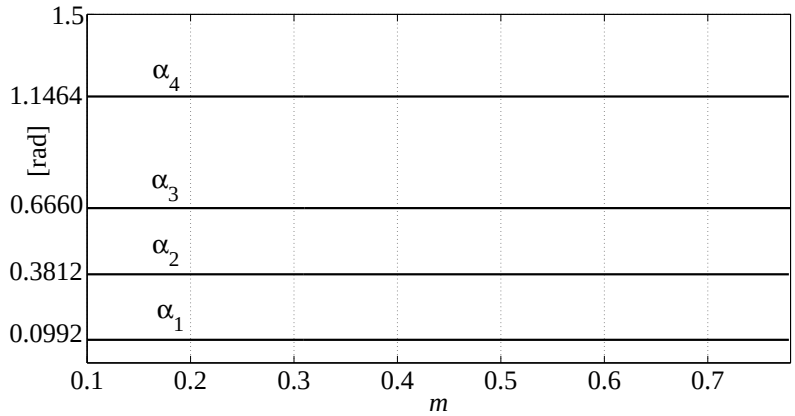


Figure 5.10: Switching angles producing the minimum THD value.

at the reference value, and at the same time, to ensure low THD level. This is particularly important because it allows to reduce output filter dimension and cost. Moreover, it is worth noting that the inverter switches at fundamental frequency of 50 Hz which means low switching losses and higher efficiency.

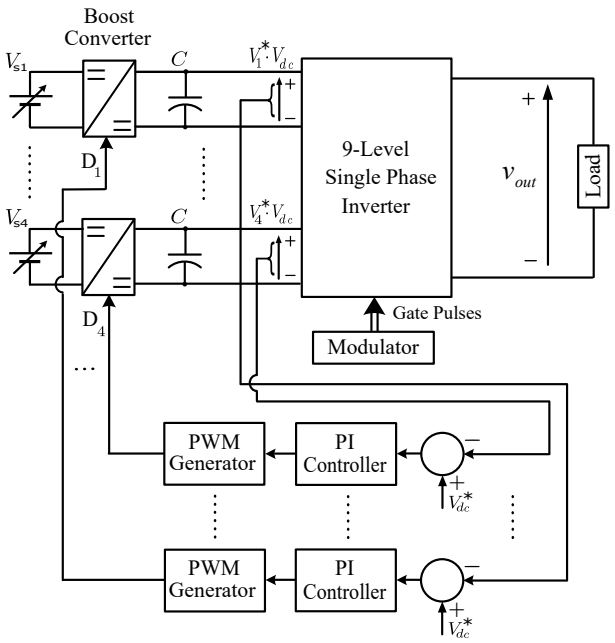


Figure 5.11: Block diagram of 9-level inverter with proposed modulation technique and current controlled boost converter.

5.3 A High Efficiency Selective Harmonic Elimination Technique for Multilevel Converters

5.3.1 Introduction

SHE techniques offer several advantages over other modulation methods: the most important is the low switching frequency principally for high voltage and high power applications, where switching losses are a major concern and their reduction is of prime importance. To find the analytical solution of the SHE equations is difficult because the problem is not linear. Numerous solving techniques have been proposed; they require high computational cost when the number of level is high [271, 272, 261, 277]. In order to reduce computational complexity, in [322] ,we proposed a new approach for a SHE technique. It consists of a simple expression to compute the switching angles that are equispaced in the interval $\left[0, \frac{\pi}{2}\right]$. Considering $l-$level inverters with s dc sources, this technique is capable to remove all harmonics, except those having order $n = 4sk \pm 1,\ k = 1, 2, 3, ...$ from the inverter output voltage, allowing very low THD. A mathematical proof about the orders of the harmonics deleted and not deleted, is given. It transforms the expression of harmonic amplitude from sum to product of sin and cos that is more simple to zero. High efficiency is ensured by the choice of switching frequency equal to fundamental one.

Table 5.2: System parameters used in the simulation.

Parameter	Description	Value
$V_n^* V_{dc}$	Input DC voltage [V]	40-60
V_{out}^*	Peak output reference voltage[V]	400
C	DC bus capacitor [mF]	1
$R - L$	Resistive-inductive load [Ω]-[mH]	50-1
f_{PWM}	Boost converter switching frequency [kHz]	5
K_{P1}	PI proportional gain	0.3
K_{P2}	PI proportional gain	0.3
K_{Pi3}	PI proportional gain	0.2
K_{P4}	PI proportional gain	1.5
K_{I1}	PI integral gain	5
K_{I2}	PI integral gain	10
K_{I3}	PI integral gain	4
K_{I4}	PI integral gain	3

5.3.2 Mathematical Model

For this study, a single phase l-level converter is considered. A modulation employing a reference sinusoidal signal at fundamental frequency is considered, having peak value V_m. In the interval $\left[0,\, \frac{\pi}{2}\right]$, the switching angles are the elements of the following equispaced sequence: $\alpha_k = (k-1)\,\alpha, \quad k = 1,\, 2,\, \ldots s$, where $\alpha = \frac{\pi}{2s}$. The s H-bridges are fed by s different dc voltage sources V_{dck} depending on the switching angles

$$\begin{cases} V_{dc1} = V_m \left[\sin\left(\frac{\alpha_1+\alpha_2}{2}\right)\right] \\ V_{dck} = V_m \left[\sin\left(\frac{\alpha_k+\alpha_{k+1}}{2}\right) - \sin\left(\frac{\alpha_{k-1}+\alpha_k}{2}\right)\right] \end{cases} \tag{5.21}$$

where $k = 2,\, 3,\, \ldots s$, where $\alpha_{s+1} = \frac{\pi}{2}$.

The choice of this modulation allows to delete all harmonics except those having order $n = 4sk \pm 1, \;\; k = 1,\, 2,\, 3,\, ...$

5.3.2.1 Calculation of n values that delete the harmonics amplitudes V_n

The spectrum of the inverter output voltage contains only odd harmonics, expressed as

$$V_n = \frac{4}{n\pi} \sum_{k=1}^{s} V_{dck} \cos\left(n\alpha_k\right) \tag{5.22}$$

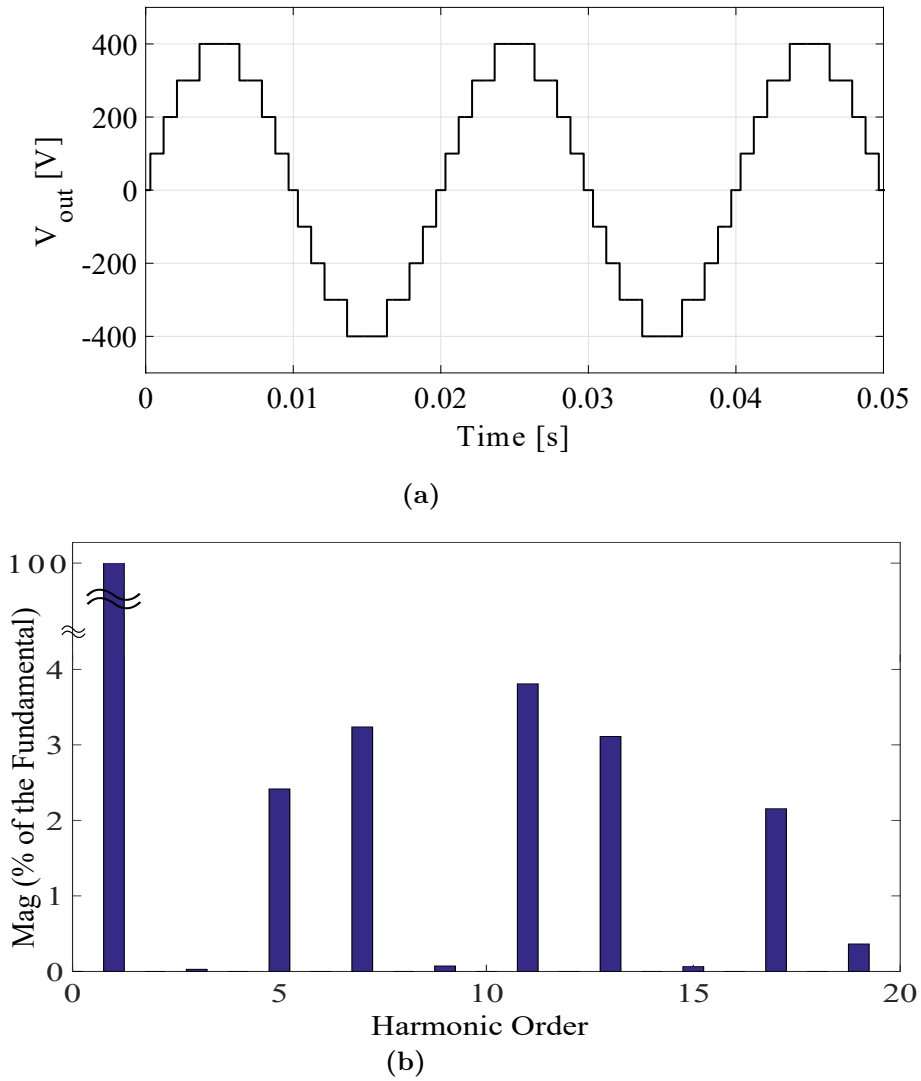


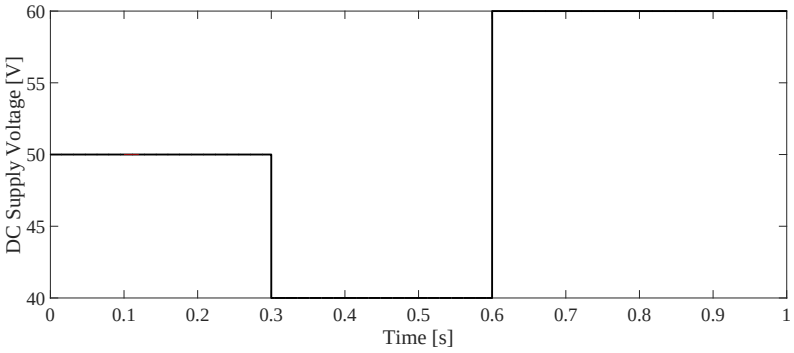
Figure 5.12: a) Output voltage waveform, b) Harmonic spectrum.

In order to compute the values n, such that $V_n = 0$, $n = 3, 5, 7, ...$, expression (5.22) is rearranged as

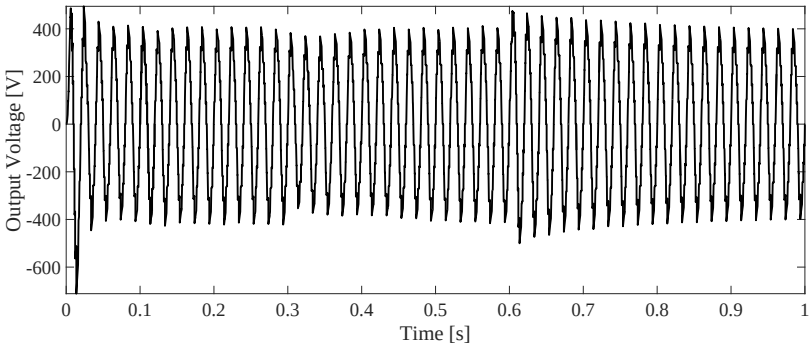
$$V_n = \frac{4V_m}{n\pi} \sum_{k=1}^{s} \left[\sin\left(\frac{\alpha_k+\alpha_{k+1}}{2}\right)\right] \left[\cos\left(n\left(k-1\right)\alpha\right) - \cos\left(nk\alpha\right)\right] \tag{5.23}$$

Applying Prosthaphaeresis formula to (5.23) and equalizing to zero, follows

$$2\sin\left(\frac{n\alpha}{2}\right)\left[\sum_{k=1}^{s} \sin\left(\left(2k-1\right)\frac{\alpha}{2}\right)\sin\left(n\left(2k-1\right)\frac{\alpha}{2}\right)\right] = 0 \tag{5.24}$$



(a)



(b)

Figure 5.13: a) DC supply voltage variation, b) Response of the system to DC supply voltage variation.

In literature results about discrete orthogonality properties of cos and sin functions are well known, but they are not completely applicable for the problem proposed in this paper.

Applying the Werner's formulas to (5.24), the following equality holds:

$$\begin{aligned} &2\sum_{k=1}^{s}\sin\left((2k-1)\,\tfrac{\alpha}{2}\right)\sin\left(n\,(2k-1)\,\tfrac{\alpha}{2}\right)= \\ &=[\sum_{k=1}^{s}\cos\left((n-1)\,(2k-1)\,\tfrac{\alpha}{2}\right)+ \\ &-\sum_{k=1}^{s}\cos\left((n+1)\,(2k-1)\,\tfrac{\alpha}{2}\right)] \end{aligned} \tag{5.25}$$

Lemma: For each s positive integer and $\beta \in R$, $\beta \neq k\pi$, $k = 0, \pm1, \pm2, \ldots$, the following relation holds

$$\sum_{k=1}^{s} \cos\left((2k-1)\,\beta\right) = \begin{cases} \frac{1}{2}\frac{\sin(2s\beta)}{\sin(\beta)} & \beta \neq p\pi,\ \ p = 1,\, 2,\, \ldots \\ \\ (-1)^p\, s & \beta = p\pi \end{cases} \tag{5.26}$$

Proof: By applying the Eulero's formulas $\cos(x) = \frac{e^{ix}+e^{-ix}}{2}$, $\sin(x) = \frac{e^{ix}-e^{-ix}}{2i}$ (i is the unit imaginary number), the following relation follows

$$\begin{aligned} &\sum_{k=1}^{s} \cos\left((2k-1)\,\beta\right) = \tfrac{1}{2}[e^{-i\beta} \sum_{k=1}^{s} \left(e^{i2\beta}\right)^k + \\ &+e^{i\beta} \sum_{k=1}^{s} \left(e^{-i2\beta}\right)^k] \end{aligned} \tag{5.27}$$

By applying to (5.27) the formula of geometric sum

$$\sum_{k=0}^{s} q^k = \frac{1-q^{s+1}}{1-q} \quad q \neq 1 \tag{5.28}$$

it is possible to obtain, by algebraic manipulations, the relation (5.26).

Based on Lemma 1., equation (5.24) becomes

$$\begin{aligned} &2\sin\left(\tfrac{n\alpha}{2}\right)\left[\sum_{k=1}^{s} \sin\left((2k-1)\,\tfrac{\alpha}{2}\right)\sin\left(n\,(2k-1)\,\tfrac{\alpha}{2}\right)\right] = \\ &\tfrac{1}{2}\sin\left(n\tfrac{\alpha}{2}\right)\left[\frac{\sin((n-1)s\alpha)}{\sin\left((n-1)\frac{\alpha}{2}\right)} - \frac{\sin((n+1)s\alpha)}{\sin\left((n+1)\frac{\alpha}{2}\right)}\right] \end{aligned} \tag{5.29}$$

After algebraic manipulations (5.29) becomes

$$\cos\left(\frac{\pi}{4s}\right)\sin^2\left(n\frac{\pi}{4s}\right)\frac{\sin\left((n-1)\,\frac{\pi}{2}\right)}{\sin\left((n-1)\,\frac{\pi}{4s}\right)\sin\left((n+1)\,\frac{\pi}{4s}\right)} \tag{5.30}$$

The expression (5.30) is equal to zero for any odd n because $\sin\left((n-1)\,\frac{\pi}{2}\right) = 0$, except for $n = 4sk \pm 1$ $k = 1, 2, 3, \ldots$ that set to zero the denominator.

Summarizing, the solutions of problem (5.24) are:

$$n = 2k + 1 \qquad n \neq 4sk \pm 1 \quad k = 1,\ 2,\ 3,\ ... \tag{5.31}$$

In order to investigate about indeterminate form $\left(\frac{0}{0}\right)$ of (5.30) in the points $n = 4sk \pm 1 \quad k = 1,\ 2,\ 3,\ ...$, the following limit is evaluated by applying De L'Hopital's rule:

$$\lim_{n \to 4sk \pm 1} \cos\left(\frac{\pi}{4s}\right) \sin^2\left(n\frac{\pi}{4s}\right) \frac{\sin\left((n-1)\,\frac{\pi}{2}\right)}{\sin\left((n-1)\,\frac{\pi}{4s}\right) \sin\left((n+1)\,\frac{\pi}{4s}\right)} = s \cdot \sin\left(\frac{\pi}{4s}\right) \tag{5.32}$$

Relation (5.32) allows to conclude that the harmonics V_n, $n = 4sk \pm 1 \quad k = 1,\ 2,\ 3,\ ...$, are different by zero, therefore (5.31) holds.

5.3.3 Simulation Results

Fig. 5.14 shows the single-phase l-level inverter configuration.

In order to confirm theoretical results about the values n that zero the amplitudes V_n, Fig. 5.15, Fig. 5.16 and Fig. 5.17 are highlighted for a 5-level, 9-level and for a 11-level inverter, respectively.

The red line (–.) represents the quantity $\left(-\frac{1}{2}\sin\left(n\frac{\alpha}{2}\right)\left[\frac{\sin((n+1)s\alpha)}{\sin\left((n+1)\frac{\alpha}{2}\right)}\right]\right)$ in (5.29).

The blue line (– –) the quantity $\left(\frac{1}{2}\sin\left(n\frac{\alpha}{2}\right)\left[\frac{\sin((n-1)s\alpha)}{\sin\left((n-1)\frac{\alpha}{2}\right)}\right]\right)$.

The continuous black line is their sum, all of them depending on n that is on x-axis. In Fig. 5.15 the twelve dot symbols are the pairs $\left(8k \pm 1,\ 2\sin\left(\frac{\pi}{8}\right)\right)$, where $k = 1,\ 2,\ 3,\ 4,\ 5,\ 6$. In Fig. Fig. 5.16 the six dot symbols are the pairs $\left(16k \pm 1,\ 4\sin\left(\frac{\pi}{16}\right)\right)$, where $k = 1,\ 2,\ 3$. In Fig. 5.17 the four dot symbols are the pairs $\left(20k \pm 1,\ 5\sin\left(\frac{\pi}{20}\right)\right)$, where $k = 1,\ 2$. In both cases, the second component, on $y-$axes, is obtained by (5.32).

In the considered harmonic order interval [3, 49], the sum function is zero for all n except the dot symbols that correspond to:

- $n = 8k \pm 1$, $k = 1,\ 2,\ 3,\ 4,\ 5,\ 6$ for 5-level inverter;
- $n = 16k \pm 1$, $k = 1,\ 2,\ 3$ for 9-level inverter;
- $n = 20k \pm 1$, $k = 1,\ 2$ for 11-level inverter.

Fig. 5.18-Fig. 5.22 show the spectrum analysis for five, nine, eleven, fifteen and twenty-one level inverters, respectively.

Fig. 5.23 shows the $THD\,\%$ as a function of the number of levels. When the number of levels ranges from 15 to 25, the total harmonic distortion ranges from 5.06 to 2.95.

5.3.4 Experimental results

The multilevel converter prototype used to carried out the experimental results is deeply shown in chapter 7 . For the purpose of this modulation technique, only 4 H-bridge modules of the multilevel prototype were used in order to obtain the required 9−level inverter.

The dc voltages, obtained for $V_m = 250$ V, are equal to 48.77 V, 90.12 V, 69.97 V, 37.33 V, respectively and the applied load is characterized by an active power of 0.3702 kW and a reactive power of 0.0051 kVAR.

In these conditions, the measured voltage and current waveforms are shown in Fig. 5.24.

The proposed procedure zero all harmonics except those having order $16k \pm 1 \;\; k = 1, 2, \ldots$. as shown in Fig. 5.25, obtained in open condition.

In Fig. Fig. 5.26, obtained in load condition, these harmonics assume very small values, as shown in Tab. 5.3.

Experimental results, obtained for an 9−level inverter, have confirmed the validity of the proposed modulation technique.

Table 5.3: Harmonic amplitudes in percentage, obtained in load condition.

n	$V_n\%$
3	0.871
5	0.571
7	0.389
9	0.297
11	0.261
13	0.209

5.4 Single-Phase Chebyshev Algorithm for Harmonics Mitigation in CHB Five-Level Inverters

5.4.1 Introduction

In [323] we proposed a modulation technique based on a partition generated by first kind Chebyshev polynomials zeros is proposed and applied to five-level cascaded H-bridge inverters. The same technique, applied to three phase voltage source inverters, has been presented in [293]. The Chebyshev modulation technique (CMT) allows to reduce THD of the output voltage waveform in comparison to the value obtained by LSPWM and PSPWM and the fact that the CMT is able to generate the switching signals without a need for carrier signals demonstrates a simple implementation advantage.

5.4.2 Mathematical model

A single phase five-level cascaded inverter shown in Fig. 5.27 is considered. A time partition generated by first kind Chebyshev polynomials zeros is used to create the switching pulses Q_i $i = 1, \ldots, 8$ represented in Figs. Fig. 5.28 and Fig. 5.29 driving the MOSFETs of five-level cascaded inverter. They are obtained assuming the data in sec. 5.4.3.

The procedure that generates these switching pulses is summarizes in the flowcharts in Fig. 5.30 and Fig. 5.31. It is articulated in the following steps:

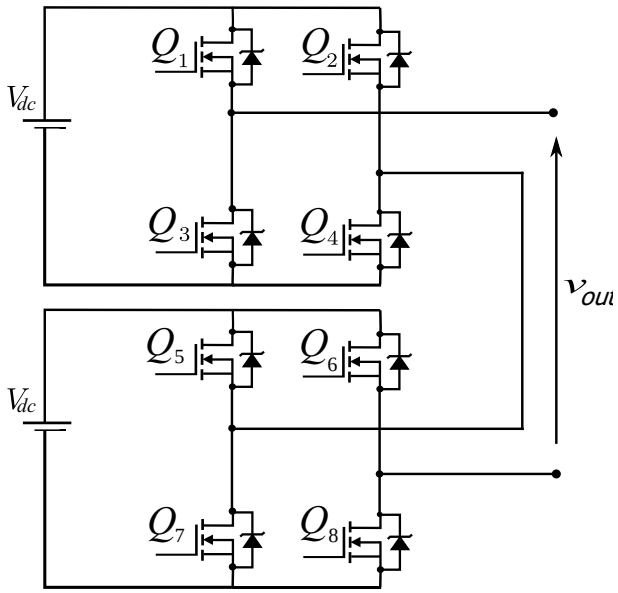


Figure 5.27: Cascaded five-level inverter configuration.

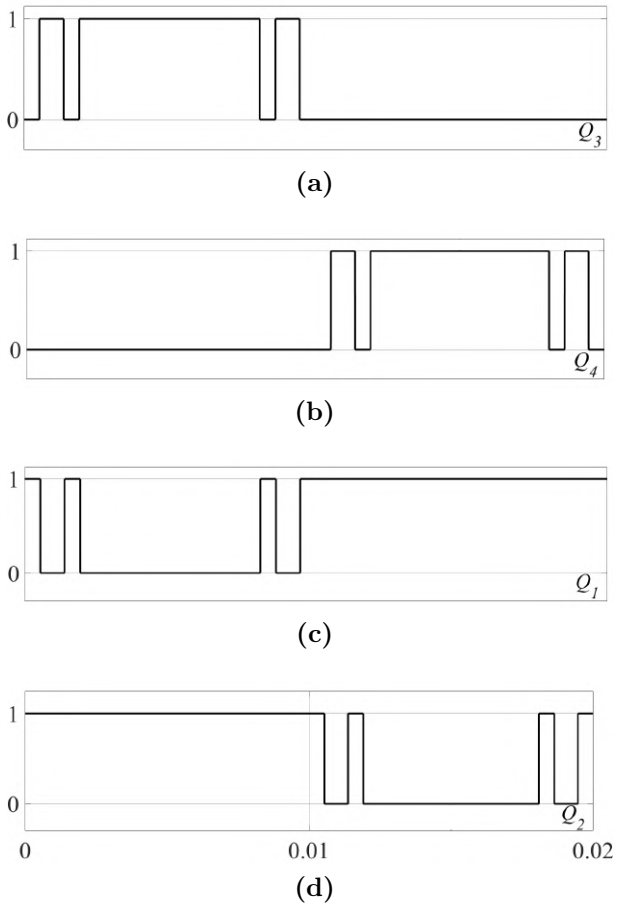


Figure 5.28: Switching pulses (a) Q_3, (b) Q_4, (c) Q_1, (d) Q_2.

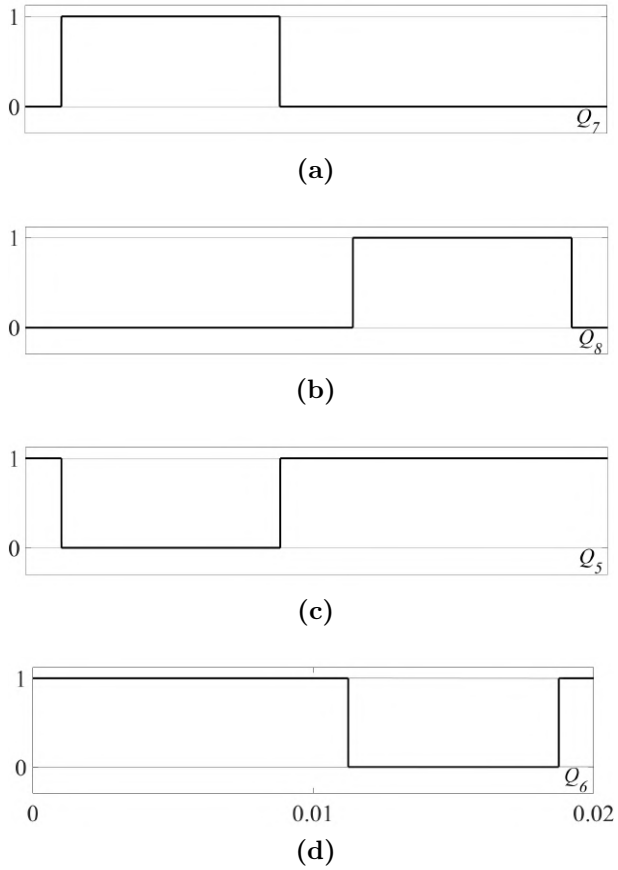


Figure 5.29: Switching pulses (a) Q_7, (b) Q_8, (c) Q_5, (d) Q_6.

1. it sets the time-shift α $(0 < \alpha < T/2)$ between the pulse patterns that driving Q_3 and Q_7, respectively;
2. it computes the first kind Chebyshev polynomials zeros x_j in $[0, T/2]$, $j = 1, \ldots, N+1$ ((1a) in Fig. 5.30) and y_j in $[\alpha, T/2 - \alpha]$, $j = 1, \ldots, M+1$ ((1b) inFig. 5.30) where N and M represent the number of pulses in half period;
3. it modifies these partitions to create the new partitions t_i, $i = 1, \ldots, N+1$ and d_i, $i = 1, \ldots, M+1$ that start from $t_1 = 0$ and $d_1 = \alpha$, respectively ((2a) and (2b) in Fig. 5.30);
4. as represented in Fig. Fig. 5.32, it defines the pulse widths $Toff_{ai}$ and Ton_{ai}, $i = 1, \ldots, N$ as (3a) and (4a) in Fig. 5.30, in the interval $[0, T/2]$ and $Toff_{bi}$ and Ton_{bi}, $i = 1, \ldots, M$ as (3b) and (4b) in Fig. 5.30) in the interval $[\alpha, T/2 - \alpha]$;
5. inside the intervals $[t_i, t_{i+1}]$, $i = 1, \ldots, N$ and $[d_i, d_{i+1}]$, $i = 1, \ldots, M$ it defines the start and end times of ON pulses ((5a)-(6a) and (5b)-(6b) in Fig. 5.30) and it stores them in two vectors;
6. it translates these two vectors in the periods $[T/2, T]$ and $[T/2 + \alpha, T - \alpha]$,respectively;
7. it generates the pulses Q_i, $i = 1, \ldots, 4$ in the intervals $[0, T/2] \cup [T/2, T]$ following the flowchart inFig. 5.31 (a) and the pulses Q_i, $i = 5, \ldots, 8$ in the

intervals $[\alpha, T/2-\alpha] \cup [T/2+\alpha, T-\alpha]$ following the flowchart in Fig. 5.31 (b).

5.4.3 Simulated results

The proposed CMT was applied to the cascaded five-level inverter shown in Fig. 5.27. A MATLAB code[2] was developed to generate switching pulses signals that were used by the multilevel inverter SIMULINK model [2]. The two H-bridges were fed by equal dc voltage $V_{dc} = 50\,V$ and a linear load $R = 10\,\Omega$ and $L = 24\,mH$ was connected. The input data (see Fig. 5.30) were chosen as: $T = 0.02\,s$, $M = 3$, $N = 1$ and $\alpha = \frac{T}{16}\,s$. The corresponding switching frequency was $f_s = 250\,Hz$, the considered modulation index was 1.064. Fig. 5.33 and Fig. 5.34 show the output voltage waveform and the corresponding harmonic spectrum, respectively.

The obtained results were compared to those carried out by PSPWM and level shifted phase opposition disposition PWM (LS-POD-PWM) techniques, at the same conditions. Fig. 5.35, Fig. 5.36 and Fig. 5.37, Fig. 5.38 show the output voltage and harmonic spectrum obtained by PSPWM and LS-POD-PWM, respectively, by using a triangular carrier signal at frequency of $f_s = 250\,Hz$. Tab. 5.4 shows the THD% obtained by all techniques considering until 49^{th} harmonic. It can be observed that, in the considered conditions, the proposed CMT allows to obtain lower THD%, reducing filter size and cost.

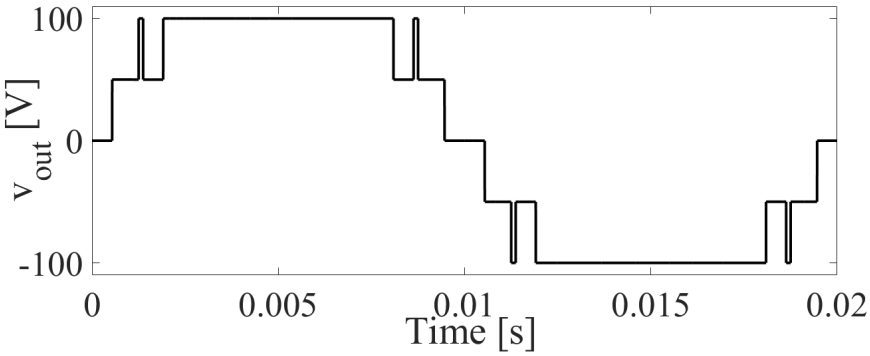


Figure 5.33: Output voltage waveform obtained by CMT.

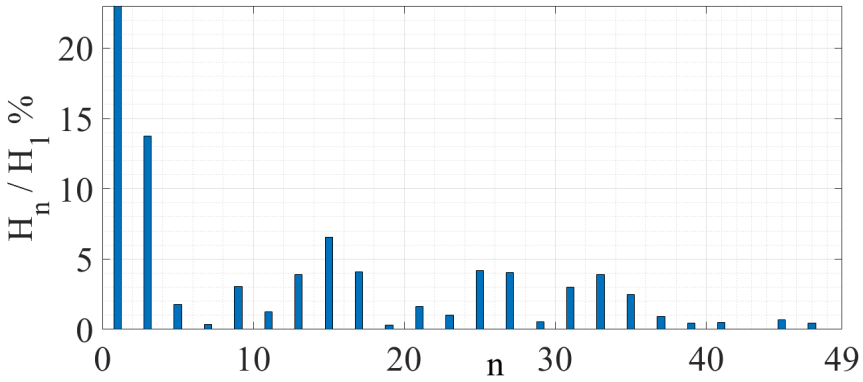


Figure 5.34: Harmonic spectrum obtained by CMT.

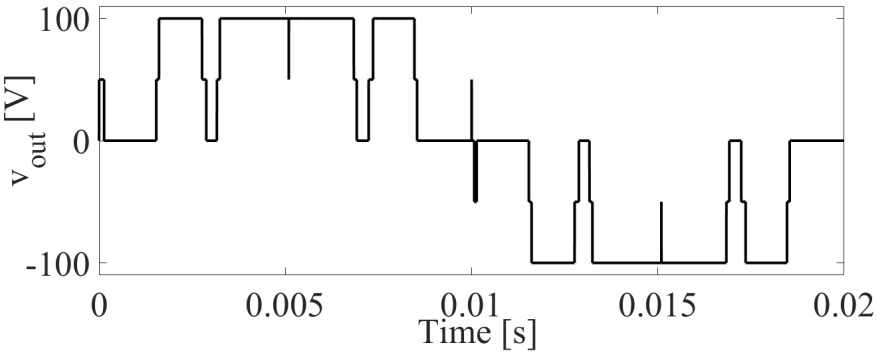


Figure 5.35: Output voltage waveform obtained by PSPWM.

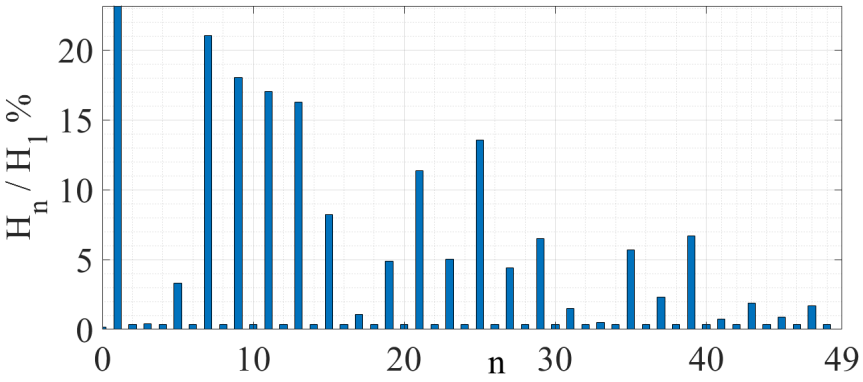


Figure 5.36: Harmonic spectrum obtained by PSPWM.

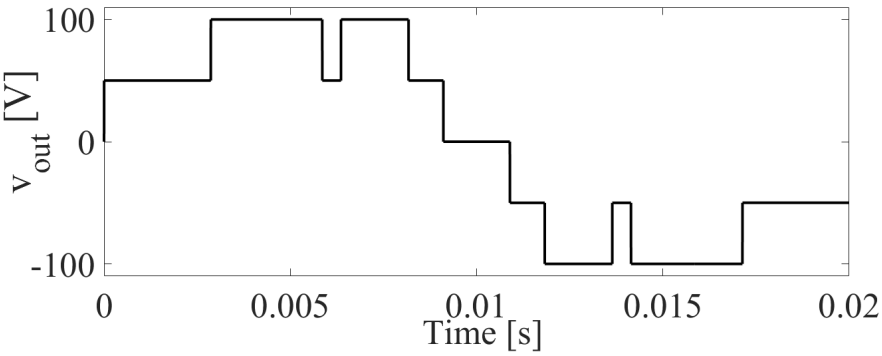


Figure 5.37: Output voltage waveform obtained by LS-POD-PWM.

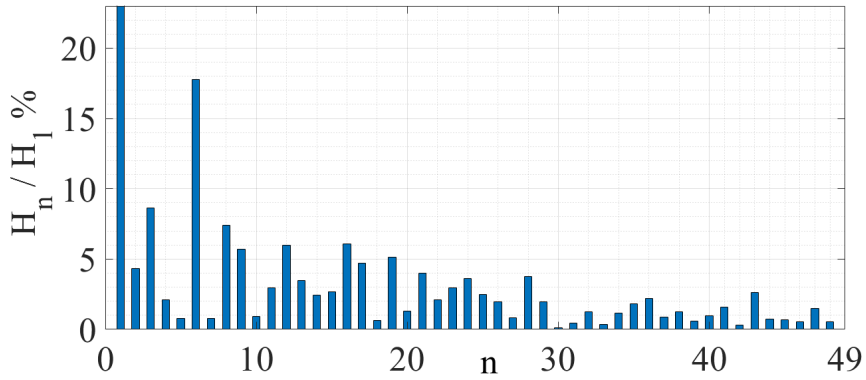


Figure 5.38: Harmonic spectrum obtained by LS-POD-PWM.

Table 5.4: Computed THD% obtained by different modulation techniques.

Modulation technique	THD%
CMT	18.7
PSPWM	43.9
LSPWM-POD	27.6

5.5 Harmonic Elimination Procedure for Cascaded Multilevel Inverters Having a Particular Even Number of DC Sources

5.5.1 Introduction

Several methods are implemented for harmonics elimination/mitigation in multilevel inverters [270]. In paper [282] a generalized formulation for Selective Harmonic Mitigation Pulse Amplitude Modulation (SHM-PAM) has been presented to control cascaded H-bridge inverters with non-equal DC sources. For five level inverter topology, real-time analytical methods for SHE problem are proposed in [10], [11]. In the modulation technique proposed in this chapter, cascaded multilevel inverters characterized by a number of level $l = 2s+1$ with $s = 2^n \quad n = 1, 2, 3, ...$, are considered and a procedure that allows to eliminate $n + 1$ harmonics and their respective multiple from the output voltage waveform, is proposed.

5.5.2 Mathematical Model

The single phase l-level inverter shown in Fig. 5.14 is considered with $l = 2s + 1$ and s number of dc sources given by $s = 2n, n = 1, 2, 3, ...$. The proposed technique allowing to eliminate $n + 1$ harmonics and their multiple, assumes:

- the dc sources V_i, $i = 1, 2, 3, ..., s$ feeding each H-bridge unequal and variable;
- fundamental frequency modulation.

The Fourier decomposition of output voltage of multilevel converter v_{out} can be expressed as:

$$v_{out}(wt) = \frac{4}{\pi} \sum_{k=1,3,5...}^{\infty} \frac{1}{k} \left[\sum_{i=1}^{s} V_i cos(k\alpha_i) \right] sin(kwt) \tag{5.33}$$

Introducing the p. u. quantities $V_i^* = \frac{V_i}{V_{dc}} \, i = 1, 2, 3, ..., s$ and assuming the voltages $V_1^* = V_2^* = V_3^* = ...V_s^*$depending on a positive coefficient C, such that $V^* = C_m$, where $m = \frac{\pi H_1}{4sV_{dc}}$ is the modulation index and H_1 is the fundamental harmonic amplitude, the following system can be written:

$$\begin{cases} V^*[cos(\alpha_1) + cos(\alpha_2) + cos(\alpha_3) + ...cos(\alpha_s)] = sm \\ \left\{ \frac{V^*}{k} [cos(k\alpha_1) + cos(k\alpha_2) + cos(k\alpha_3) + cos(k\alpha_s)] \right\} = 0 \quad k = 3, 5, ..., r_{n+1} \end{cases} \tag{5.34}$$

where r_{n+1} is the order of the last deleted harmonic. The unknown switching angles

$\alpha_1, ..., \alpha_s$ have to satisfy the following conditions:

$$0 < \alpha_k < \frac{\pi}{2} \quad k = 1, 2, 3, ..., s \tag{5.35}$$

with $\alpha_k \neq \alpha_h, \quad k \neq h$.

From the first equation of system 5.34it is possible to obtain the parameter C:

$$C = \frac{V^*}{m} = \frac{s}{cos(k\alpha) + cos(\alpha_2) + cos(\alpha_3) + ... + cos(k\alpha_s)} \tag{5.36}$$

The proposed procedure generates a linear system $s \times s$ in the unknowns $\alpha_i, \quad i = 1, 2, 3, ..., s$.

$$A\alpha = b \tag{5.37}$$

The matrix A and the vector b are defined in the following. The procedure sets to zero $n + 1$ harmonics

$$\frac{1}{k} \sum_{i=1}^{s} cos(k\alpha_i) = 0 \quad k = 3, 5, ..., r_{n+1} \tag{5.38}$$

By applying the Prosthaphaeresis formulas to 5.38, the following system is obtained

$$\frac{2}{k} \sum_{i=1,3}^{s-1} cos(\frac{k}{2}(\alpha_i + \alpha_{i+1}))cos(\frac{k}{2}(\alpha_i - \alpha_{i+1})) = 0 \tag{5.39}$$

For $k = 3h, h = 1, 3, ...,$ observing that $cos\left(\frac{3h}{2}(\beta + \gamma)\right) = 0$ when$\beta + \gamma = \frac{\pi}{3} + \frac{2}{3}r\pi, \quad r = 0, \pm1, \pm2, ...,$ the solutions of 5.39 can be constrained by the following $\frac{s}{2}$ relations

$$\alpha_i + \alpha_{i+1} = \frac{\pi}{3}, \quad i = 1, 3, ..., s - 1 \tag{5.40}$$

The relations in 5.40 are the first $\frac{s}{2}$ rows of 5.37. Substituting 5.40 in 5.39, the following equation is obtain

$$\sum_{i=1,3...}^{s-1} cos(k\delta_i) = 0 \quad k = 3, 5, ..., r_{n+1} \tag{5.41}$$

where $\delta_i = \frac{1}{2}(\alpha_i - \alpha_{i+1})$.). Equation 5.41 is similar to equation 5.38, but its number of addends is half respect to those contained in 5.38.

The procedure applies another time the Prosthaphaeresis formulas to 5.41 for $k = 5h, h = 1, 3, ...$, consequently $\frac{s}{4}$ relations similar to 5.40 are imposed for zero these harmonics; these relations, expressed in α_i , are the next $\frac{s}{4}$ rows of 5.37. An expression similar to 5.41 with half number of addends is obtained. In order to delete higher order harmonics, the Prosthaphaeresis formulas are reapplied to the new obtained expressions and consequently equations similar to 5.40 in new variables depending on α_i , are imposed. This process go on until 5.38 is reduced to one to to one term in the variables γ_1 and γ_2 having the following form:

$$cos(k\gamma_1)cos(k\gamma_2) \tag{5.42}$$

In order to zero the last two harmonics, having order r_n and r_{n+1}, and their multiple, the following system is obtained

$$\begin{cases} cos(r_n h\gamma_1)cos(r_n h\gamma_2) = 0 \\ cos(r_{n+1} h\gamma_1)cos(r_{n+1} h\gamma_2) = 0 \end{cases} \tag{5.43}$$

with $h = 1, 3, ...$

By 5.43 follows the system 5.44depending on α_i.

$$\begin{cases} \gamma_1 + \gamma_2 = \frac{\pi}{r_n} \\ \gamma_1 - \gamma_2 = \frac{\pi}{r_{n+1}} \end{cases} \tag{5.44}$$

Relations in 5.44 are the last two rows of 5.37.

The matrix $A = \begin{pmatrix} A_1 \\ A_2 \\ . \\ . \\ . \\ A_n \\ A_{n+1} \end{pmatrix}$ has coefficients $a_{ij} = 0, \pm 1$ and it is composed by sub-matrices $A_j \quad j = 1, 2, ..., n+1$ that, for $j = 1$ and$j = 2$, are shown in Tab. 5.5. The size of A_1 is $\frac{s}{2} \times s$, of $A_2$is $\frac{s}{4} \times s$, of $A_n$and $A_{n+1}$is $1 \times s$. The components of A_n are $a_{nj} = \pm 1 \quad j = 1, ..., s$. The components of $A_n + 1$ are:

$$\begin{cases} a_{(n+1)j} = a_{nj} \quad j = 1, ..., \frac{s}{2} \\ a_{(n+1)j} = -a_{nj} \quad j = \frac{s}{2} + 1, ..., s \end{cases}$$

The vector b in 5.37 is shown in Tab. 5.6.

In order to better understand the proposed method, some examples are discussed.

$$A_{1(\frac{s}{2}xs)} = \begin{pmatrix} 1 & 1 & 0 & 0 & \cdots & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & \cdots & 0 & 0 & 0 & 0 \\ \vdots & & & & \ddots & & & & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & \cdots & 0 & 0 & 1 & 1 \end{pmatrix}$$

$$A_{2(\frac{s}{2}\times s)} = \begin{pmatrix} 1 & -1 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & \cdots & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 1 & -1 & & \cdots & 0 & 0 & 0 & 0 \\ \vdots & & & & & & & & & \ddots & & & & \vdots \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \cdots & 1 & -1 & 1 & -1 \end{pmatrix}$$

Table 5.5: Matrices $Aj \;\; j = 1, 2. \; .$

$$b = \left(\underbrace{\frac{\pi}{3}, ..., \frac{\pi}{3}}_{2^{n-1}=\frac{s}{2}}, \underbrace{\frac{2\pi}{5}, ..., \frac{2\pi}{5}}_{2^{n-2}=\frac{s}{4}}, \underbrace{\frac{2^2\pi}{7}, ..., \frac{2^2\pi}{7}}_{s^{n-3}=\frac{s}{8}}, ..., \underbrace{\frac{2^{n-1}\pi}{r_n}}_{2^0}, \underbrace{\frac{2^{n-1}\pi}{r_{n+1}}}_{2^0} \right)$$

Table 5.6: Vector b.

A. 5-level inverter

In this case two harmonics (third and fifth) and their odd multiple will be deleted. The second equation of 5.34 can be written as:

$$\frac{V^*}{k}[cos(k\alpha_1) + cos(k\alpha_2)] = 0 \quad k = 3, 5$$

Equation 5.39 becomes

$$2cos(\frac{k}{2}(\alpha_1 + \alpha_2))cos(\frac{k}{2}(\alpha_1 - \alpha_2)) = 0 \quad k = 3h, 5h, \;\; h = 1, 3, ...$$

Therefore, to zero the third and fifth harmonics follows

$$\begin{cases} \alpha_1 + \alpha_2 = \frac{\pi}{3} \\ \alpha_1 - \alpha_2 = \frac{\pi}{5} \end{cases} \tag{5.45}$$

The final system is $\begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \begin{pmatrix} \alpha_1 \\ \alpha_2 \end{pmatrix} = \begin{pmatrix} \frac{\pi}{3} \\ \frac{\pi}{5} \end{pmatrix}$. Its solution, taking into account condition 5.35 and sorting the absolute values of components in ascendant order is $\tilde{\alpha_1} = \frac{\pi}{15}$and $\tilde{\alpha_2} = \frac{4\pi}{15}$.

B. 9-level inverter

The procedure allows to delete three harmonics (third, fifth and seventh) and their odd multiple

$$\frac{V^*}{k}[cos(k\alpha_1) + cos(k\alpha_2) + cos(k\alpha_3) + cos(k\alpha_4)] = 0 \quad k = 3, 5, 7 \tag{5.46}$$

Equation 5.39 becomes

$$2cos(\frac{k}{2}(\alpha_1 + \alpha_2))cos(\frac{k}{2}(\alpha_1 - \alpha_2) + 2cos(\frac{k}{2}(\alpha_3 - \alpha_4)cos(\frac{k}{2}(\alpha_3 - \alpha_4)) = 0 \tag{5.47}$$

$k = 3h, 5h, 7h, \;\; h = 1, 3, ...$

Therefore to zero the third harmonic follows

$$\begin{cases} \alpha_1 + \alpha_2 = \frac{\pi}{3} \\ \alpha_3 + \alpha_4 = \frac{\pi}{3} \end{cases} \tag{5.48}$$

Equation 5.47 becomes

$$cos(k\beta_1) + cos(k\beta_2) = 0 \quad k = 3h, 5h, 7h, \;\; h = 1, 3, ... \tag{5.49}$$

where $\beta_1 = \frac{\alpha_1 - \alpha_2}{2}$and $\beta_2 = \frac{\alpha_3 - \alpha_4}{2}$. Reapplying Prosthaphaeresis formulas to 5.49 follows

$$2cos(\frac{k}{2}(\beta_1 + \beta_2))cos(\frac{k}{2}(\beta_1 - \beta_2)) = 0 \quad k = 5h, 7h, \;\; h = 1, 3, ...$$

To zero the fifth and seventh harmonics follows

$$\begin{cases} \beta_1 + \beta_2 = \frac{\pi}{5} \\ \beta_1 - \beta_2 = \frac{\pi}{7} \end{cases} \tag{5.50}$$

i.e.

$$\begin{cases} \alpha_1 - \alpha_2 + \alpha_3 - \alpha_4 = \frac{2\pi}{5} \\ \alpha_1 - \alpha_2 - \alpha_3 + \alpha_4 = \frac{2\pi}{7} \end{cases} \tag{5.51}$$

The final system is

$$\begin{pmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & -1 & -1 & 1 \end{pmatrix} \begin{pmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \alpha_4 \end{pmatrix} = \begin{pmatrix} \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{2\pi}{5} \\ \frac{2\pi}{7} \end{pmatrix}$$

and, by solving this system, taking into account condition 5.35, considering the absolute values of and sorting these values in ascending order, the following switching angle, in radians, are obtained: $\tilde{\alpha_1} = 1.4960 \cdot 10^{-2}, \tilde{\alpha_2} = 4.3384 \cdot 10^{-1}, \tilde{\alpha_3} = 6.1336 \cdot 10^{-1}$and $\tilde{\alpha}_4 = 1.0622$.

C. 17-level inverter

In this case the harmonics deleted are four: third, fifth, seventh and eleventh and their odd multiple. Following the steps discussed in the previous cases, the obtained matrix A, the vector b and the obtained rearranged switching angles, in radians, are

$$A = \begin{pmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & -1 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{pmatrix}$$

$$b = \begin{pmatrix} \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{2\pi}{5} \\ \frac{2\pi}{5} \\ \frac{4\pi}{7} \\ \frac{4\pi}{11} \end{pmatrix} \quad \tilde{\alpha} = \begin{pmatrix} 1.2784 \cdot 10^{-1} \\ 1.5776 \cdot 10^{-1} \\ 2.9104 \cdot 10^{-1} \\ 4.7056 \cdot 10^{-1} \\ 5.7664 \cdot 10^{-1} \\ 7.5616 \cdot 10^{-1} \\ 9.1936 \cdot 10^{-1} \\ 1.2050 \end{pmatrix}$$

D. 33-level inverter

By this configuration, five harmonics (third, fifth, seventh, eleventh and thirteenth) are eliminated with their odd multiple. The matrix A is given by

$$A = \begin{pmatrix} S_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & S_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & S_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & S_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & S_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & S_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & S_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & S_1 \\ S_2 & S_2 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & S_2 & S_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & S_2 & S_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & S_2 & S_2 \\ S_2 & -S_2 & S_2 & -S_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & S_2 & -S_2 & S_2 & -S_2 \\ S_2 & -S_2 & -S_2 & S_2 & S_2 & -S_2 & -S_2 & S_2 \\ S_2 & -S_2 & -S_2 & S_2 & -S_2 & S_2 & S_2 & -S_2 \end{pmatrix}$$

where $S_1 = [1\,1]$, $S_2 = [1\,-1]$, $O = [0\,0]$. The vector b and the switching angles are:

$$b = \begin{pmatrix} \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{\pi}{3} \\ \frac{2\pi}{5} \\ \frac{2\pi}{5} \\ \frac{2\pi}{5} \\ \frac{2\pi}{5} \\ \frac{4\pi}{7} \\ \frac{4\pi}{7} \\ \frac{8\pi}{11} \\ \frac{8\pi}{13} \end{pmatrix} \qquad \tilde{\alpha} = \begin{pmatrix} 7.0092 \cdot 10^{-3} \\ 3.6929 \cdot 10^{-2} \\ 1.7021 \cdot 10^{-1} \\ 2.4867 \cdot 10^{-1} \\ 2.7859 \cdot 10^{-1} \\ 3.4973 \cdot 10^{-1} \\ 4.1187 \cdot 10^{-1} \\ 4.5581 \cdot 10^{-1} \\ 5.9139 \cdot 10^{-1} \\ 6.3533 \cdot 10^{-1} \\ 6.9747 \cdot 10^{-1} \\ 7.9853 \cdot 10^{-1} \\ 8.7699 \cdot 10^{-1} \\ 1.0402 \\ 1.0841 \\ 1.3258 \end{pmatrix}$$

5.5.3 Simulation Results

Simulation results are obtained by using MATLAB software [2]. In previous Section the obtained angles are given for 5-level, 9-level, 17-level and 33-level inverters and for them Figures 2, 3, 4 and 5 show the harmonic analysis. It is evident that the procedure eliminates the harmonics and their odd multiple depending on the level and the obtained THD% are very low as shown in Tab. 5.7.

Table 5.7: Computed parameter C and $THD\%$.

level l	parameter C	$THD\%$
5	1.214	16.44
9	1.245	10.89
17	1.258	4.94
33	1.267	2.98

Considering the grid connection applications, Tab. 5.8 shows the levels l_h(imposed by both the CIGRE WG 36–05 and the EN 50160 grid code [13], [14].

Following the grid codes requirements, it is possible to observe that the 17-level inverter, in addition to the elimination, reduces the thirteenth harmonic and the 33-level inverter reduces until the twenty-third harmonic. Fig. 5.43 shows the output voltages, in p.u., for 5-level, 9-level, 17-level and 33-level inverters highlighting, for the last case, the very good quality of the waveform.

Table 5.8: Grid codes EN 50160 and CIGRE WG 36-05.

	Odd	harmonics		Even	harmonics
Not multiple	of 3	Multiple	of 3		
n	l_n (%)	n	l_n (%)	n	l_n (%)
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.5	6....10	0.5
13	3	21	0.5	>10	0.2
17	2	>21	0.2	-	-
19	1.5	-	-	-	-
23	1.5	-	-	-	-
25	1.5	-	-	-	-
>25	0.2+32.5/n	-	-	-	-

5.5.4 Experimental Results

In order to validate the proposed procedure, the experimental prototype described in chapter 7 has been reconfigured for a 9-level inverter. The voltage dc source is

equal to $45\,V$ and the connected load has $R = 48.8\,\Omega$ and$L = 0.94\,mH$. Figures Fig. 5.44 and Fig. 5.45 show the output voltage and current waveforms and the harmonic analysis of the output voltage, respectively [15], [16]. The measured THD is equal to 10.94, that is very close to the computed value (see Tab. 5.7). Experimental analysis has shown the accuracy of the proposed procedure.

5.6 A New Pulse Active Width Modulation (PAWM) for Multilevel Converters

5.6.1 Introduction

Usually, existing SHE-PWM methods consider the switching angles as the unique degrees of freedom. For an assigned number of levels and a PWM algorithm, the higher the number of angles the higher the number of eliminated harmonics, but at the cost of increased frequency and switching losses. SHE-PAM techniques, in addition to pulse width modulation, vary the amplitudes of the input-side voltages, resulting additional degrees of freedom. Conventional equations are reformulated in such a way constant switching angles are obtained for a wide modulation index range.

Unequal DC link voltages and dynamic voltage unbalances represent significant problems in multilevel converters. To face with this problem, the elimination theory and the concept of resultants have been introduced in [253], Particle Swarm Optimization (PSO) theory in [254] and Homotopy in [255]. Paper [256] presents a multilevel selective harmonic elimination pulse-width modulation (MSHE-PWM) technique for transformerless static synchronous compensator (STATCOM) systems that optimizes both DC-voltage levels and switching angles, [257] proposes SHE at fundamental frequency in a 5-level cascaded inverter, based on graphical separation of functions zeros, [258] presents a SHE-PWM fulfilling IEC 61000-3-6, IEC 61000-2-12, EN 50160 and CIGRE WG 36-05 standards for single and three phase medium voltage H-bridge converters with variable DC links. Paper [282] proposes a generalized formulation for selective harmonic mitigation pulse amplitude modulation (SHM-PAM) to control CHB inverter with unequal DC sources.

SHE algorithms require the solution of a system of transcendental equations that

is not easy to find analytically, in the full range of modulation indices or operating points. Several iterative techniques have been proposed such as Newton–Raphson, sequential quadratic programming, gradient optimization, theory of resultants, but they are computationally burdensome, moreover, convergence becomes challenging with the increase of the number of variables. A Groebner-based SHE-PWM algebraic method has been proposed in [259] and [260]: the nonlinear high-order SHE equations are converted in an equivalent triangular form, then a recursive algorithm has been used to solve each triangular equation. Fast and accurate analytical methods have been presented in [261], [262] for 5-level inverters. However, none of these methods provide switching states for applications with continuously varying operating point.

In [324]we presents a pulse active width modulation (PAWM) with equally-spaced switching angles, developed for l-level CHB inverters fed by s unequal DC voltage sources. With proposed method, all harmonics, except those of order $n = 2kl \pm 1$, $k = 1, 2, \ldots$ disappear from the output voltage. A mathematical proof of the number and the order of deleted harmonics is given. Experimental results and a discussion validate proposed technique.

It is worth notice that both switching angles and total harmonic distortion (THD) of the output voltage do not depend on the modulation index m, which can be easily varied changing DC voltage levels. Proposed method can be successfully adopted in all those applications with variable DC sources, e.g. photovoltaic energy systems, uninterruptible power supplies (UPS), electric vehicle power trains, etc.

Proposed method works within the range of modulation index $0 \leq m \leq 1$, in which solution always exists.

To evaluate advantages and feasibility, proposed PAWM has been compared with

the methods described in [248], [250], [258], [249], [261]-[264].

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5.6.2 Pulse active width modulation (PAWM)

A l-level cascaded inverter, consisting of s H-bridges fed by s unequal DC voltage sources V_{dc1}, V_{dc2}, ... , V_{dcs}, has been considered, as shown in Fig. Fig. 5.46, with the following hypotheses:

1. the output voltage waveform v_0 is modulated by a reference sinusoidal signal (RSS) at fundamental frequency
2. the switching angles are chosen as $\theta_k = (2k-1)\,\frac{\pi}{2l}, \quad k = 1,\ 2\ldots,\ s$ and are equispaced with step $\alpha = \frac{\pi}{l}$, $l = 2s+1$ within the interval $\left[0,\ \frac{\pi}{2}\right]$
3. in the waveform v_0, s levels called E_1, E_2, ... E_s are identified in the following manner: considering a generic interval $[\theta_k,\ \theta_{k+1}]$, the level E_k is fixed at the magnitude of the RSS at the middle point, given by

$$E_k = V_m \sin\left(\frac{\theta_k + \theta_{k+1}}{2}\right) = V_m \sin\left(k\alpha\right) \quad k = 1,\ 2, ...,\ s \tag{5.52}$$

where V_m is the peak value of the RSS (see Fig.Fig. 5.47). The amplitudes of the DC voltage sources are

$$V_{dck} = E_k - E_{k-1} \qquad k = 1,\ 2, ...,\ s \tag{5.53}$$

with $E_0 = 0$ and $\theta_{s+1} = \frac{\pi}{2}$.

Under these assumptions and applying the Fourier series expression, the amplitude of the n^{th} harmonic V_n of v_0 is given by

$$V_n = \frac{4}{n\pi} \sum_{k=1}^{s} (E_k - E_{k-1}) \cos(n\theta_k) \tag{5.54}$$

Since v_0 is an odd function, even harmonics are absent and the formulation (5.54) holds only for odd harmonics.

As example, in Fig. Fig. 5.47 a 11-level inverter is considered, in this case $s = 5$, $l = 11$, $\theta_1 = \frac{\pi}{22}$, $\theta_2 = \frac{3\pi}{22}$, $\theta_3 = \frac{5\pi}{22}$, $\theta_4 = \frac{7\pi}{22}$ and $\theta_5 = \frac{9\pi}{22}$.

The amplitude of the first harmonic must be set to the modulation index value.

By rearranging equation (5.54), follows

$$V_n = \frac{4}{n\pi} \sum_{k=1}^{s} E_k \left[\cos\left(n(2k-1)\frac{\alpha}{2}\right) - \cos\left(n(2k+1)\frac{\alpha}{2}\right)\right] \tag{5.55}$$

Notice that $\cos\left((2s+1)\, n\frac{\alpha}{2}\right) = 0$ because $(2s+1)\, n\frac{\alpha}{2} = n\frac{\pi}{2}$ with n odd.

Applying Prosthaphaeresis formula in (5.55) and substituting E_i with (5.52), follows

$$V_n = \frac{4 \cdot 2V_m}{n\pi} \sin\left(n\frac{\alpha}{2}\right) \left[\sum_{k=1}^{s} \sin(nk\alpha) \sin(k\alpha)\right] \tag{5.56}$$

and after some trigonometric manipulations

$$V_n = \frac{4 \cdot V_m}{n\pi} \sin\left(n\frac{\alpha}{2}\right) \sum_{k=1}^{s} \left[\cos\left((n-1)\,k\alpha\right) - \cos\left((n+1)\,k\alpha\right)\right] \tag{5.57}$$

5.6.3 Analytical computation of n values that give $V_n = 0$ varying l

In this Section it is demonstrated that proposed modulation technique eliminates all harmonics, except those of order $n = 2kl \pm 1$, $k = 1, 2, \ldots$. The case $n = -1$ is not significant for the considered applications. Notice that in (5.57) the term $\sin\left(n\frac{\alpha}{2}\right)$ is equal to zero only for $n = 2kl$ even, hence only the sum $\sum_{k=1}^{s}$ $\left[\cos\left((n-1)\,k\alpha\right) - \cos\left((n+1)\,k\alpha\right)\right]$ contributes for the computation of n giving $V_n = 0$ [265].

Theorem 1:The sum

$$\sum_{k=1}^{s} \left[\cos\left((n-1)\,k\alpha\right) - \cos\left((n+1)\,k\alpha\right)\right] \quad \alpha = \frac{\pi}{l},\ l = 2s+1,\ s = 2,\ 3,\ \ldots \tag{5.58}$$

is equal to zero for all odd n, $n \neq 2kl \pm 1$, $k = 0, 1, 2, \ldots$.

Proof:

Introducing the function $S_l(h)$

$$S_l(h) = \sum_{k=1}^{s} \cos(hk\alpha) \tag{5.59}$$

with $h = n \pm 1$ and applying Eulero's formula to (5.59), the following expression is obtained

$$S_l(h) = \frac{1}{2}\left[\sum_{k=1}^{s}\left(e^{ih\alpha}\right)^k + \sum_{k=1}^{s}\left(e^{-ih\alpha}\right)^k\right] \tag{5.60}$$

with i imaginary unit. Since the sums in (5.60) are geometrical sums, (5.61) is obtained

$$S_l(h) = \frac{1}{2}\left[e^{ih\alpha}\frac{1-e^{ih\alpha s}}{1-e^{ih\alpha}} + e^{-ih\alpha}\frac{1-e^{-ih\alpha s}}{1-e^{-ih\alpha}}\right] \tag{5.61}$$

$h \neq 2kl$, $k = 0, 1, 2, \ldots$.

By mathematical manipulations (see **Appendix**), the following relation is obtained

$$S_l(h) = \frac{\sin\left(h\frac{\pi}{4}\,\frac{l-1}{l}\right)}{\sin\left(h\frac{\pi}{2l}\right)}\cos\left(h\frac{\pi}{4}\,\frac{l+1}{l}\right) \tag{5.62}$$

with $h \neq 2lk$, $k = 0, 1, 2, \ldots$. Rearranging (5.62) by using trigonometric formulas,

the following relation is obtained

$$S_l(h) = \frac{1}{2}\left[\frac{\sin\left(h\frac{\pi}{2}\right)}{\sin\left(h\frac{\pi}{2l}\right)} - 1\right] \tag{5.63}$$

From (5.59) and (5.63), the sum (5.58) becomes

$$\begin{array}{l} \sum_{k=1}^{s}\left[\cos\left((n-1)k\alpha\right) - \cos\left((n+1)k\alpha\right)\right] = \\ = S_l(n-1) - S_l(n+1) = \\ \frac{1}{2}\left[\frac{\sin\left((n-1)\frac{\pi}{2}\right)}{\sin\left((n-1)\frac{\pi}{2l}\right)} - \frac{\sin\left((n+1)\frac{\pi}{2}\right)}{\sin\left((n+1)\frac{\pi}{2l}\right)}\right] \end{array} \tag{5.64}$$

and, through easy mathematical manipulations, the following relationship is obtained

$$\begin{array}{l} \sum_{k=1}^{s}\left[\cos\left((n-1)k\alpha\right) - \cos\left((n+1)k\alpha\right)\right] = \\ \\ = -\cos\left(n\frac{\pi}{2}\right)\frac{\cos\left(\frac{\pi}{2l}\right)\sin\left(n\frac{\pi}{2l}\right)}{\sin\left((n-1)\frac{\pi}{2l}\right)\sin\left((n+1)\frac{\pi}{2l}\right)} \end{array} \tag{5.65}$$

For n odd, $n \neq 2lk \pm 1$, $k = 0, 1, 2, \ldots$, formula (5.65) is zero.

In order to evaluate (5.65) in $n = 2lk \pm 1$, where it is not defined (because has the form $\frac{0}{0}$), the following limit computation is done by applying the De L'Hospital rule

$$\lim_{n\to 2lk\pm 1}\left[-\cos\left(\frac{\pi}{2l}\right)\cos\left(n\frac{\pi}{2}\right)\frac{\sin\left(n\frac{\pi}{2l}\right)}{\sin\left((n-1)\frac{\pi}{2l}\right)\sin\left((n+1)\frac{\pi}{2l}\right)}\right] = \pm\frac{l}{2} \tag{5.66}$$

In this way, it is demonstrated that for $n = 2lk \pm 1$, the sum $\sum_{k=1}^{s} \left[\cos\left((n-1)\,k\alpha\right) - \cos\left((n+1)\,k\alpha\right)\right]$ 0.

From (5.65) and (5.66), the thesis is demonstrated.

In Fig. Fig. 5.48, a 11-level inverter is considered and the functions $S_{11}\,(n-1)$, $S_{11}\,(n+1)$ and their difference are shown, highlighting that only the harmonics of order $n = 21,\ 23,\ 43,\ 45$ are not zero.

Fig. Fig. 5.49 shows the influence of the modulation index m on the switching angles and DC voltage sources for 11-level CHB inverter. It is observed that switching angles remain constant and DC voltage varies linearly with m.

Fig. Fig. 5.50 shows the harmonic analysis obtained for l-level CHB inverters with $l = 5,\ 7,\ 9,\ 11,\ 13,\ 15$.

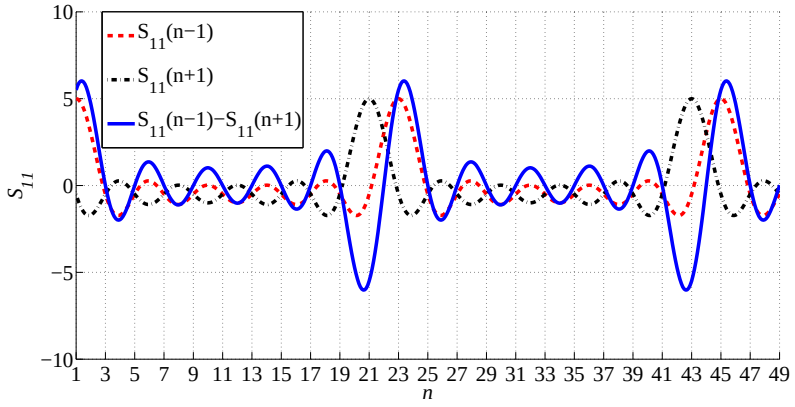


Figure 5.48: Behavior of the functions $S_{11}\,(n-1)$, $S_{11}\,(n+1)$ and their difference.

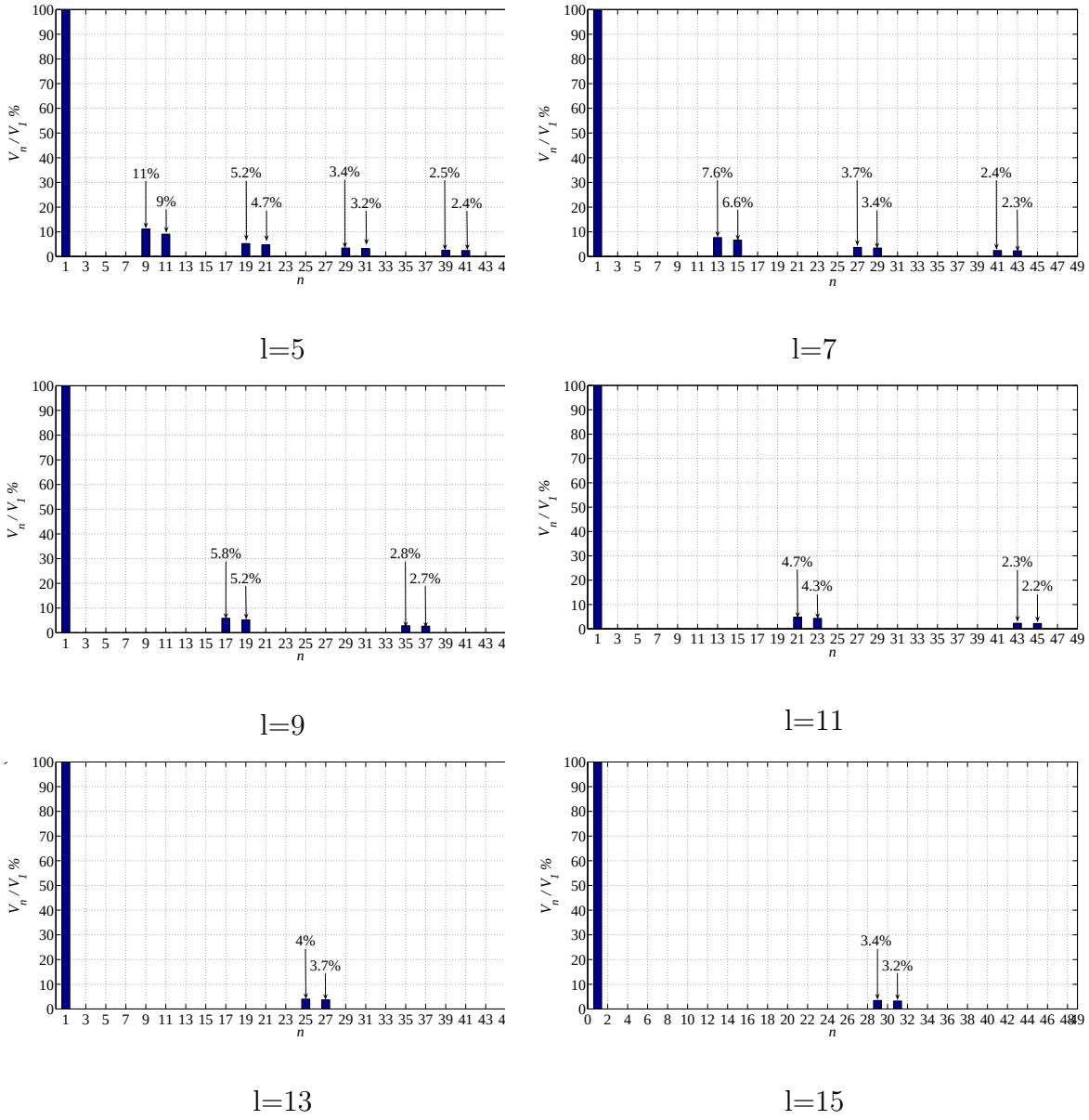


Figure 5.50: Harmonic analysis obtained for l-level CHB inverters with $l = 5, 7, 9, 11, 13, 15$

5.6.4 Comparison with other modulation techniques

In order to demonstrate the quality of PAWM, it has been compared with some methods known in literature.

Comparison with the method described in [250] A cascaded l-level inverter working at fundamental switching frequency ($l = 2s+1$ where s is the number of DC sources) is examined and the differences between them are shown in the following.

PAWM allows to zero more harmonics than the method proposed in [250]. It doesn't delete the harmonics having order

$$2lk \pm 1 \qquad k = 1,\, 2,\, \ldots \tag{5.67}$$

while, the procedure in [250] doesn't delete the harmonics having order

$$2Lk \pm 1 \qquad k = 1,\, 2,\, \ldots \tag{5.68}$$

where $L = l - 1$, therefore

$$2\,(l-1)\,k \pm 1 = 2lk \pm 1 - 2k \qquad k = 1,\, 2,\, \ldots\,. \tag{5.69}$$

Comparing (5.67) with (5.69) the term $2k$ implies that in [250] the first not deleted harmonic (for $k = 1$) is of order $(2l - 3)$ that is lower in comparison to the order $(2l - 1)$ obtained by PAWM. For example, for a 5-level inverter, considering up to the 49^{th} harmonic, PAWM does not delete 9 harmonics, the procedure in [250]

doesn't delete 12 harmonics as shown in Table Tab. 5.9.

In PAWM the first switching angle is different by zero: in fact, the switching angles are chosen such as $\theta_k = (2k-1)\,\frac{\pi}{2l}, \quad k = 1, .2.., s$. In [250] the first angle is always equal to zero. In fact, the angles are chosen as $\theta_k = (k-1)\,\frac{\pi}{(l-1)}, \quad k = 1, .2.., s$ (formula (5) in [250]). In Table Tab. 5.9, l-level inverters with $l = 5,\ 7,\ 9,\ 11,\ 13$ are considered and, for each of them, the harmonics deleted by PAWM and the technique in [250] are summarized taking into account the values until 49^{th} harmonic. The red dots denote the not canceled harmonics by PAWM, the blue dots the not canceled harmonics by modulation in [250] and the 'x' symbols the deleted ones.

The THD% of output voltage is defined as

$$\text{THD\%} = \frac{\sqrt{\sum_{i=3,\,5\,\ldots}^{49} V_i^2}}{V_1} 100 \tag{5.70}$$

it is constant as modulation index varies. Fig. Fig. 5.51 shows the output voltage THD% depending on levels numbers considering until $l = 21$, obtained by PAWM technique and by procedure in [250]. The better performance of PAWM is evident.

Table 5.9: Comparison between PAWM and technique in [250].

n	l									
	5		7		9		11		13	
	PAWM	[250]	PAWM	[250]	PAWM	[250]	PAWM	[250]	PAWM	[250]
3	x	x	x	x	x	x	x	x	x	x
5	x	x	x	x	x	x	x	x	x	x
7	x	●	x	x	x	x	x	x	x	x
9	●	●	x	x	x	x	x	x	x	x
11	●	x	x	●	x	x	x	x	x	x
13	x	x	●	●	x	x	x	x	x	x
15	x	●	●	x	x	●	x	x	x	x
17	x	●	x	x	●	●	x	x	x	x
19	●	x	x	x	●	x	x	●	x	x
21	●	x	x	x	x	x	●	●	x	x
23	x	●	x	●	x	x	●	x	x	●
25	x	●	x	●	x	x	x	x	●	●
27	x	x	●	x	x	x	x	x	●	x
29	●	x	●	x	x	x	x	x	x	x
31	●	●	x	x	x	●	x	x	x	x
33	x	●	x	x	x	●	x	x	x	x
35	x	x	x	●	●	x	x	x	x	x
37	x	x	x	●	●	x	x	x	x	x
39	●	●	x	x	x	x	x	●	x	x
41	●	●	●	x	x	x	x	●	x	x
43	x	x	●	x	x	x	●	x	x	x
45	x	x	x	x	x	x	●	x	x	x
47	x	●	x	x	x	●	x	x	x	●
49	●	●	x	●	x	●	x	x	x	●

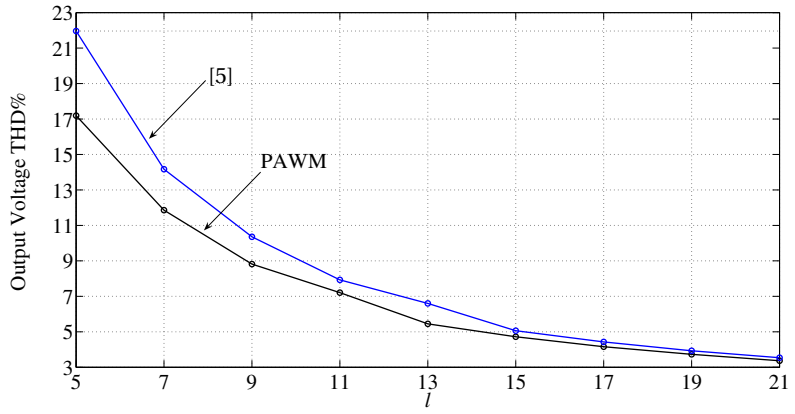


Figure 5.51: THD% obtained by PAWM as a function of levels number.

Comparison of PAWM with conventional SHE-SHM-PWM and SHE-SHM-PAM methods The performance of proposed PAWM has been compared with conventional SHE-SHM-PWM [261], [262], [263], [264] and SHE-SHM-PAM [248], [258], [249]. One switching transition per each level is considered, which offers identical switching frequency in SHE-SHM methods. Conventional SHE-PWM and SHE-PAM methods eliminate a total number of $\frac{l-3}{2}$ and $l-2$ harmonics, respectively. Fig. Fig. 5.52 shows the number of deleted harmonics as a function of levels number, considering until to the 301^{th} harmonic for proposed PAWM and for conventional SHE-PWM and SHE-PAM. PAWM eliminates a larger number of harmonics than conventional SHE methods. For example, for a 13-level CHB inverter, the total number of harmonics eliminated by SHE-PWM, SHE-PAM and PAWM are 5, 11, 127, respectively, if single phase configuration is considered, and 5, 11, 86, respectively, if three phase configuration is considered.

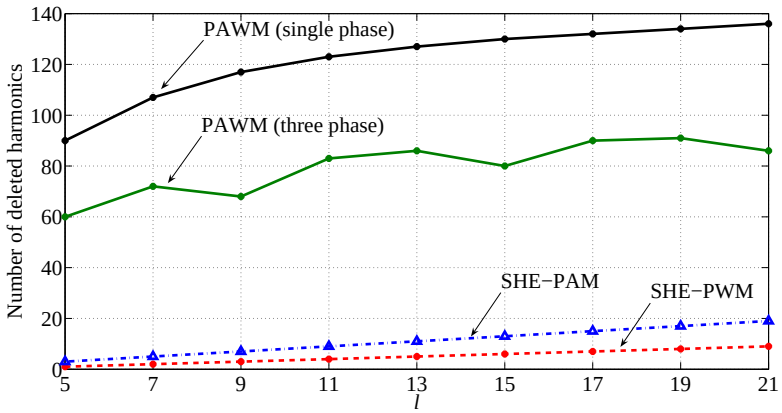


Figure 5.52: Number of deleted harmonics as a function of levels number.

In the following, three phase systems, in which third and multiple harmonics are not controlled, are considered. In particular, the output voltage THD% in three phase CHB 5- and 7- level inverters are computed and shown in Figs. Fig. 5.53 and Fig. 5.54, respectively. Results are carried out by using PAWM, SHM-PAM

technique applied to mitigate harmonics of order $k = 5, 7, \ldots, 49$ [258, 249] and SHE-PWM [261, 262, 263, 264] applied to eliminate the fifth harmonic for 5−level inverter, and the fifth and the seventh harmonics for 7−level inverter. Regarding SHE-PWM, when for a given m more solutions exist, the graph in Fig. Fig. 5.53 is obtained by choosing the values returning lesser THD. For 7- level inverter the SHE-PWM solution exists only in the modulation index range $m = [0.5, 084]$. Due to the intrinsic elimination of third and multiple harmonics in three phase systems, the proposed PAWM gives a little higher THD% values than SHM-PAM technique for CHB 5- and 9- level inverters, as shown in Fig. Fig. 5.55. For CHB 7- and 11-level inverters, the performance of the PAWM is better, in particular for 11-level. The weighted THD (WTHD), i. e. the harmonics amplitudes weighted with respect to the fundamental $\left(\frac{V_n}{V_1}\%\right)$ shown in Fig. Fig. 5.56 is computed for a three phase CHB 5-level inverter by using PAWM, SHE-PWM applied to eliminate the fifth harmonic considering $m = 0.8$ [261] and by SHM-PAM used to mitigate the harmonics of order $k = 5, 7, \ldots, 49$ [258, 249].

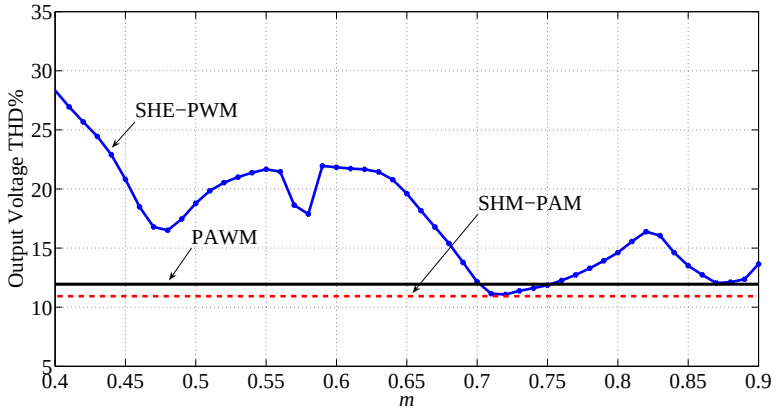


Figure 5.53: Output voltage THD% for a three phase CHB 5-level inverter, obtained by PAWM and conventional SHE-PWM and SHM-PAM techniques.

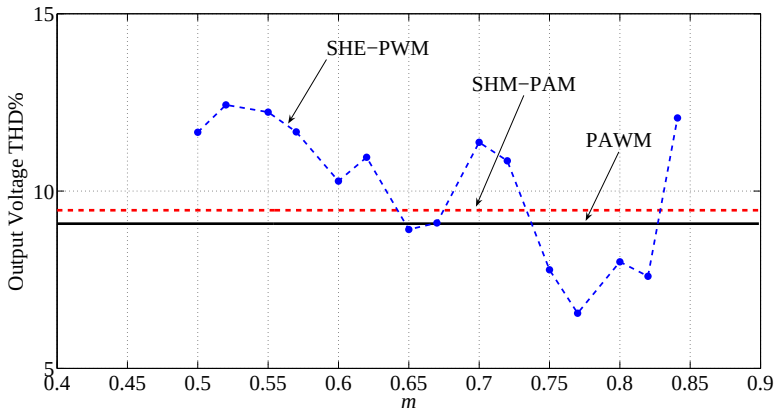


Figure 5.54: Output voltage THD% for a three phase CHB 7-level inverter, obtained by PAWM and conventional SHE-PWM and SHM-PAM techniques.

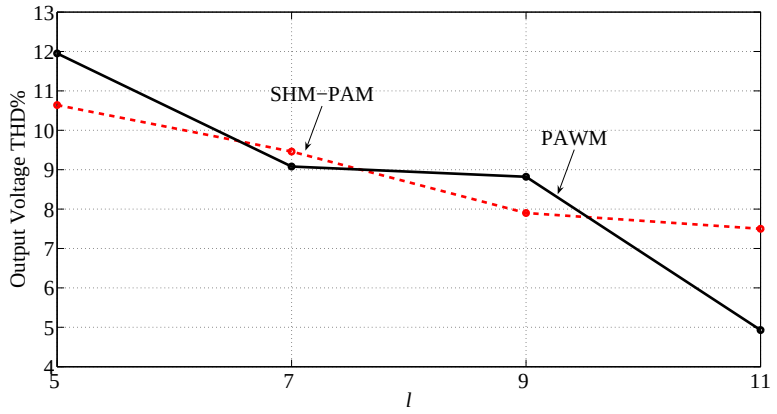


Figure 5.55: Output voltage THD% for a three phase CHB 5-level inverter, obtained by PAWM and conventional SHE-PWM and SHM-PAM techniques.

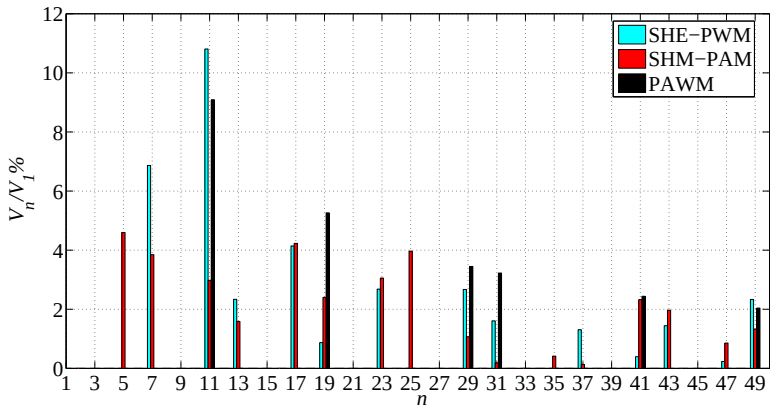


Figure 5.56: WTHD for a three phase CHB 5-level inverter, obtained by PAWM, SHE-PWM and SHM-PAM techniques.

5.6.5 Experimental results

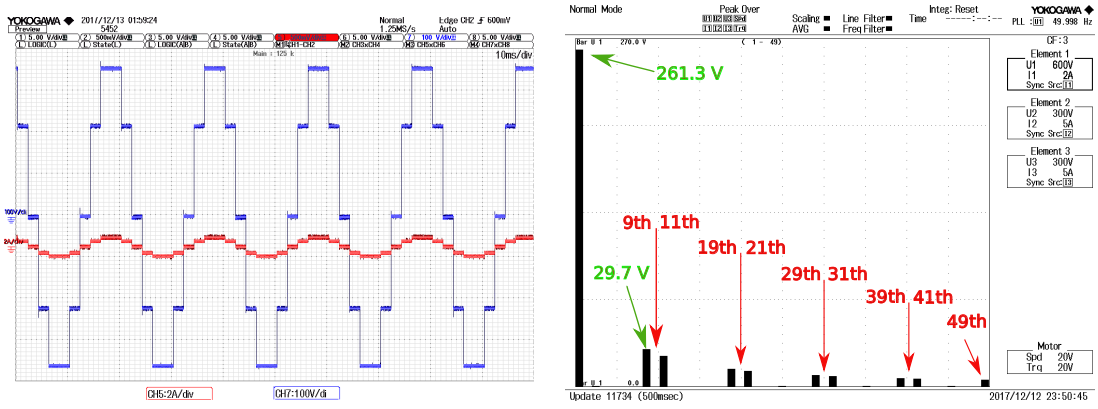
Experimental results have been obtained using a set of H-bridge cells produced by DigiPower [1]. Each cell (600 V, 30 A) can operate at switching frequency exceeding 40 kHz. The different multilevel configurations have been obtained cascading up to 5 cells, thus resulting $l = 5, 7, 9, 11$. Fig. Fig. 5.57 shows a single phase cascaded 9-level inverter configuration. Each H-bridge has its own DSP which provides to data acquisition and conditioning and SPI communications. The resulting converter is controlled by a field programmable gate array (FPGA) Intel Cyclone® V SE 5CSEBA6U23I7 programmed with Quartus [266]-[267], which provides pulse generation and dead-band logic with 32-bit resolution. Each cell is supplied by a programmable DC power supply Genesys 600-2.6, rated 600 V, 2.6 A, produced by TDK-Lambda.

Each H-bridge is supplied according to (5.53) with $V_m = 380$ V; the fundamental frequency is 50 Hz. The load connected to the multilevel inverters is characterized

by $R = 315\,\Omega$ and $L = 11.56\,\text{mH}$.

An eight channel Digital Oscilloscope Yokogawa DLM4058 (2.5 GS/s 500 MHz) and a Yokogawa WT1800 power meter complete the experimental setup. Obtained results, shown in Figs. Fig. 5.58-Fig. 5.61, are in full agreement with theoretical analysis.

Figure 5.57: Experimental setup.



(a) **(b)**

Figure 5.58: 5-level inverter configuration: (a) Output voltage (blue line) and current (red line) waveforms, (b) Harmonics amplitudes of output voltage in Volt.

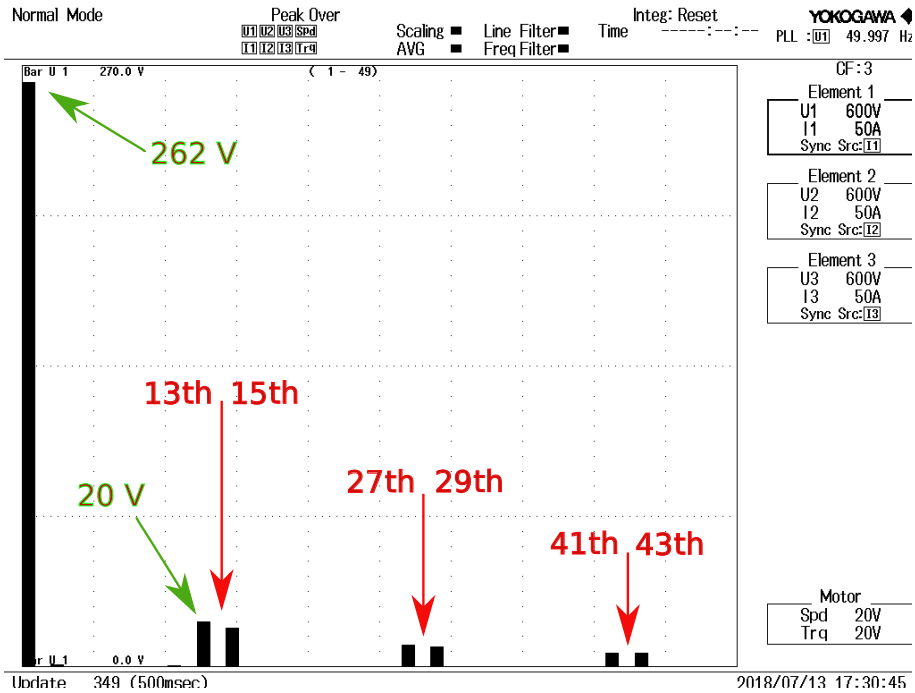


Figure 5.59: Harmonics amplitudes of output voltage for 7-level inverter.

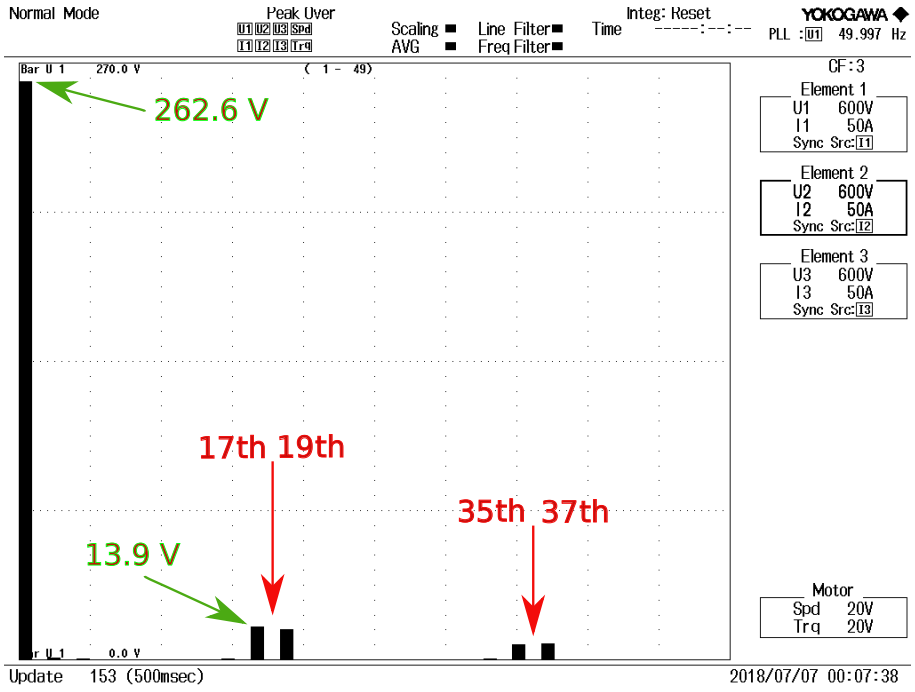


Figure 5.60: Harmonics amplitudes of output voltage for 9-level inverter.

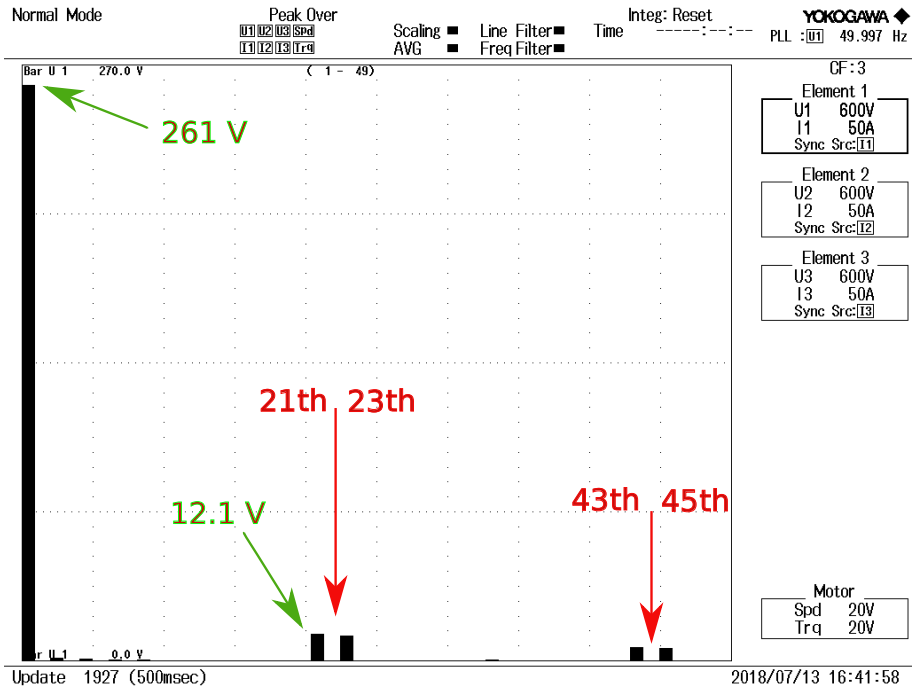


Figure 5.61: Harmonics amplitudes of output voltage for 11-level inverter.

The robustness of PAWM to disturbances around the designed DC link voltages, is verified considering a 7-level inverter connected with the RL load.

Assuming the designed DC voltages equal to $V_{dc1r} = 164.9\,V$, $V_{dc2r} = 132.2\,V$, $V_{dc3r} = 73.38\,V$, the tests named Case#1, Case#2 and Case#3, where disturbances occur, are performed and the corresponding output voltages THD% are measured. In Table Tab. 5.10 the considered disturbances are specified and the THD% is shown for each case. It is possible to observe that, in the worst Case#3, the THD% increases of about the same percentage of DC voltages disturbances, therefore the system is well conditioned. In the better Case#1 the increase of THD% is lesser respect to disturbances percentages.

Table 5.10: Output voltage THD% vs. designed DC link voltages disturbance.

	V_{dc1} [V]	V_{dc2} [V]	V_{dc31} [V]	THD%
DC voltages	V_{dc1r}=164.9	V_{dc2r}=132.2	V_{dc3r}=73.38	11.86
Case#1	V_{dc1r}-10%=148.4	V_{dc2r}+10%=145.4	V_{dc3r}+5%=77.1	12.32
Case#2	V_{dc1r}-20%=131.9	V_{dc2r}+20%=158.7	V_{dc3r}+10%=80.7	13.51
Case#3	V_{dc1r}-30%=115.4	V_{dc2r}+30%=171.9	V_{dc3r}+20%=88.1	15.46

The same 7-level configuration with the same load is used to evaluate transient conditions during modulation index variations, obtained modifying, for each module, the equation (5.53), i.e. V_{dck}, $k = 1, 2, .3$. DC voltages values change from $V_{dc1} = 108.5\,\mathrm{V}$, $V_{dc2} = 87\,\mathrm{V}$, $V_{dc3} = 48.3\,\mathrm{V}$ corresponding to $m = 0.657$ to the new values $V_{dc1} = 164.9\,V$, $V_{dc2} = 132.2\,\mathrm{V}$, $V_{dc3} = 73.38\,V$ corresponding to $m = 1$, as shown in Fig. Fig. 5.62(a). Voltage and current transient responses are shown in Fig. Fig. 5.62(b). It can be noticed that steady state condition is reached after about 30 ms.

5.6.6 Conclusions

A new procedure based on pulse amplitude width modulation (PAWM) has been developed for CHB converters fed by unequal DC voltage sources. Proposed procedure identifies equispaced switching angles and performs a modulation of the output voltage on the base of a reference sinusoidal signal fixed at the fundamental frequency. A mathematical proof has been presented demonstrating that PAWM deletes all harmonics embedded within the output voltage waveform of a l-level inverter, except those of order $n = 2kl \pm 1$, $k = 1, 2, \ldots$.

Harmonic elimination capability of PAWM has been validated by simulation and experimental results as well as comparisons with some existing methods.

The main features of PAWM can be summarized as follows:

- its fundamental switching frequency operation guarantees high efficiency
- for a chosen number of levels and for the whole modulation index range ($0 \leq m \leq 1$) it fixes, in optimal way, both the switching angles as well as the amplitudes of the DC-voltages, resulting more harmonics eliminated than using other methods
- THD% does not depend on the modulation index
- when implemented on a 17- level inverter, proposed PAWM satisfies the main grid code requirement (THD% $< 5\%$) without the use of any passive filter; full harmonics elimination (up to 49-th order) is obtained by using a 27-level inverter.

Potential applications of PAWM are numerous, it can be successfully implemented in multilevel converters with DC converters in front of the H-bridges. Among the others: photovoltaic and wind generators, UPS.

Appendix

Formula (5.61) can be written as

$$S_l(h) = \frac{1}{2}\left[e^{ih\alpha}\frac{1-e^{ih\alpha s}}{1-e^{ih\alpha}} + \frac{1}{e^{ih\alpha}}\frac{1-\frac{1}{e^{ih\alpha s}}}{1-\frac{1}{e^{ih\alpha}}}\right] =$$
$$= \frac{1}{2}\left[e^{ih\alpha}\frac{1-e^{ih\alpha s}}{1-e^{ih\alpha}} + \frac{1}{e^{ih\alpha s}}\frac{1-e^{ih\alpha s}}{1-e^{ih\alpha}}\right] =$$
$$= \frac{1}{2}\frac{1-e^{ih\alpha s}}{1-e^{ih\alpha}}\left(e^{ih\alpha} + \frac{1}{e^{ih\alpha s}}\right) =$$
$$= \frac{1}{2}\frac{1-e^{ih\alpha s}}{1-e^{ih\alpha}}\left(\frac{e^{ih\alpha(s+1)}+1}{e^{ih\alpha s}}\right) =$$
$$= \frac{e^{-ih\alpha\frac{s}{2}}-e^{ih\alpha\frac{s}{2}}}{e^{-ih\frac{\alpha}{2}}-e^{ih\frac{\alpha}{2}}}\ \frac{e^{ih\alpha\frac{s}{2}}}{e^{ih\frac{\alpha}{2}}}\ \frac{e^{ih\alpha\frac{s+1}{2}}+e^{-ih\alpha\frac{s+1}{2}}}{2}\ \frac{e^{ih\alpha\frac{s+1}{2}}}{e^{ih\alpha s}} =$$
$$= \frac{\sin\left(h\alpha\frac{s}{2}\right)}{\sin\left(h\frac{\alpha}{2}\right)}\cos\left(h\alpha\frac{s+1}{2}\right)\frac{e^{ih\alpha\frac{s+1}{2}}\,e^{ih\alpha\frac{s}{2}}}{e^{ih\alpha s}\,e^{ih\frac{\alpha}{2}}}.$$

Since $\frac{e^{ih\alpha\frac{s+1}{2}}\,e^{ih\alpha\frac{s}{2}}}{e^{ih\alpha s}\,e^{ih\frac{\alpha}{2}}} = e^{ih\alpha 0} = 1$, it follows that previous equation becomes:

$$\frac{\sin\left(h\alpha\frac{s}{2}\right)}{\sin\left(h\frac{\alpha}{2}\right)}\cos\left(h\alpha\frac{s+1}{2}\right)=$$
$$=\frac{\sin\left(h\frac{\pi}{4}\frac{l-1}{l}\right)}{\sin\left(h\frac{\pi}{2l}\right)}\cos\left(h\frac{\pi}{4}\frac{l+1}{l}\right)$$

that is formula (5.62) which can be written as

$$\frac{\sin\left(h\left(\frac{\pi}{4}-\frac{\pi}{4l}\right)\right)}{\sin\left(h\frac{\pi}{2l}\right)}\cos\left(h\left(\frac{\pi}{4}+\frac{\pi}{4l}\right)\right)$$

By using the trigonometric formula $\sin p\cos q=\frac{1}{2}\left[\sin\left(q+p\right)-\sin\left(q-p\right)\right]$, the previous formula becomes

$$\frac{1}{2}\frac{\sin\left(h\frac{\pi}{2}\right)-\sin\left(h\frac{\pi}{2l}\right)}{\sin\left(h\frac{\pi}{2l}\right)}$$
$$=\frac{1}{2}\left[\frac{\sin\left(h\frac{\pi}{2}\right)}{\sin\left(h\frac{\pi}{2l}\right)}-1\right]$$

that is formula (5.63). By substituting $(n-1)$ and $(n+1)$ to h, formula (5.64) is obtained:

$$\sum_{k=1}^{s}\left[\cos\left(\left(n-1\right)k\alpha\right)-\cos\left(\left(n+1\right)k\alpha\right)\right]=$$
$$=S_l\left(n-1\right)-S_l\left(n+1\right)=$$
$$\frac{1}{2}\left[\frac{\sin\left((n-1)\frac{\pi}{2}\right)}{\sin\left((n-1)\frac{\pi}{2l}\right)}-\frac{\sin\left((n+1)\frac{\pi}{2}\right)}{\sin\left((n+1)\frac{\pi}{2l}\right)}\right]$$

Considering S as function in the variable n, by applying to the numerators the trigonometric formula $\sin\left(q\pm p\right)=\sin p\cos q\pm\sin q\cos p$, previous formula becomes:

$$-\frac{1}{2}\cos n\frac{\pi}{2}\left[\frac{1}{\sin\left((n-1)\frac{\pi}{2l}\right)}+\frac{1}{\sin\left((n+1)\frac{\pi}{2l}\right)}\right]$$
$$=-\frac{1}{2}\cos n\frac{\pi}{2}\frac{\sin\left((n+1)\frac{\pi}{2l}\right)+\sin\left((n-1)\frac{\pi}{2l}\right)}{\sin\left((n-1)\frac{\pi}{2l}\right)\sin\left((n+1)\frac{\pi}{2l}\right)}$$
$$=-\cos n\frac{\pi}{2}\frac{\sin\left(n\frac{\pi}{2l}\right)\cos\left(\frac{\pi}{2l}\right)}{\sin\left((n-1)\frac{\pi}{2l}\right)\sin\left((n+1)\frac{\pi}{2l}\right)}$$

that is (5.65).

5.7 Summary

With increase in use of non-linear loads, the issues of power supply harmonics are more noticeable than ever. Controlling and monitoring industrial system designs and

their effects on utility distribution systems are potential problems for the industrial consumer.

In this chapter, several innovative modulation techniques for multilevel converters have been presented. These procedures have been developed with the aim of providing a better harmonic content with respect to the other well-know SHE modulations and their advantages have been highlighted in this chapter. Several comparisons with the conventional modulation techniques have been presented and the experimental results have been shown in order to validate the proposed mathematical models.

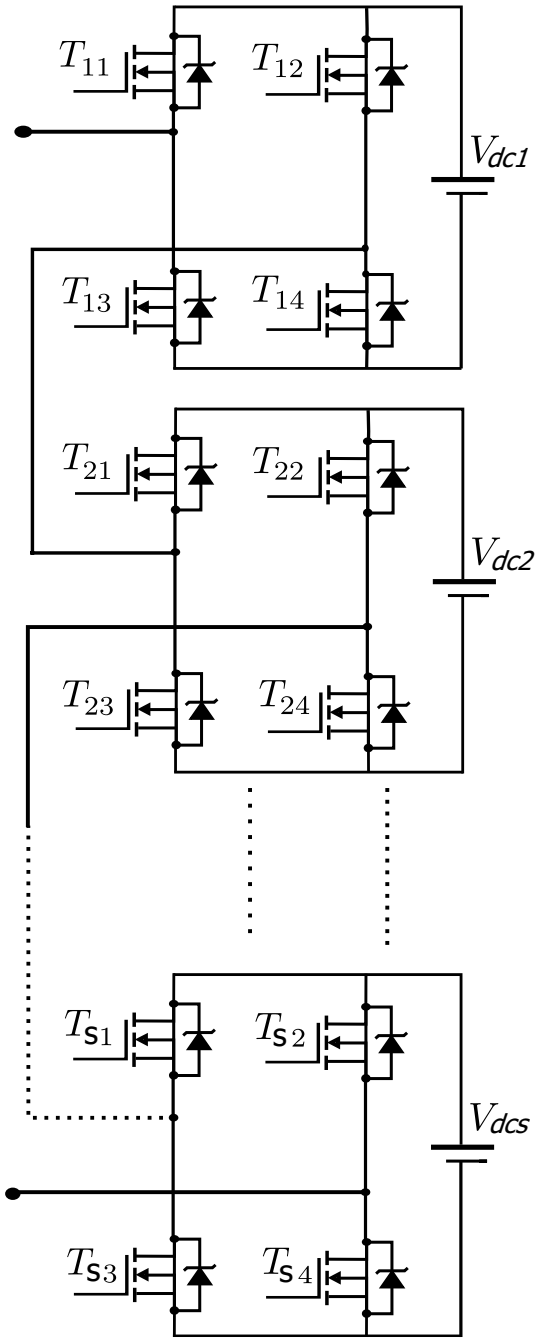


Figure 5.14: Single-phase l-level inverter configuration.

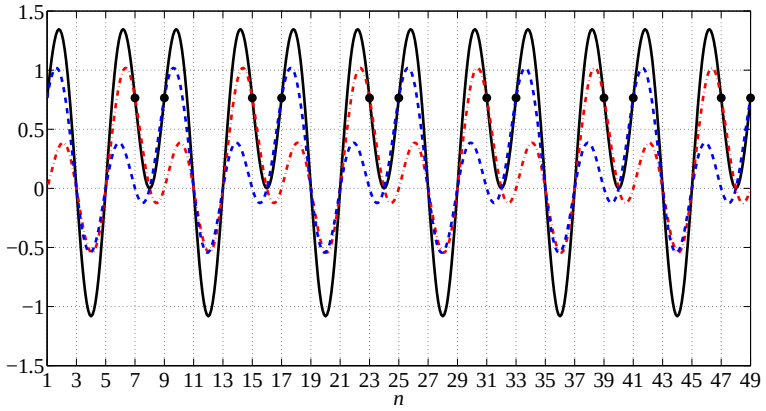


Figure 5.15: Graphs of formula (5.29) obtained for 5-level inverter.

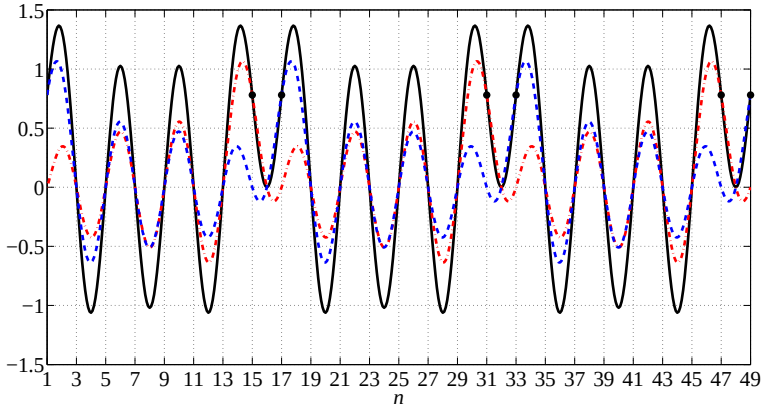


Figure 5.16: Graphs of formula (5.29) obtained for 9-level inverter.

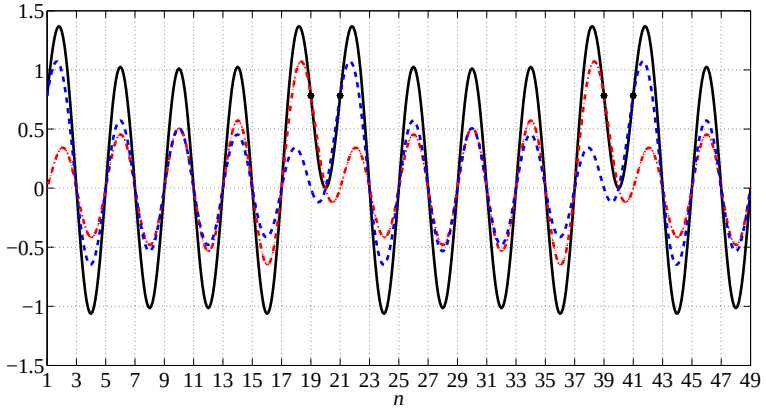


Figure 5.17: Graphs of formula (5.29) obtained for 11-level inverter.

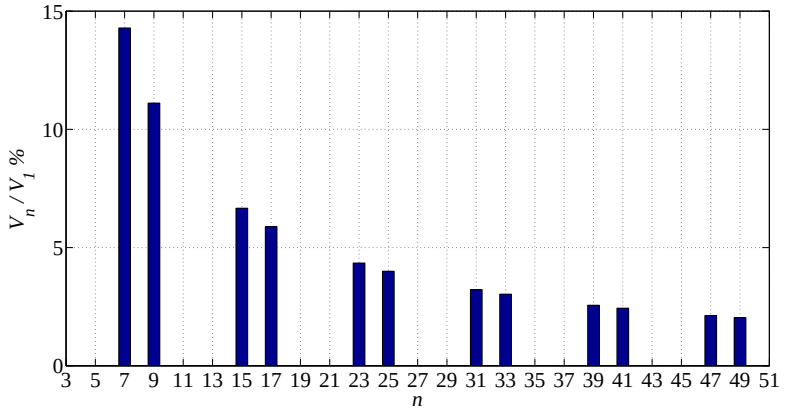


Figure 5.18: Spectrum analysis for a 5- level inverter.

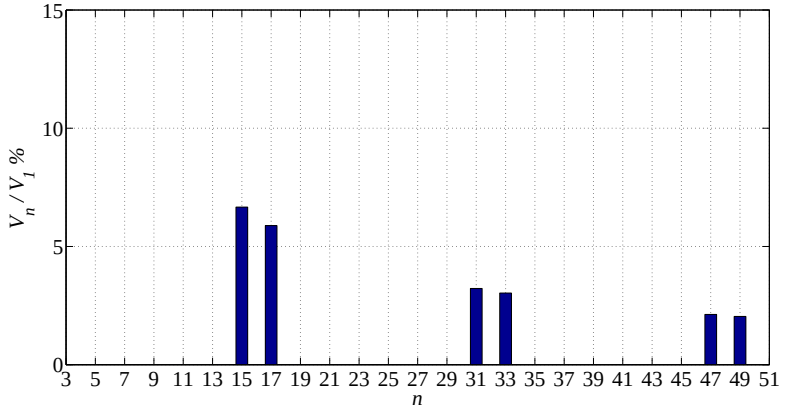


Figure 5.19: Spectrum analysis for a 9- level inverter.

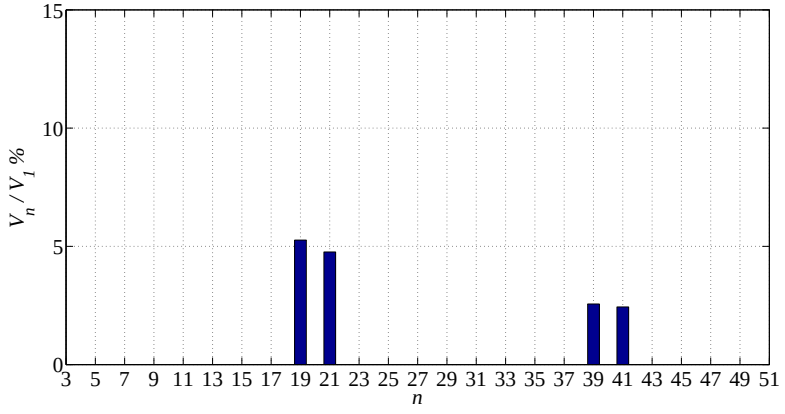


Figure 5.20: Spectrum analysis for a 11- level inverter.

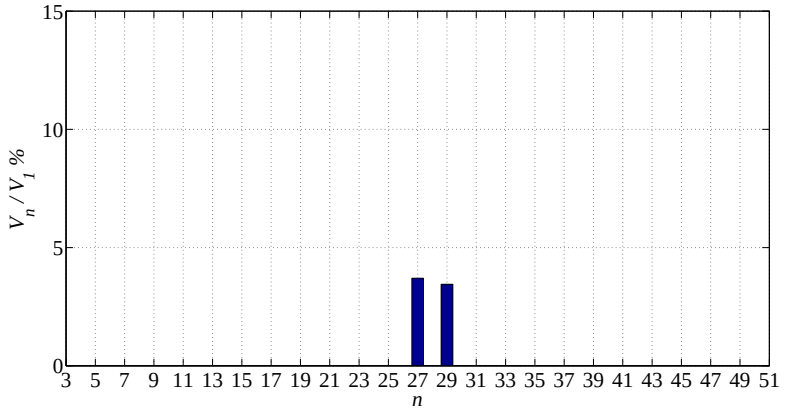


Figure 5.21: Spectrum analysis for a 15- level inverter.

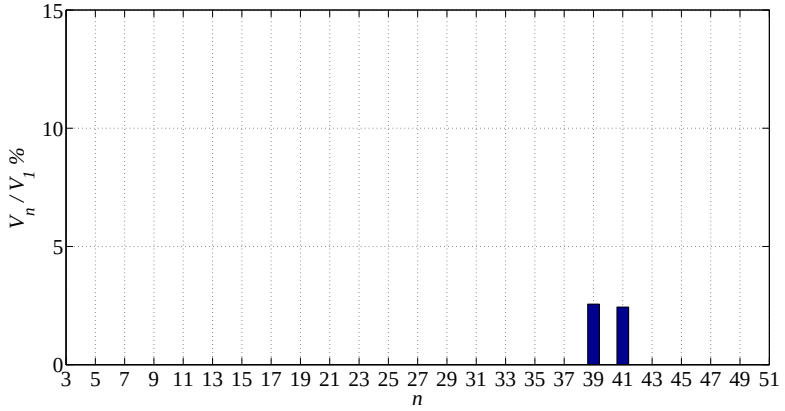


Figure 5.22: Spectrum analysis for a 21- level inverter.

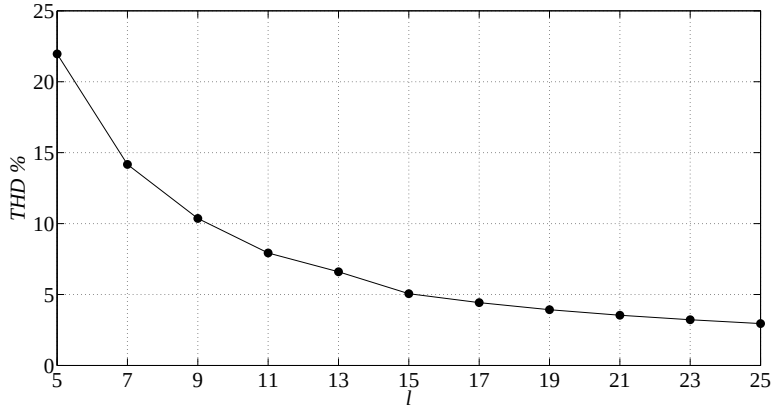


Figure 5.23: $THD\%$ depending on number of levels.

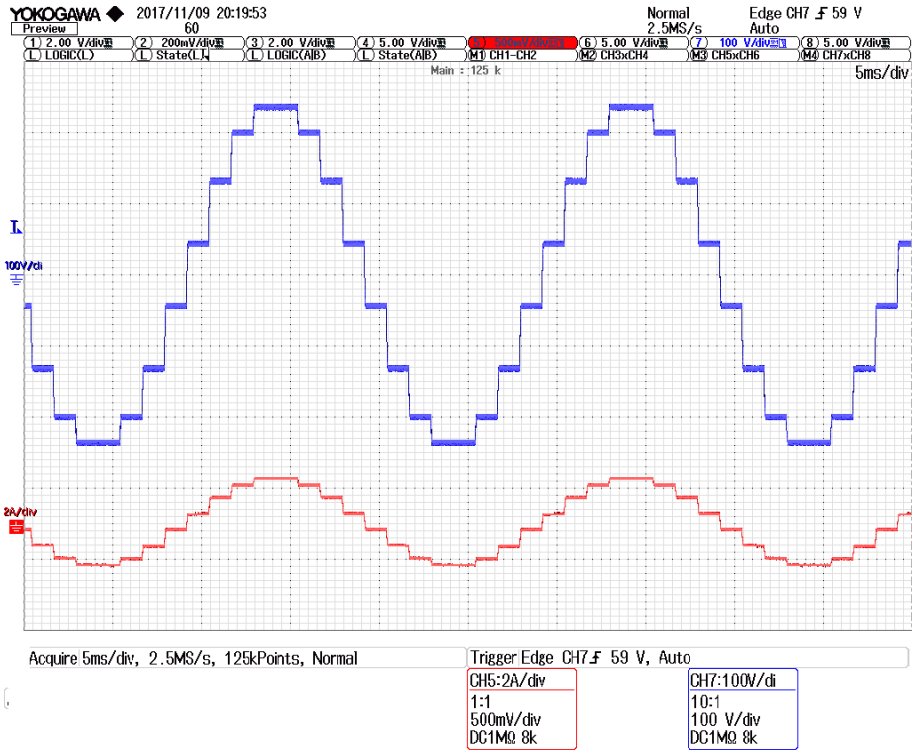


Figure 5.24: Voltage and current waveforms.

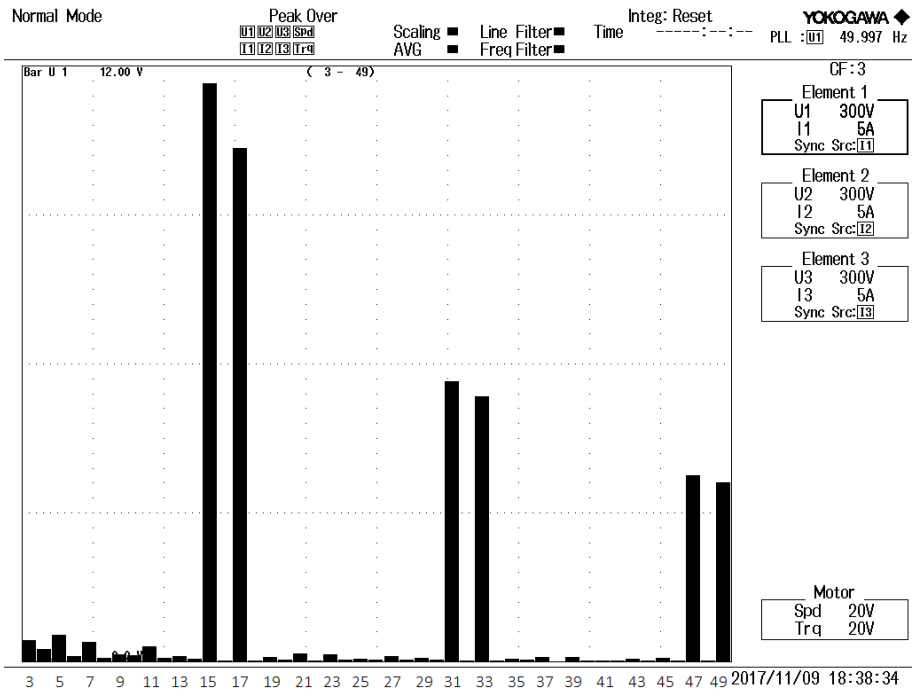


Figure 5.25: Harmonic spectrum in open condition.

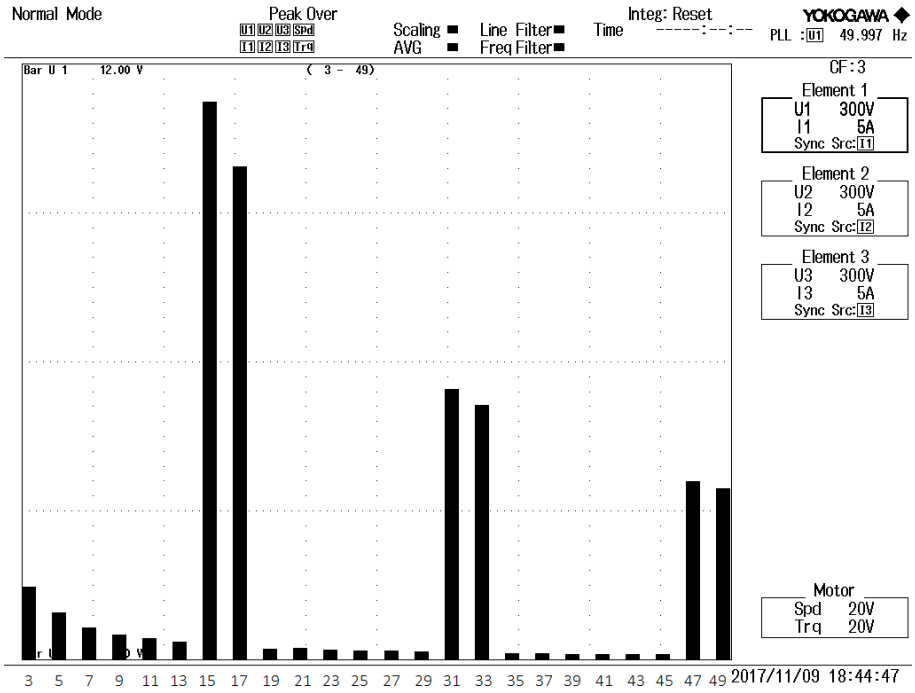


Figure 5.26: Harmonic spectrum in load condition.

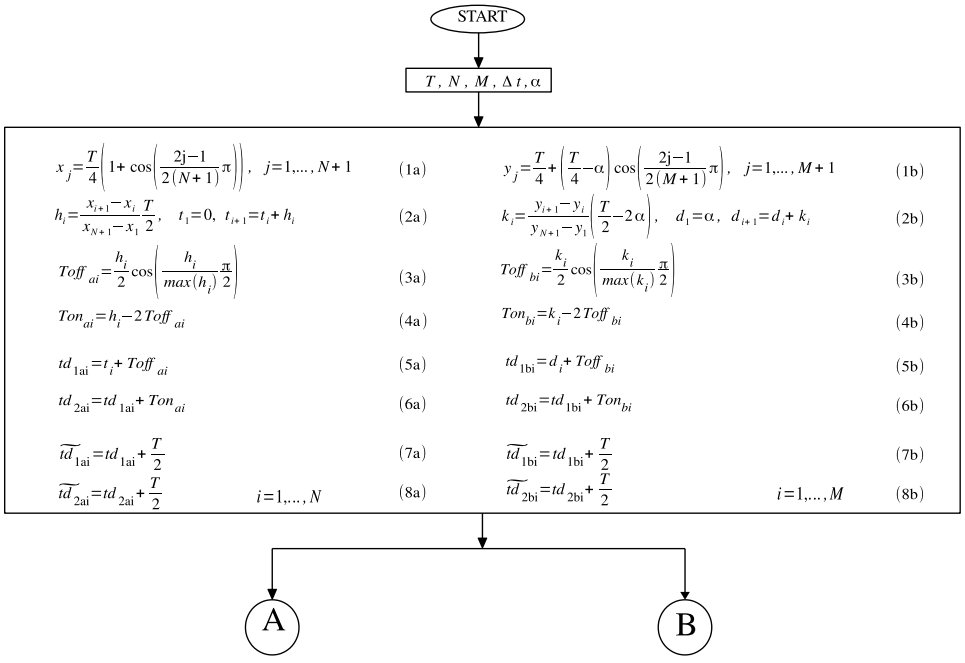
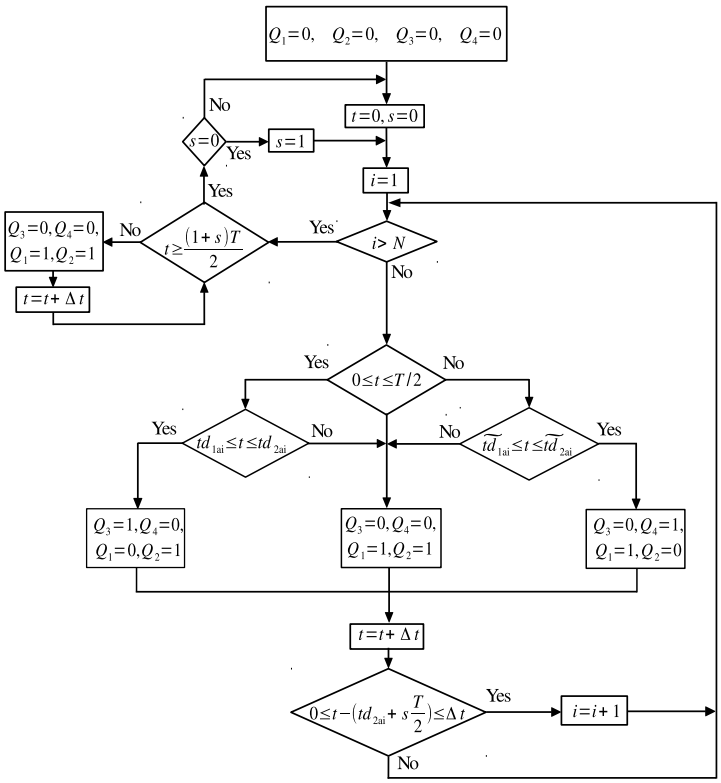
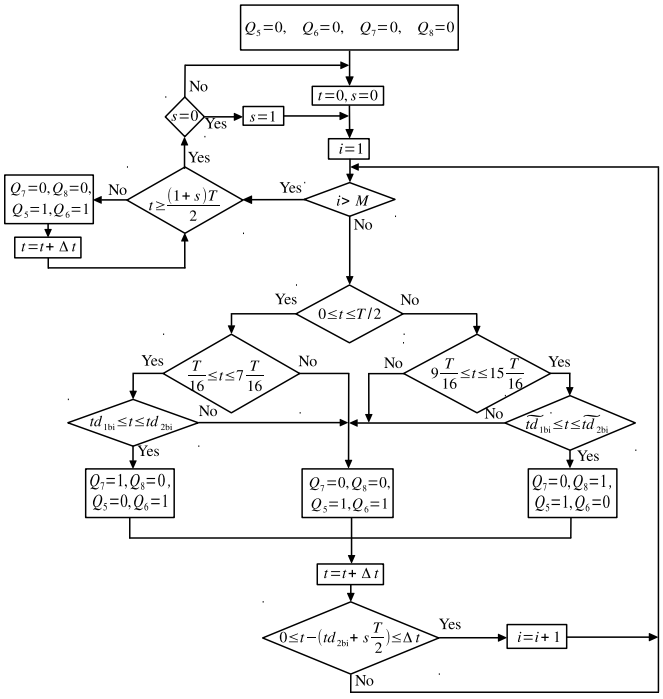


Figure 5.30: CMT flowchart.



(a)



(b)

Figure 5.31: CMT flowchart: (a) part A of Fig. 5.30, (b) part B of Fig. 5.30.

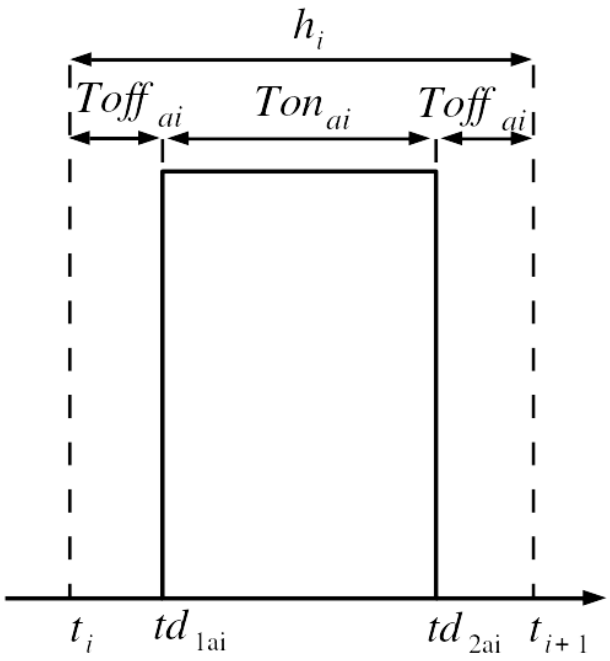


Figure 5.32: Single pulse in $[0, T/2]$.

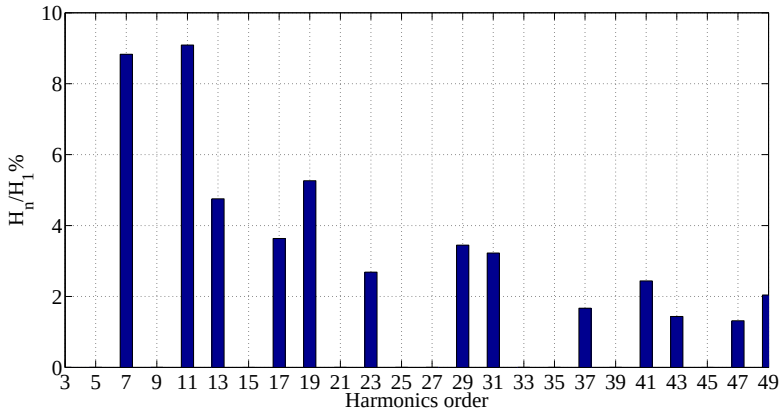


Figure 5.39: Harmonics amplitude H_n respect to the fundamental H1, for the 5-level inverter.

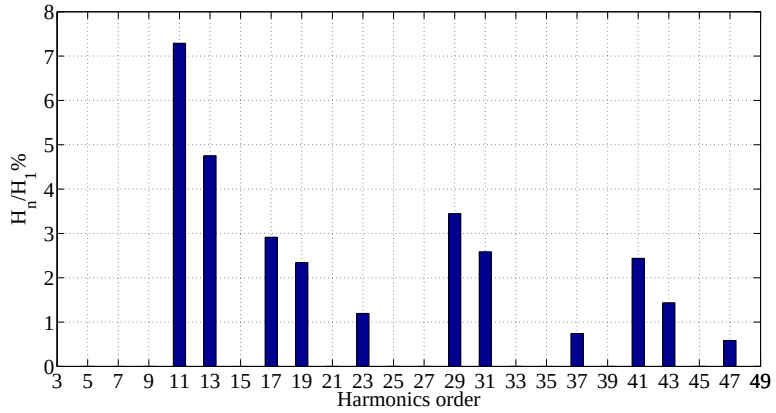


Figure 5.40: Harmonics amplitude H_n respect to the fundamental H1, for the 9-level inverter.

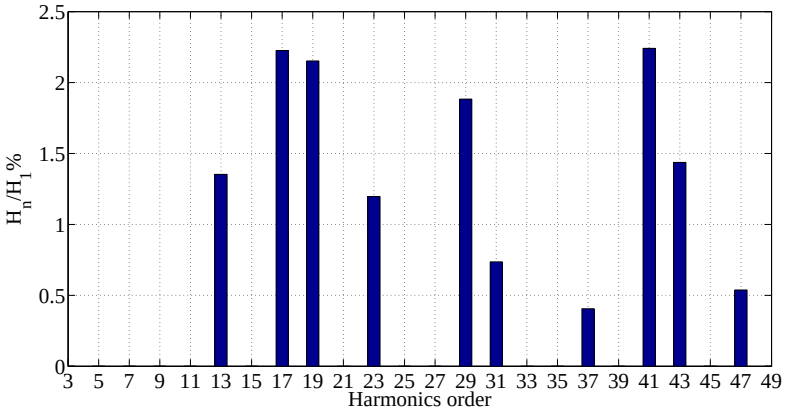


Figure 5.41: Harmonics amplitude H_n respect to the fundamental H1, for the 17-level inverter.

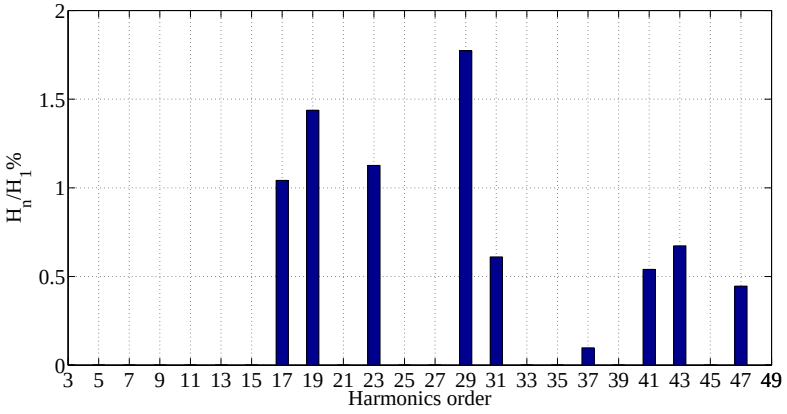


Figure 5.42: Harmonics amplitude H_n respect to the fundamental H1, for the 33-level inverter.

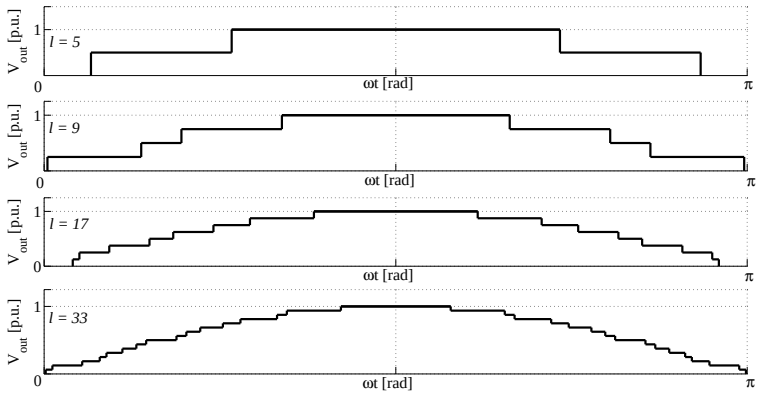


Figure 5.43: Output voltages for 5-level, 9-level, 17-level and 33-level inverters.

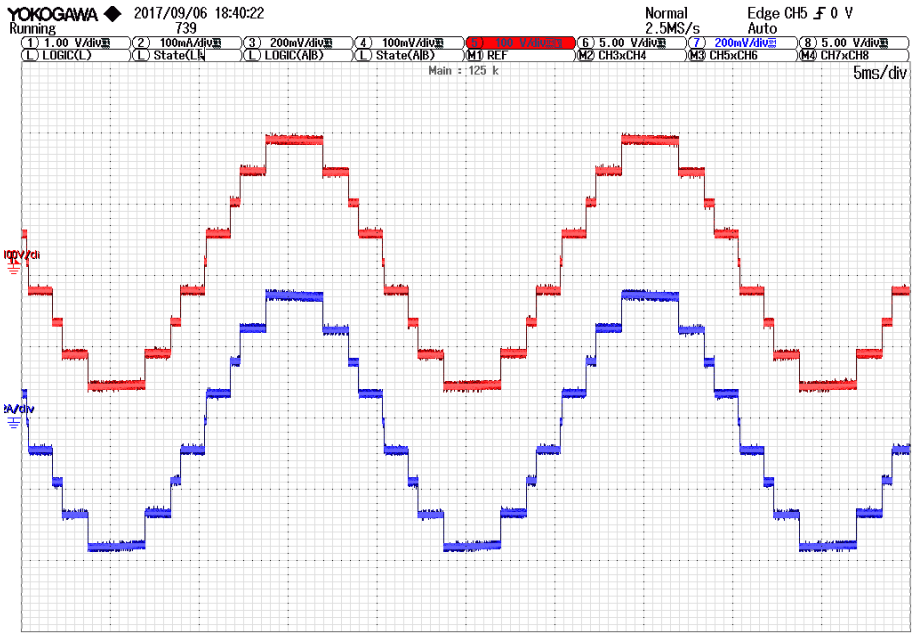


Figure 5.44: Output voltage and current waveforms.

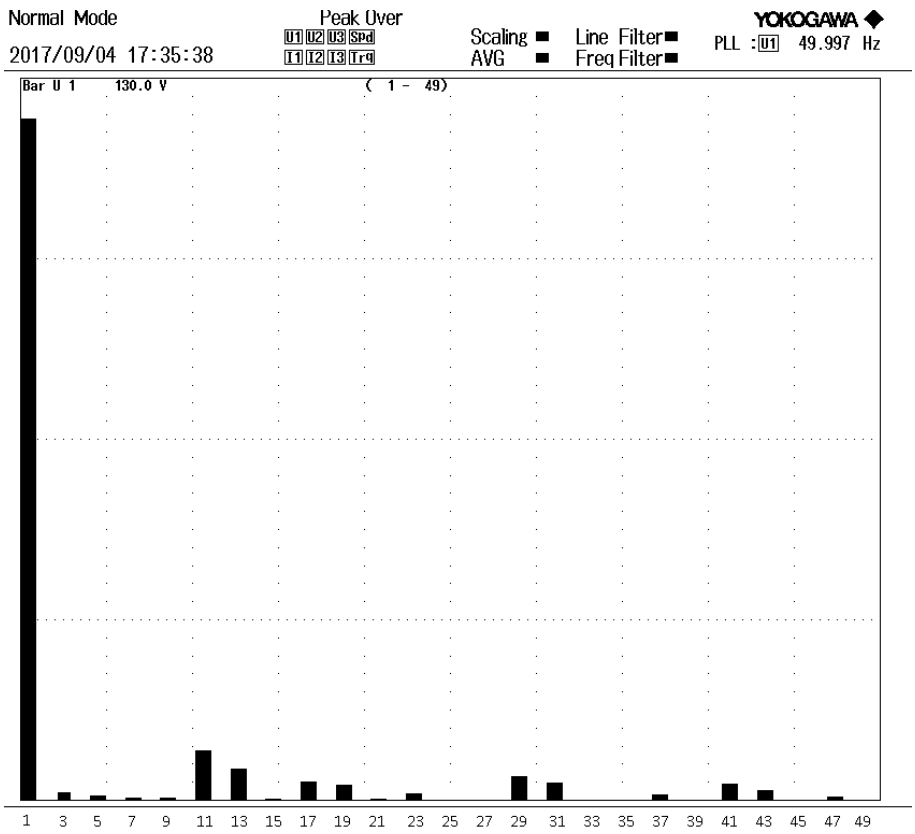


Figure 5.45: Harmonic analysis of the output voltage waveform shown in Fig. 5.44.

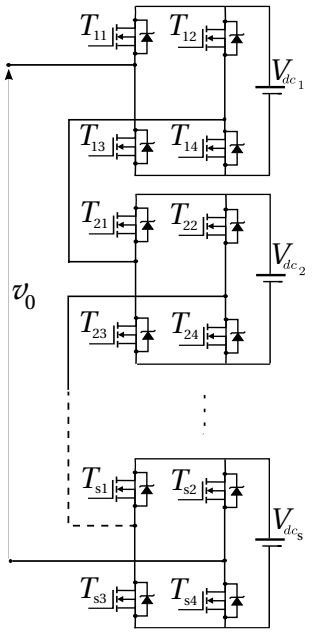


Figure 5.46: Multilevel inverter configuration.

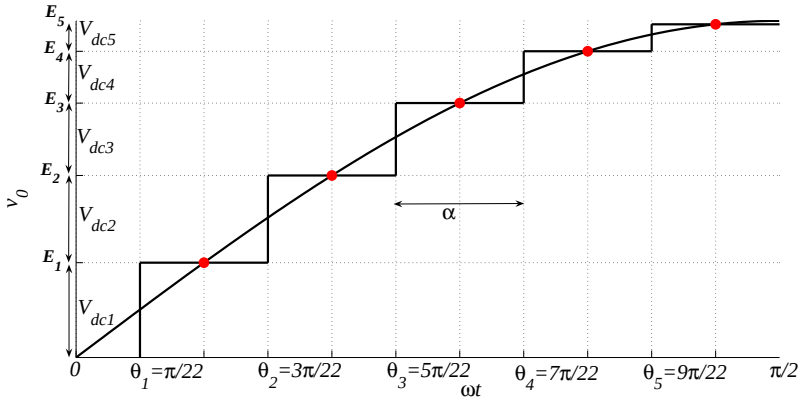
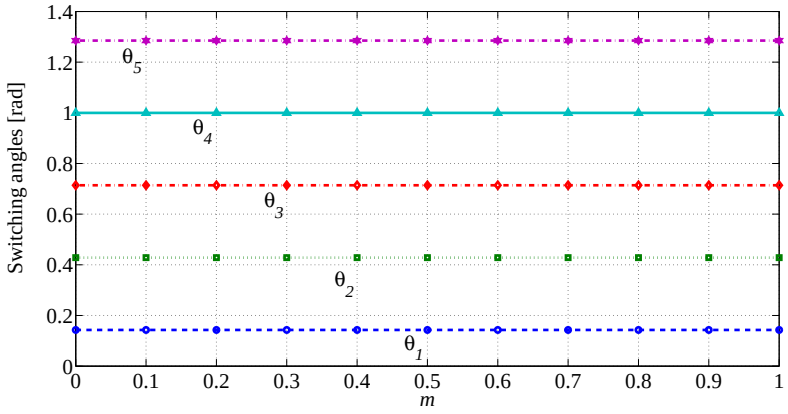
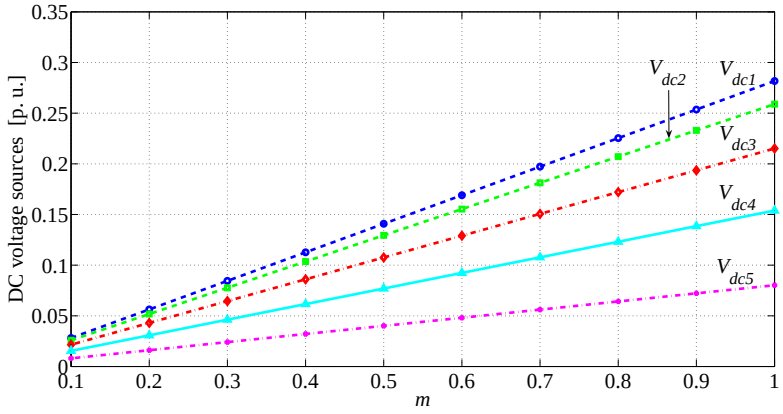


Figure 5.47: 11-level inverter output voltage waveform.

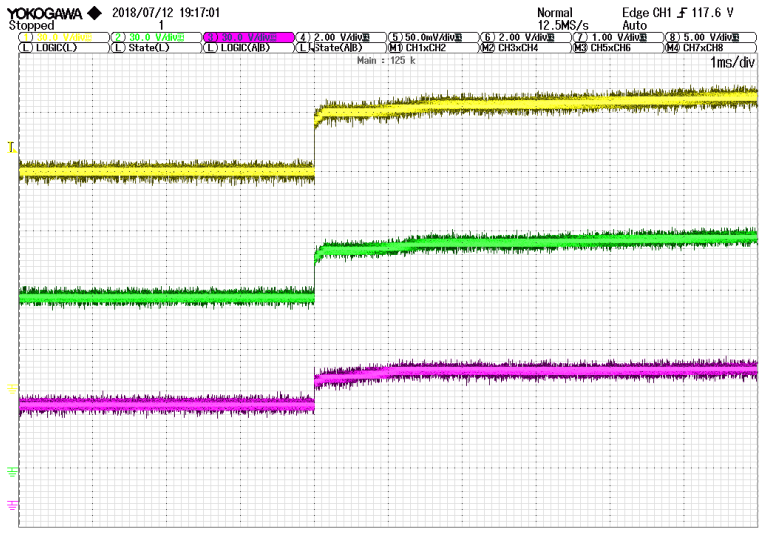


(a)

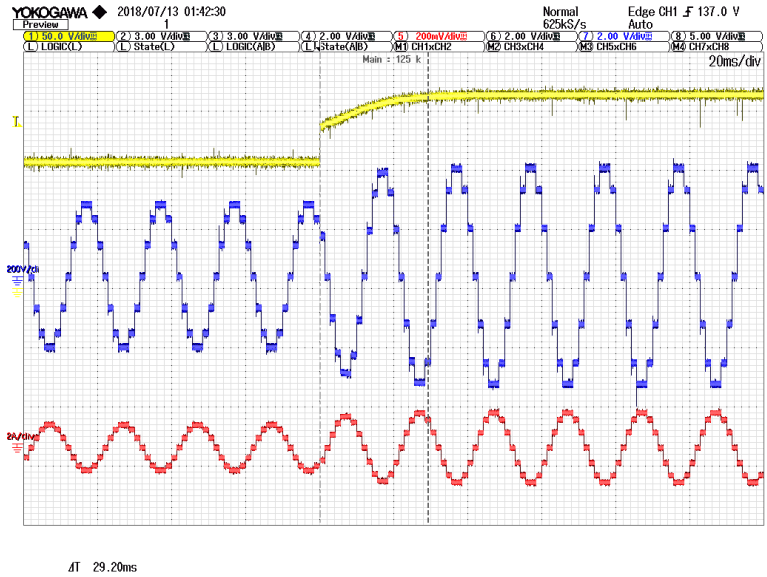


(b)

Figure 5.49: Variation of (a) switching angles and (b) DC voltage sources with m in 11-level CHB inverter.



(a) DC voltage sources steps corresponding to a modulation index variation from $m = 0.64$ to $m = 1$



(b) Output voltage (blue line) and current (red line) waveforms

Figure 5.62: Transient response.

6 Main Control Board Design

6.1 Overview

The development of modular multilevel converters, requires the implementation of complex modulations and control algorithms chapter 4, which must be executed in "real time". Moreover, based on the kind of application, there is a flow of very high number of signals between the multilevel converter and the control board, e.g. measurements of the electrical quantities, fault signals, status information of each module etc. The more number of levels increases, the more required computational effort grows. This implies that in a complex system such as a multilevel converter, it is necessary to use a logic unit which is able to generate, to receive and to elaborate a huge number of data.

In low number of level converters, it is possible to use a Digital Signal Processor (DSP), a specialized microprocessor with an optimized architecture for the operational needs of digital signal processing. DSPs can have different levels of performance and they are classified according to the type of data that they are able to process (e.g. a 32bit DSP refers to a unit that is able to deal with 32 bit digital signals). The computational power of modern DSP is very high but this kind of processors have a very limited numbers of GPIO pins available in their pinout and this is a limiting factor when the numbers of level of the multilevel converter increases. Typically with a high performances DSP it is possible to control up to a 5-level three phase system. For higher levels applications it is mandatory to use a Field Programmable Gate Array (FPGA) device.

The multilevel converter presented in this thesis (see chapter 8) has been designed for a Static Synchronous Compensator (STATOM) application. It is a 33 level three-phase system, thought to be connected to the power grid. This implies that each phase is composed by 16 H-bridge modules. Each of them requires 4 modulation signals, 2 spi channels for the transmission of the local electrical quantities, a reset signal, several status signals and a synchronization signal. In addition to this huge number of information that comes from each H-bridge module of the system, the main control board has to constantly receive measurements from the power grid in order to provide a synchronization between the output of the converter and the grid voltage waveform. In the next sections the structure of the main control board is described in all its features.

6.2 Hardware Architecture of the Proposed Multilevel Converter

Before to discus the architecture of the main control board, it is necessary to explain the architecture of the whole converter and so the hardware architecture of the 33 level three-phase converter proposed in this thesis is shown in this section. The multilevel converter itself, is composed by 48 H-bridge modules (16 for each phase) and each of them is provided of a local DSP control unit which is in charge of acquiring all the local measurements of the electrical quantities and send them to the main FPGA based control board with an SPI interface. Moreover, the system involves three external measurement boards that are necessary for the interface of the power converter with the power grid: the first one is directly connected to the power grid, the second one in placed in series at the output of the multilevel converter and the third one is connected near the load that has to be stabilized by the STATCOM. The scheme of the proposed hardware architecture is shown in Fig. 6.1. In the architectural scheme it is possible to notice (in red) how many signals exchanged between the main control board and the system:

- 36 signal for the SPI communication between the external measurement boards an the main control board
- 176 signals for the modulation and control of each phase of the multilevel converter

This mean that the the main control board has to deal simultaneously with 564 signals. It's a very challenging task for the main control board. Its structure is presented in the next section.

6.3 Architecture of the Main Control Board

In order to fulfill the heavy tasks the control board shall meet, it is not only made by an FPGA device as previously mentioned. The huge complexity of the system requires more computational capability and GPIO availability than any commercial FPGA device. For this reason, the main control board is equipped with an FPGA, a CPLD and a DSP device that cooperates in order to satisfy the system requirements. A block diagram of the proposed solution is shown in Fig. 6.2 and a summary of the main tasks of each module are listed below:

- The FPGA is in charge to collect all the measurement and status information that comes from the system and to compute the control algorithm for the required application. In the specific case of proposed prototype the FPGA is computing a STATCOM control algorithm but the flexibility and the extreme modularity of the system allow to reconfigure the converter for other kind of applications, such as for motor control purposes, simply changing the control

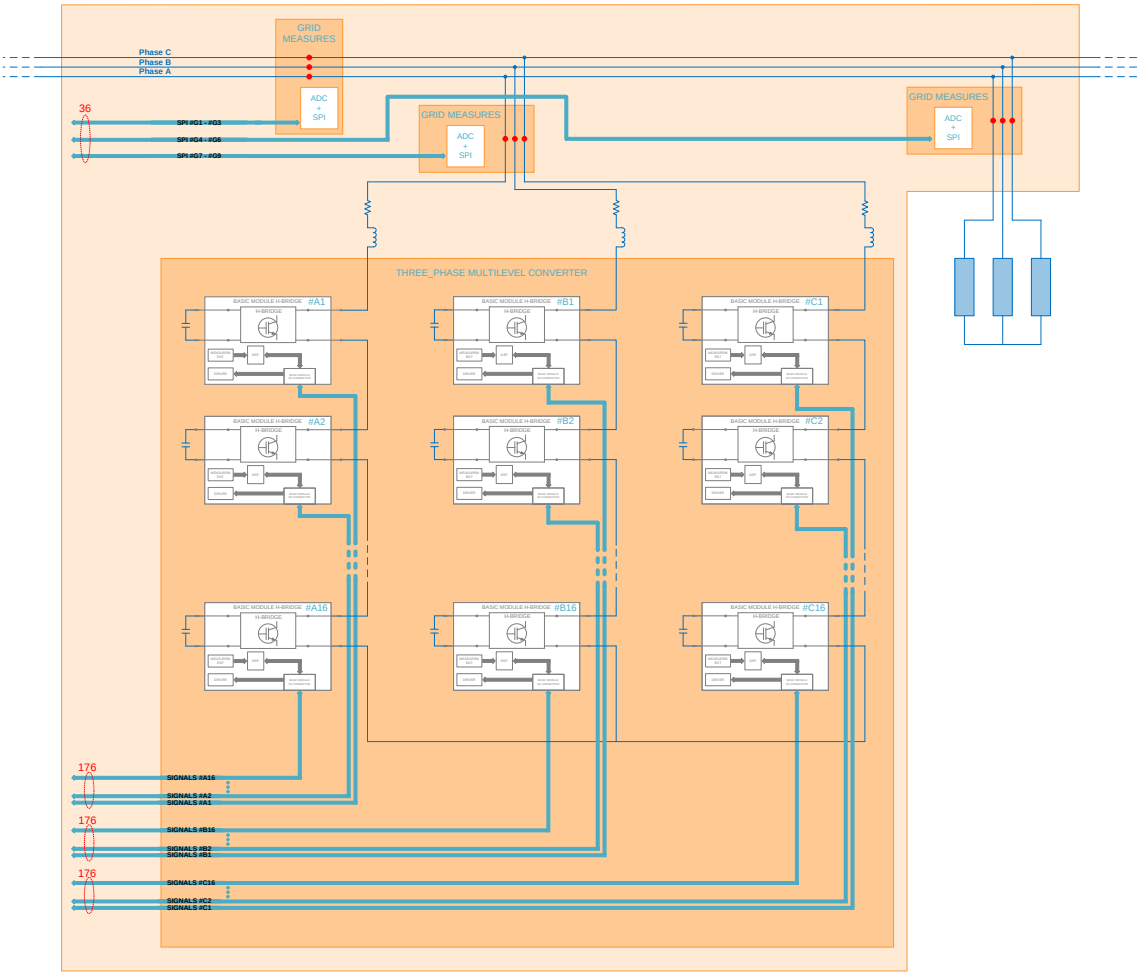


Figure 6.1: HW architecture of the system.

algorithm on the FPGA device. The tasks of the FPGA device are listed in detail below:

1. It receives through the SPI interface “SPI MASTER #GRID” the current and voltage measurements of the power grid. This information are then used to compute the control algorithm of the system.
2. It receives through the SPI interface “SPI MASTER #A” the measurements of the DC bus voltages of each H-bridge of the phase A.
3. It receives through the SPI interface “SPI MASTER #B” the measurements of the DC bus voltages of each H-bridge of the phase B.
4. It receives through the SPI interface “SPI MASTER #C” the measurements of the DC bus voltages of each H-bridge of the phase C. This values are then used together with the information received from the phase A and B to compute a DC voltage balancing control algorithm. It is necessary to avoid any kind of voltage unbalancing in the DC links of the

H-bridge modules.

5. It generates a synchronization signal called “time tick” with is sent to the CPLD. This signal is then forwarded to all the H-bridge and it is necessary to keep the right synchronism in the whole system.
6. It manages the alarm of the system. Each H-bridge can send an alarm signal when a fault occurs and the FPGA is able to identify the problem and can decide to disconnected the damaged H-bridge module or to turn-off the whole system.
7. When the problem related to a fault signal described above results in a false alarm or in a temporary problem (e.g. a lose of synchronization) the FPGA can send a reset command to the involved H-bridge module.
8. It manages a memory interface with the DSP, which provide to the FPGA the information required for the synchronization of the output voltage of the system with the power grid.
9. It manages the UART interface.
10. It manages the RS232 interface.
11. It manages the Ethernet interface.
12. It manages the LCD interface.

- The CPLD has the role of GPIO expander for the FPGA device. In fact the FPGA pinout is not able to satisfy alone the huge number of output required signals alone (switching command patterns, synchronization signals, reset signals etc.).
- The DSP architecture, which is optimized for the operational needs of digital signal processing, is exploited to compute a Phase-Locked Loop (PLL) algorithm in order to synchronize the output of the multilevel converter with the power grid voltage waveform. The information extracted from the power grid measurements by the DSP are sent to the FPGA, which use it as an input parameter for the control algorithm.

The complete architecture of the system, composed by the power converter itself and the main control board is shown in Fig. 6.3 and in Fig. 6.4 is presented in a detailed version.

6.4 Main Control Board Characteristics

In this section are reported the characteristics of the devices which make up the main control board.

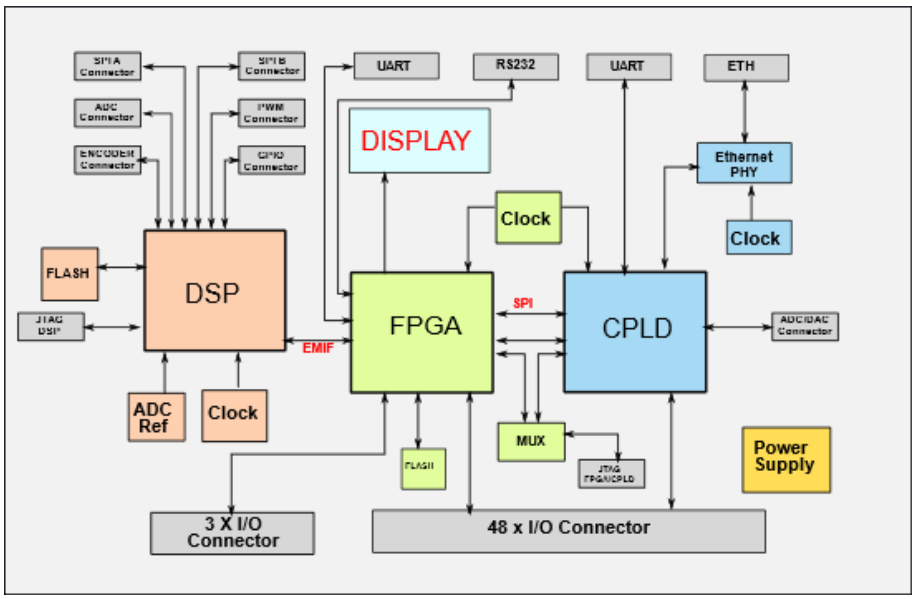


Figure 6.2: Block diagram of the main control board.

6.4.1 FPGA Device

The selection of the FPGA during the design of the control board has been based on the following considerations:

- The amount of logic that was necessary to synthesize and to implement all the required functionalities described in sec. 6.3.
- The number of pins required to interface the FPGA board with the whole system (in sec. 6.2has been shown that are required 564 I/O signals).
- The cost of the different devices on the market.

The choice fell on an Altera CYCLONE V FPGA 5CEFA7F31. Its characteristics are shown in Tab. 6.1 ,while Fig. 6.5 shows the pin planner of the device.

6.4.2 CPLD Device

The selected CPLD device is the ALTERA MAX 10 10M16DAF484. The main strong points of this family of devices are:

- Integrated dual configuration flash
- Availability of a user flash memory
- Integrated Analog to Digital Converters (ADCs)
- Availability of a support for soft core processors like Nios II

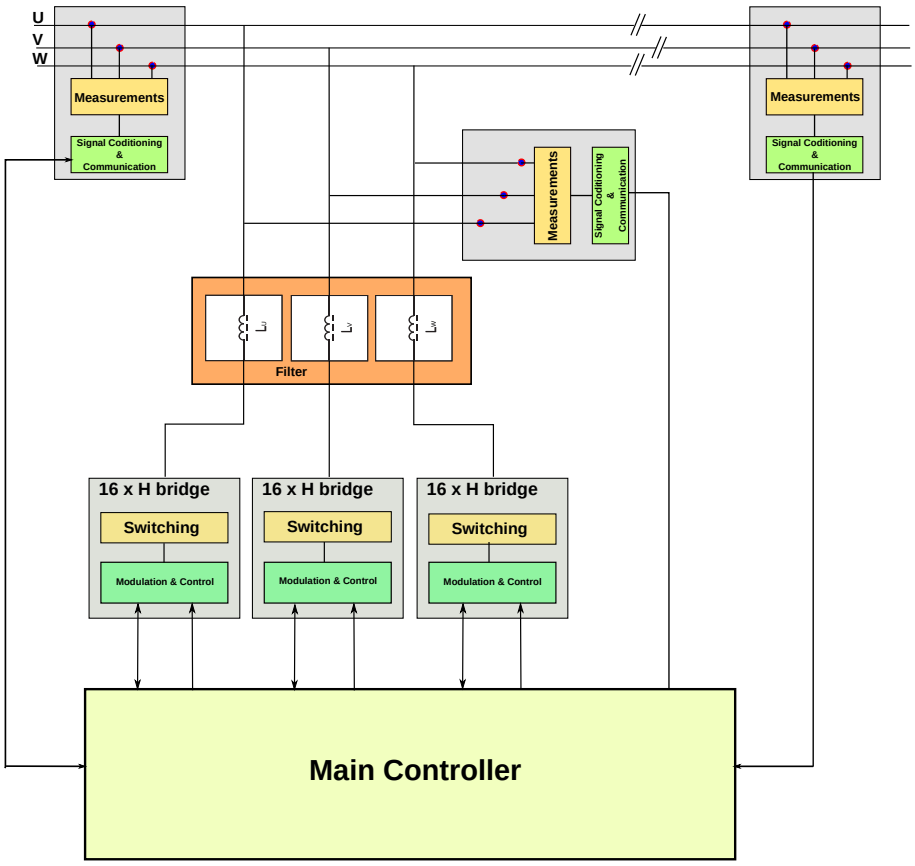


Figure 6.3: Architecture of the system.

This family represents the ideal solution for problems of system management, I/O expander, control algorithm implementation and communication management. The main characteristics of the selected device are listed in Tab. 6.2 and its pinout is shown in

6.4.3 DSP Device

Texas Instruments TMS320F2837xS Delfino 32-Bit Microcontrollers are powerful floating-point MCUs that lets designers consolidate control architectures. They also eliminate multiprocessor use in high-end systems. The real-time control subsystem is based on TI's 32-bit C28x floating-point CPU, which provides 200MHz of signal processing performance. The C28x CPU is further boosted by the new TMU accelerator. This enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations. It also includes a VCU accelerator, which reduces the latency for complex math operations common in encoded applications. The F2837xS features a real-time control accelerator, also known as CLA. The CLA provides an additional floating-point accelerator used to run parallel time-critical control algorithms. This provides bandwidth for the C28x to focus on

Table 6.1: Characteristics of the CYCLONE V FPGA 5CEFA7F31.

LEs(k)	149.5
ALMs	56480
Registers	225920
M10k memory blocks	686
M10k memory (kb)	6860
MLAB memory (kb)	836
DSP blocks	156
18x18 multipliers	312
Global clock networks	16
PLLs	7
LV DS channels (receiver/transmitter)	120/120
Hard memory controllers	2
Package	F896
GPIO	480

system tasks. The TMS320F2837xS supports up to 1MB of on-board flash memory with error correction code (ECC) and up to 164KB of SRAM. Two 128-bit secure zones are also available on the CPU for code protection.

The functional diagram of the Delfino TMS320F2837xS is shown in Fig. 6.7.

6.5 Main Control Board Prototype

The prototype of the main control board is shown in Fig. 6.8 and in Fig. 6.9, respectively in the top and bottom view. Because of the high number of signals involved in the circuit, the PCB has been designed in 12 layers. On the top view

Table 6.2: Characteristics of ALTERA MAX 10 10M16DAF484

LEs(k)	16
Block memory (kB)	549
Registers	225920
User flash memory (kB)	32-296
18x18 multipliers	45
PLLs	4
Internal configuration	Dual
ADC	1
External Memory Interface (EMIF)	Yes
GPIO	320
LVDS channels (receiver/transmitter)	22/116

it is possible to observe the three logical devices: the FPGA, the CPLD and the DSP. On the bottom are mounted the 48 connectors where each H-bridge module is connected through its own cable, allowing the exchange of all the data and the modulation patterns.

6.6 Summary

In this chapter has been presented the hardware architecture of the main control board of the 33-level three-phase prototype realized at Digipower Ltd. It is composed by three main devices: an FPGA, a CPLD and a DSP. All of them has been described from the point of view of both, their structure and their tasks in the control architecture.

Finally, the main control board prototype has been shown.

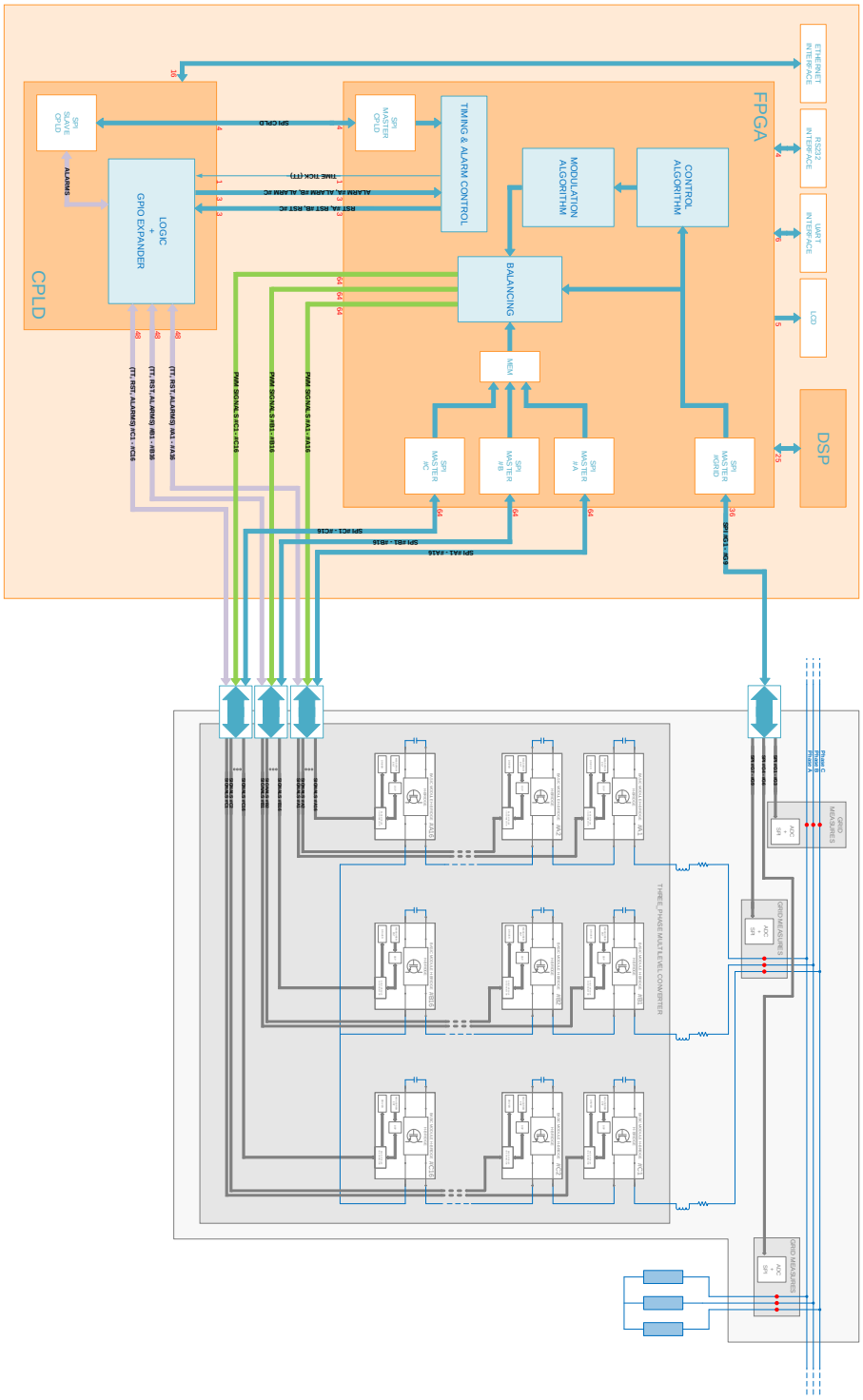


Figure 6.4: Detailed architecture of the system.

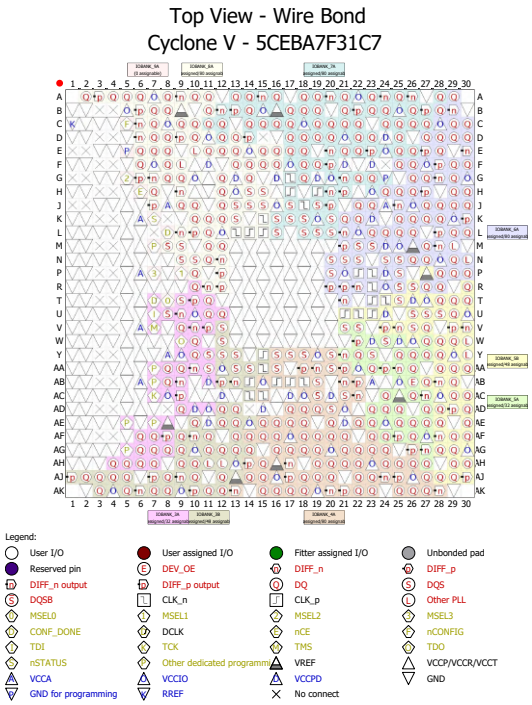


Figure 6.5: Pin planner of CYCLONE V FPGA 5CEFA7F31[329]

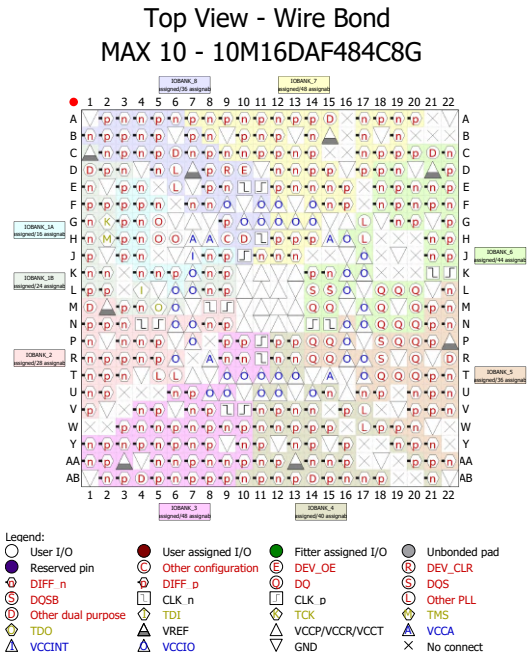


Figure 6.6: Pin planner of ALTERA MAX 10 10M16DAF484[329]

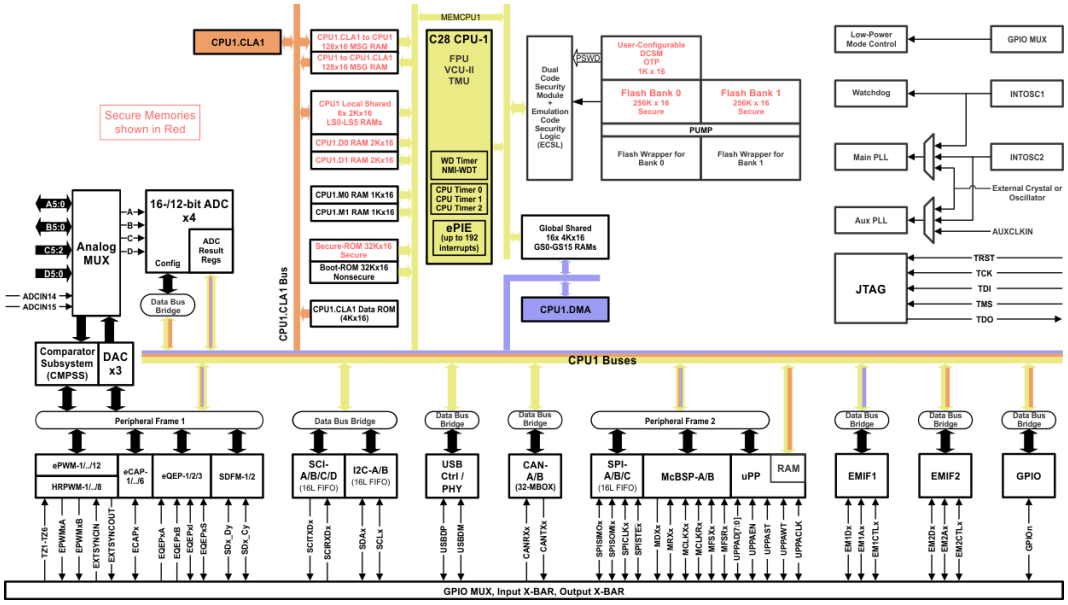


Figure 6.7: TMS320F28377S - Functional Diagram [330]

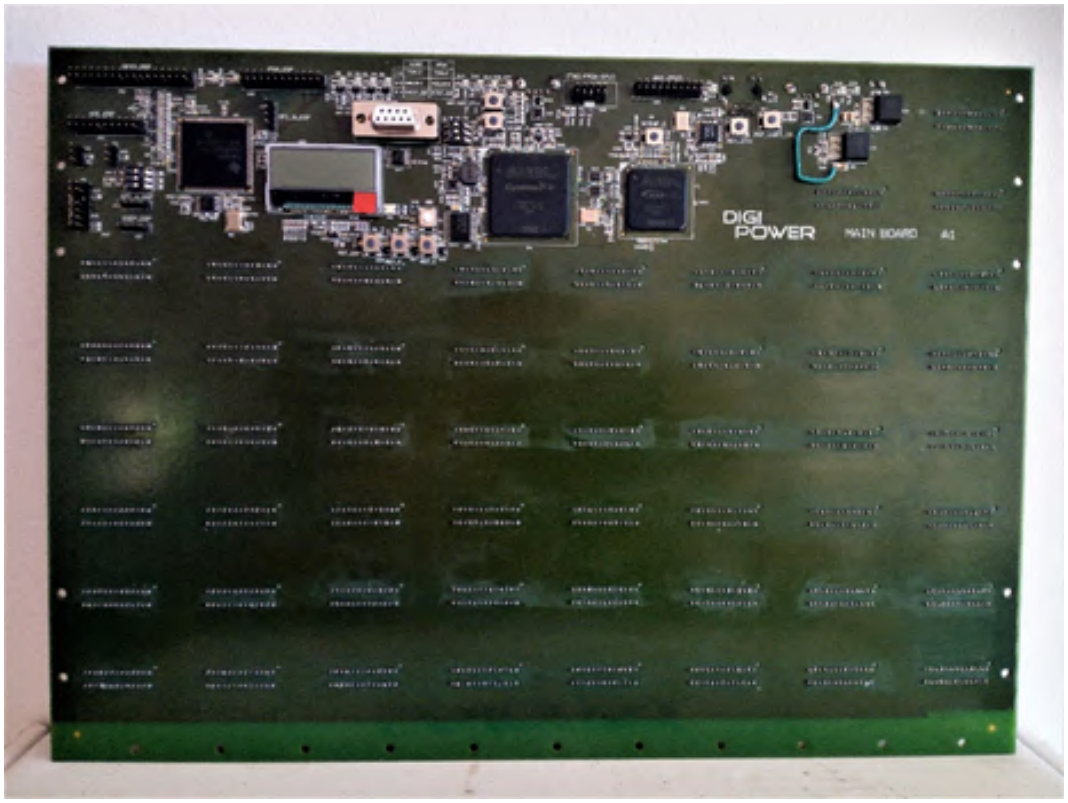


Figure 6.8: Main control board prototype (top view)

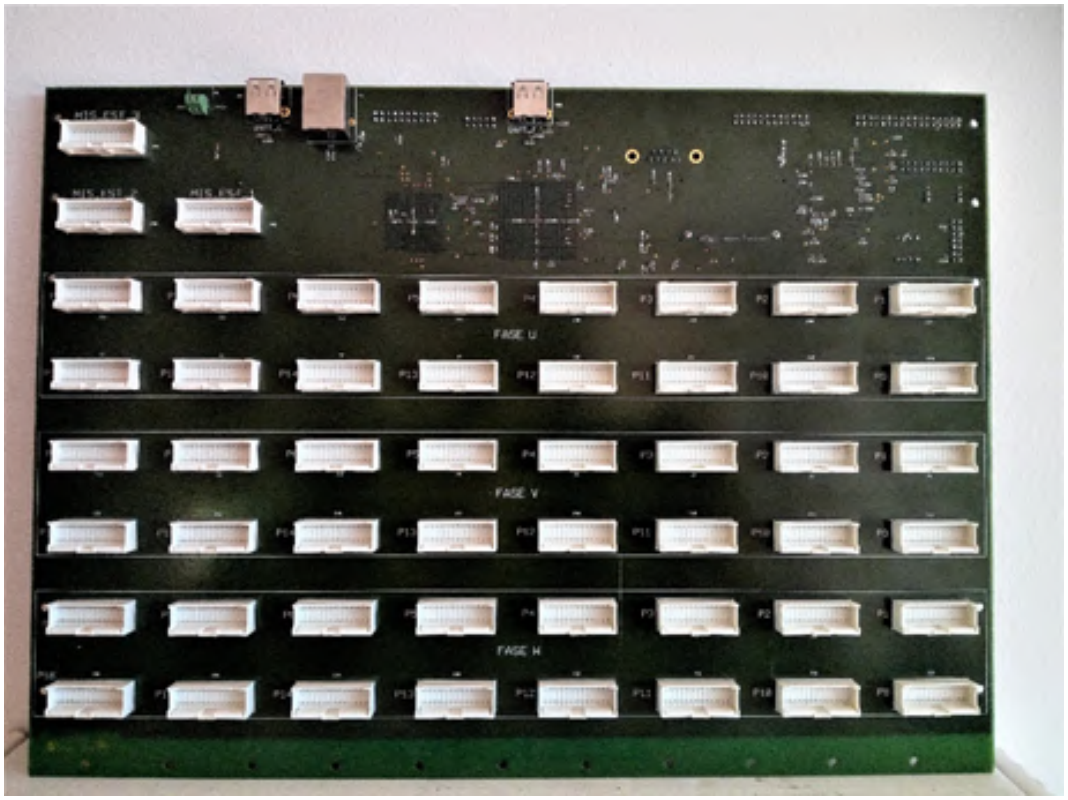


Figure 6.9: Main control board prototype (bottom view)

7 Experimental Prototype

7.1 Overview

In this chapter is shown the experimental prototype of the 33-level three phase multilevel converter prototype carried out at DigiPower s.r.l. labs. The work presented in this chapter is the synthesis of almost 2 year of hard work which involved several phases: starting from the system simulation, passing through the hardware and the mechanical design, until reaching the testing phase.

The achieved results have allowed to carry out with success the CoMoDes Project which have been formally concluded in August 2019. Anyway this was just a first step of the more ambitious goal to bring on the market of power electronic devices a multilevel converter system, fully developed at Digipower s.r.l.

7.2 H-bridge Module

The whole project has been developed with the clear aim to realize a system with a very high level of modularity and flexibility. The H-bridge module is the perfect representation of this ambitious idea. Each H-bridge is completely independent from the rest of the system and it can work also as a standalone converter. It has all the features of a standard power converter module, as depicted in Fig. 7.3:

- 4 semiconductor devices
- 2 driver circuits (each of them can drive 2 switches)
- 4 snubber circuits
- 1 DSP control board
- 2 over-current protection circuits (1 on the DC side and one on the AC side)
- 1 overvoltage protection circuit
- Input voltage measurement and conditioning circuit
- Output current measurement and conditioning circuit
- Status LED

The whole H-bridge module is shown in Fig. 7.1 while the individual sections of the module are highlighted in Fig. 7.2.The nominal operating conditions of the H-bridge module are listed in Tab. 7.1.

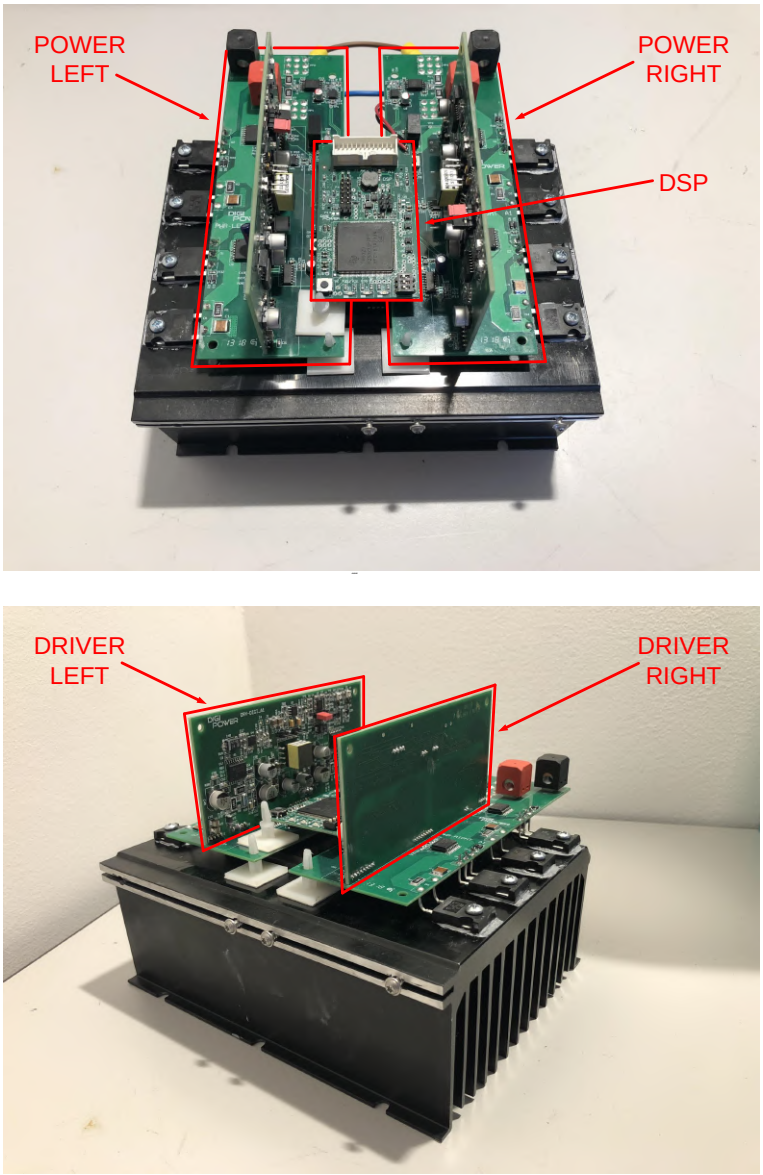


Figure 7.1: H-bridge power module.

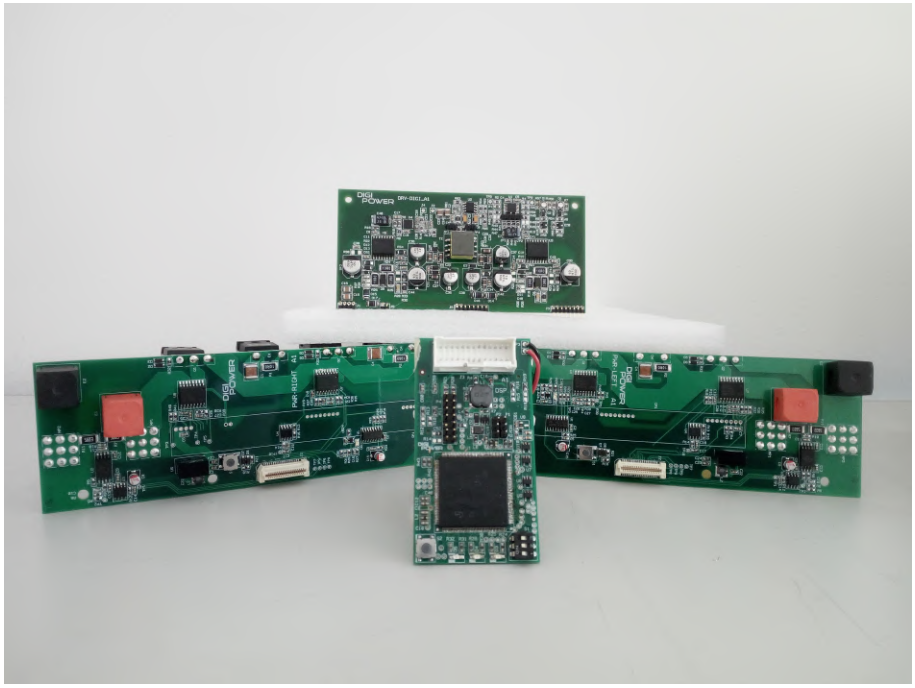


Figure 7.2: H-bridge module sections. DSP board (on the top), left power leg (on the left), right power leg (on the right), local DSP board (in the center).

Table 7.1: H-bridge module nominal operating conditions.

V_{DCnom}	600 V
I_{nom}	35 A
f_{sw}	10 kHz
T_{max}	100° C
η_{nom}	>99 %

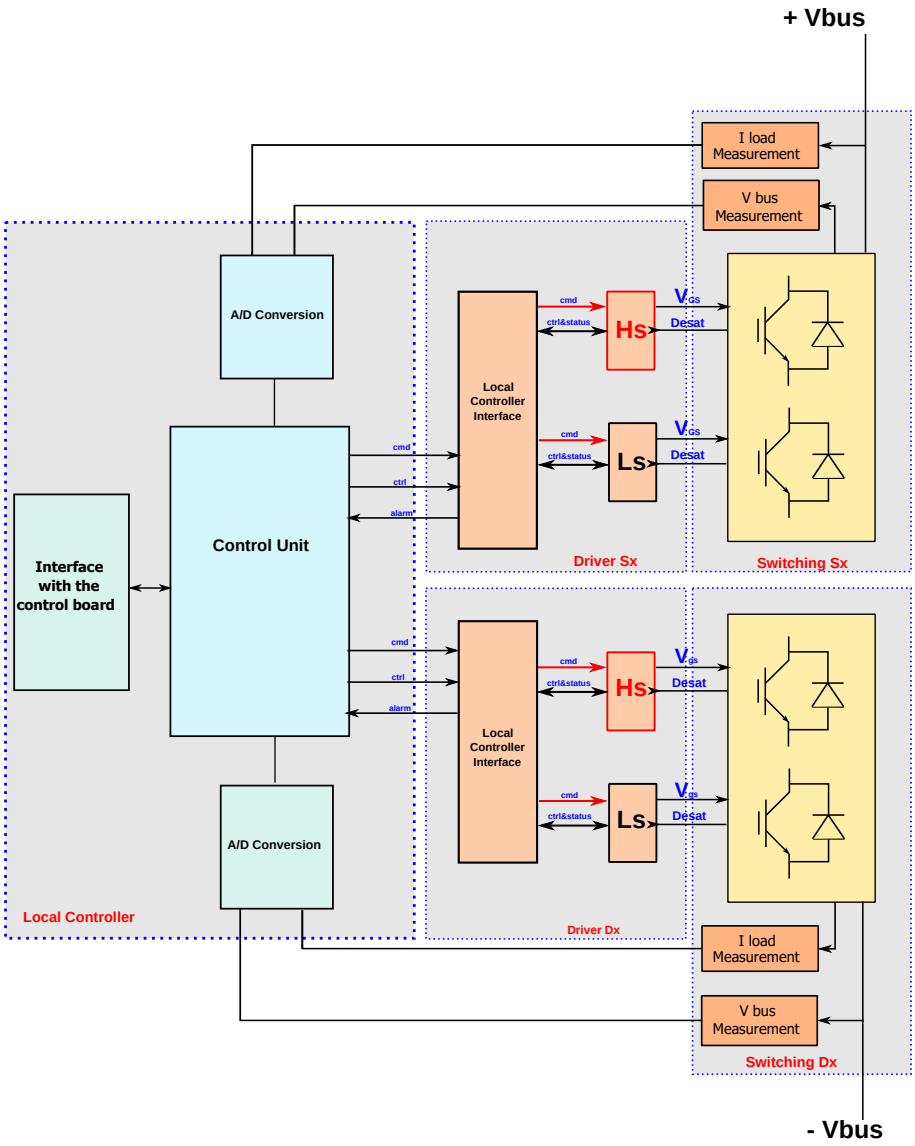


Figure 7.3: H-bridge schematic functional block.

When the H-bridge is used in a multilevel system it can easily be connected to the other modules thanks to the plug-in input and output power connectors and in this configuration the DSP board becomes a slave for the master control board (described in chapter 6). The two logic units are connected through the white I/O pin connector, located at the top of the DSP board. The exchanged signals between the main board and the local slave DSP when the multilevel configuration is used are:

- 4 gate signal patterns
- 1 voltage measurement (via SPI)
- 1 current measurement (via SPI)

- 1 synchronization signals
- 1 fault signal
- 1 reset signal
- 2 GPIO signals

7.2.1 H-bridge Module Power Tests

In this section are presented all the steps that have been done before to reach the final multilevel high power configuration. Once that the boards were individually tested, the first H-bridge module was assembled and it was tested as shown below.

7.2.1.1 Low Power test on the Single H-bridge

The first step has been the low power test. The setup is shown in Fig. 7.4 and is made by:

- H-bridge prototype module
- DC Power supply Lambda GEN600-2.6
- Auxiliary power supply ($24\,V$)
- Resistive load ($\sim 300\,\Omega$)
- Oscilloscope Yokogawa DLM4058 $2.5GS/s$, $500MHz$
- Current probe Yokogawa 701933 $50\,MHz$, $30\,A$
- Differential probe Yokogawa 700924 $1400\,V$ peak
- Power analyzer Yokogawa WT1800

The test has been done under the following conditions:

- Input DC voltage $\sim 630\,V$
- Output current $\sim 2\,A_{rms}$
- Switching frequency $10\,kHz$

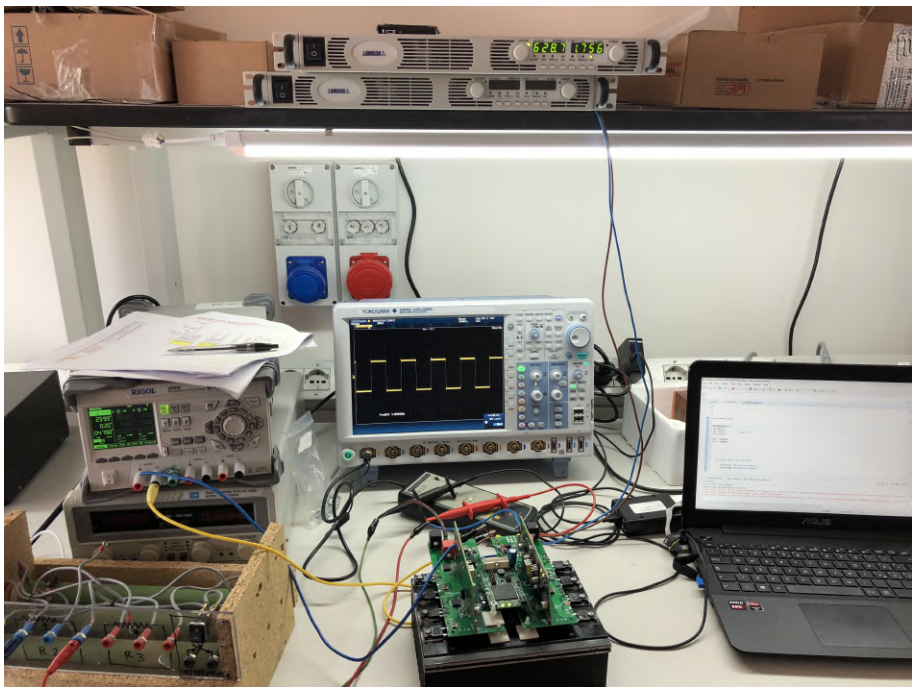


Figure 7.4: Low power test of the H-bridge module.

The power provided by the H-bridge module during this test was $\sim 1.25kW$ which is far from the nominal power of the module of $20kW$. Anyway this kind of test was essential in order to verify the correct behavior of the converter in all its sections. This test was a success and so it was possible to proceed to the nominal power test.

7.2.1.2 High Power Test on the Single H-bridge

In is depicted the setup used during the high power test. Unfortunately in the Digipower s.r.l. labs was not possible to reach the nominal power of the module of $20\,kW$ and so it was tested ad $\sim 15kW$ which was the maximum available power. The conditions of the test were the following:

- Input Dc voltage $\sim 550\,V$
- Output current $\sim 28\,A_{rms}$
- Switching frequency $10\,kHz$

This test was useful for both: test the converter near its nominal conditions, and check the efficiency of the converter. As shown by the power meter in Fig. 7.5, during this test the efficiency was equal to 98.6%. It is expected that when the converter works at its nominal power of $20\,kW$ the efficiency grows up to 99%.

Since also the high power test succeeded, the next step was to test the communication between H-bridge module and the main control board, in order mount the setup for the multilevel tests.

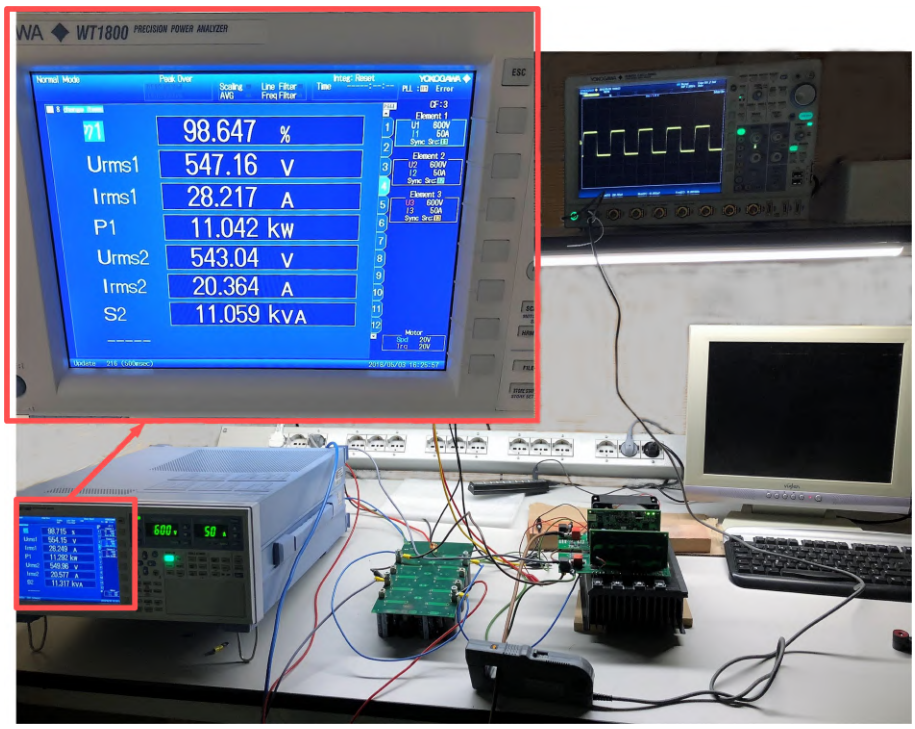


Figure 7.5: High power test of the H-bridge module.

7.3 SPI Communication Test

In this section are presented the results obtained for the SPI communication realized between each H-bridge module and the main control board. In Fig. 7.6 is shown the setup used to carry out the test. In this setup, is not possible to see the main control board since is was still under construction. To replace it, a DE10-Nano board development kit, equipped with an FPGA Altera Cyclone V, was used. The connection between the control board and the DSP on the H-bridge module is made through a Belden multiple cable 9992 with a length of 1 mt. The cable is made by 9 twisted couples of wires, individually shielded and is shown in Fig. 7.7. This choice was related to the high electromagnetic noise that is generated by the converter and which could affect and corrupt the transmitted data. The test has been carried out as follow:

- In the FPGA was allocated a soft core Nios II in charge of control the SPI master signals
- Thanks to the signal tap available on the FPGA all the input and output SPI were monitored as shown in Fig. 7.9.
- The H-bridge module receives from the FPGA the modulation pulses and sends the voltage and current measurement data to the FPGA through the SPI channels.

- The oscilloscope was used to monitor the exchanged data between the FPGA board and the H-bridge module

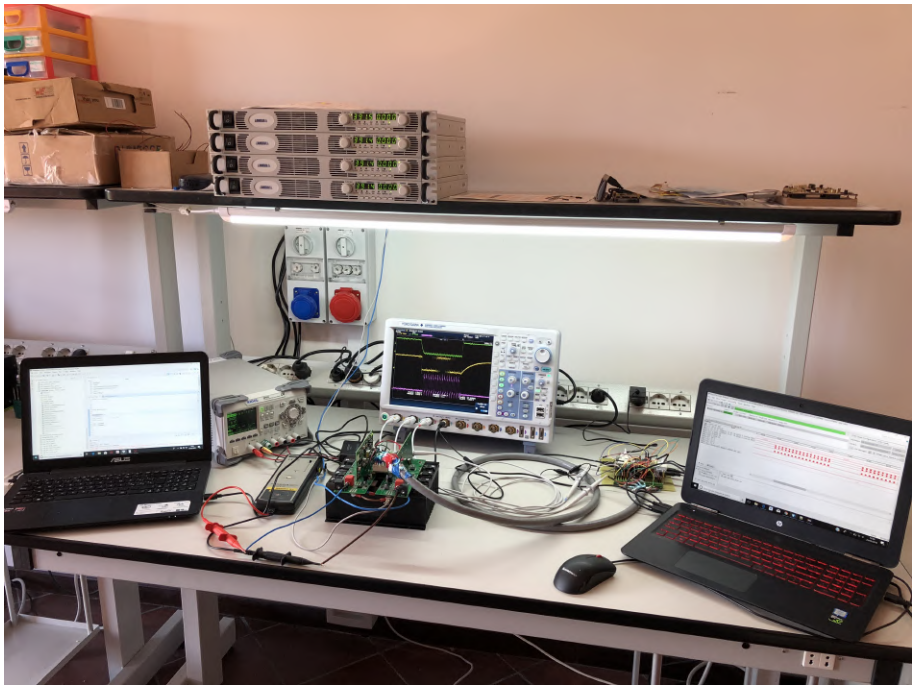


Figure 7.6: Setup for the SPI Connection test.

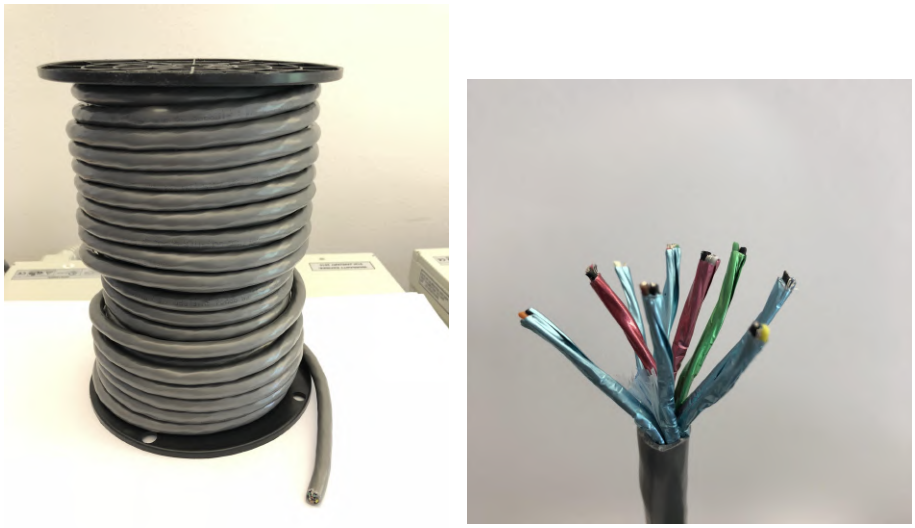
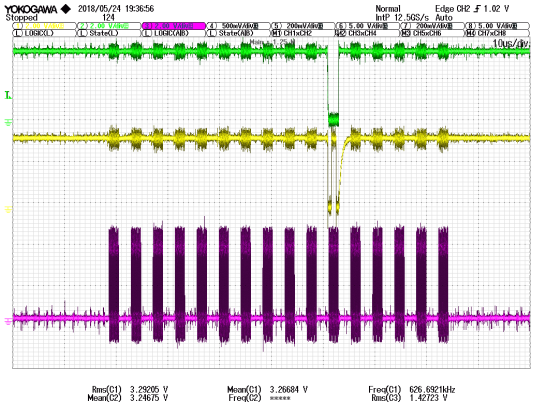


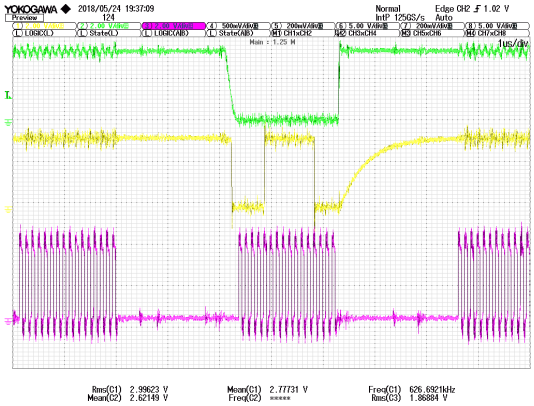
Figure 7.7: Cable Belden 9992.

The obtained results are shown in 7.8a. The FPGA (SPI master) starts the SPI communication consecutively with 16 slaves (one for each H-bridge of a single

phase). During this test only one H-bridge module was connected and so only one SPI channel (the 11th) was transmitting data.



(a) SPI Communication between the FPGA (master) and the H-bridge module (slave). Signals description: CS in green, MISO in yellow and CLK in purple.



(b) Zoom on the SPI Communication between the FPGA (master) and the H-bridge module (slave). Signals description: CS in green, MISO in yellow and CLK in purple.

Figure 7.8: SPI communication signals

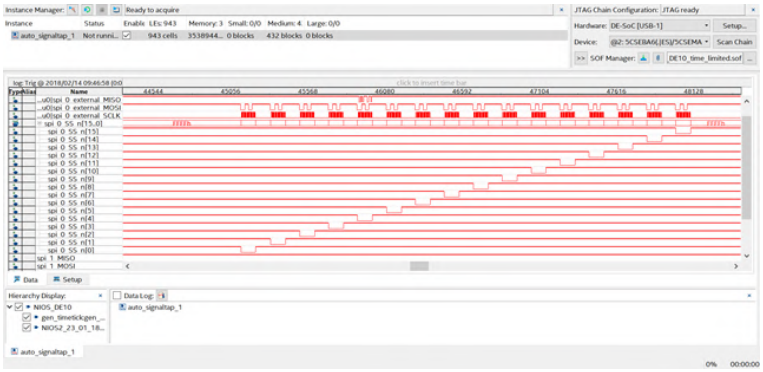


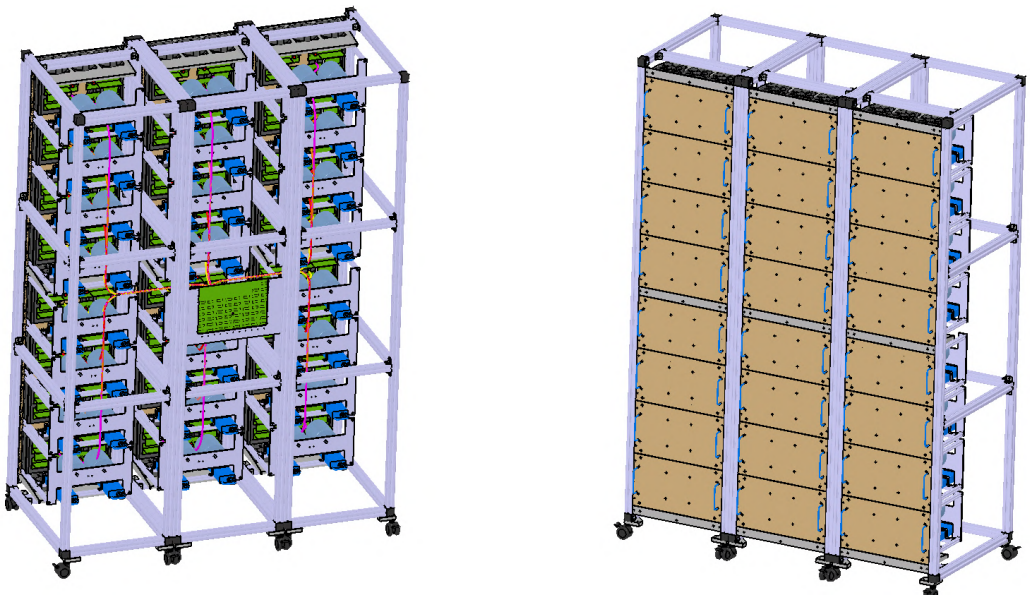
Figure 7.9: Signal tap of the FPGA board.

The obtained results suggests that the adopted configuration works well for our purpose. In particular the selected cable shown a high immunity to the generated electromagnetic noise. The previous tests, done with other kind of cables (such as an Ethernet cable), failed. They shown a corrupted data and a deformed clock signal.

7.4 Multilevel Converter Configuration

After that each H-bridge module was tested as shown in previous sections, the final structure of the 33 level converter was assembled. As it is possible to see in

the figures below, the system has been organized in 3 racks, one for each phase 7.10b 7.10aFig. 7.11. Each rack can accommodate up to 16 H-bridge modules, housed in couples inside tailored drawers 7.12b 7.12a. The main control board was mounted on the back of the central rack, in order to minimize the cables length.



(a) **(b)**

Figure 7.10: Project of the racks for the multilevel converter: (a) back view and (b) front view.

The multilevel converter prototype is still under test but some results have already been obtained. The multilevel prototype has been used in order to validate several modulation techniques, developed during my PhD activities and previously described in chapter 5. A photo gallery of the final prototype is proposed below.

7.5 Multilevel Converter Tests

The first multilevel tests were performed in the DigiPower labs. Because of some equipment limits, they were performed in "low" power conditions. In the results shown in Fig. 7.18 and in Fig. 7.19, the input dc voltage of each H-bridge module was $12\,V$ and the output current was $\sim 5\,A_{pp}$. In the case of Fig. 7.18were used 4 H-bridges for each phase, in order to realize a 9-level three-phase system. In was modulated with a multilevel space vector modulation implemented in the FPGA of the main control board chapter 6.In Fig. 7.19 is shown a test performed for a 25 level single phase configuration. 12 H-bridge modules were connected to the main control board which was performing a phase shifted modulation. For both the hardware

configurations, any critical aspects was encountered and the system was able to work without any relevant issues for a several hours.

Once the first tests were completed, the multilevel converter prototype was transported to the ENEA research center of Portici (NA) in order to perform additional tests. Because of the dimensions of the system, it was not possible to move the complete multilevel prototype to the ENEA labs and so a smaller prototype of 13-levels was used.

Among all the performed tests, two were particularly relevant:

1. Power grid synchronization test: it was executed in order to validate the efficiency of the Phase Locked Loop (PLL) algorithm. As previously described in chapter 6, this routine was implemented on the DSP located in the main control board. It receives all the current and voltage information from the power grid and it calculates in "real time" the electrical angle θ of the grid voltage. θ is then transferred by the DSP to the the FPGA device in order to generate the proper modulation signals to maintain the output voltage of the converter synchronized with the power grid. As shown in Fig. 7.20, the steady state for the synchronization with the power grid is reached in less than $60\,ms$ which are less than 3 periods of the grid frequency.
2. Thermal test: in order to grant a high reliability of the system, a thermal test under high stress conditions for the power switches was performed. The single H-bridge module worked at $600\,V$ and $40\,A$ for an hour. During all the time the thermal conditions of the main components were recorded. As it possible to observe in Fig. 7.21, the initial temperature on the case of the IGBT devices was of $40\,°C$ and at the end of the test it was around $100\,°C$. Considering that the module was working with a current bigger that its nominal value of $35\,A$ and that no fan was used during the test, it is possible to affirm that the thermal heat sink was correctly designed in order to grant the proper thermal conditions for the converter.

7.6 Summary

In this chapter all the individual parts of the multilevel converter prototype realized at Digipower Ltd have been shown. The whole process of debug and test has been described and supported with experimental results which confirms the validity of the project.

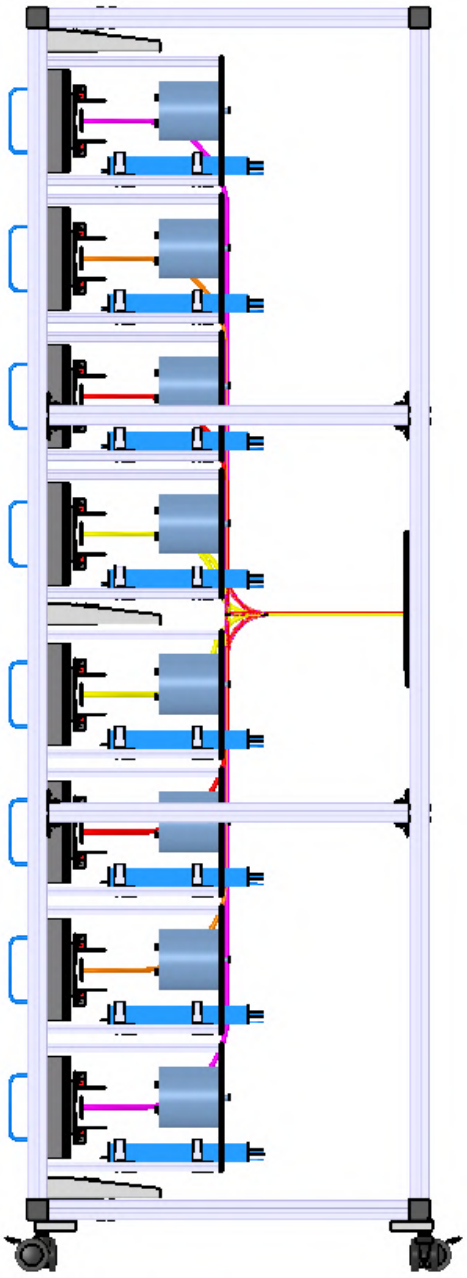
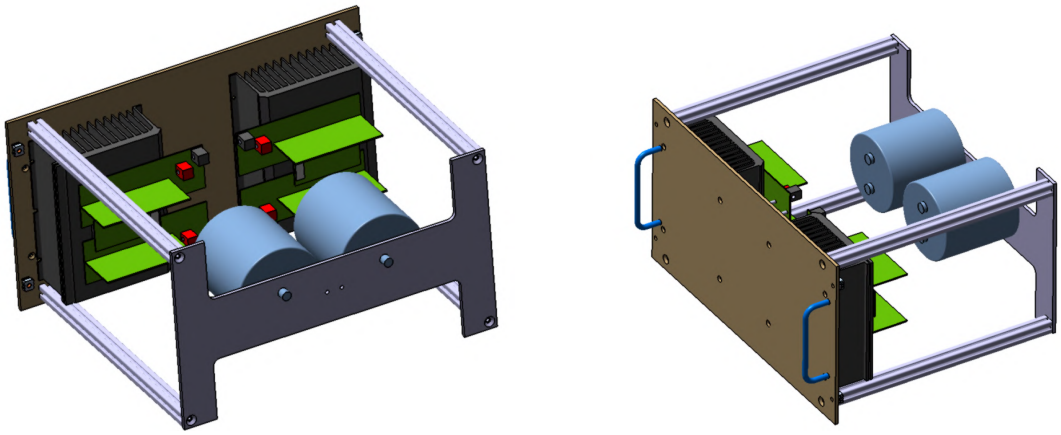


Figure 7.11: Project of the racks for the multilevel converter-side view.



(a) (b)

Figure 7.12: Project of the drawers: (a) back view and (b) side view.

Figure 7.13

Figure 7.14

Figure 7.15

Figure 7.16

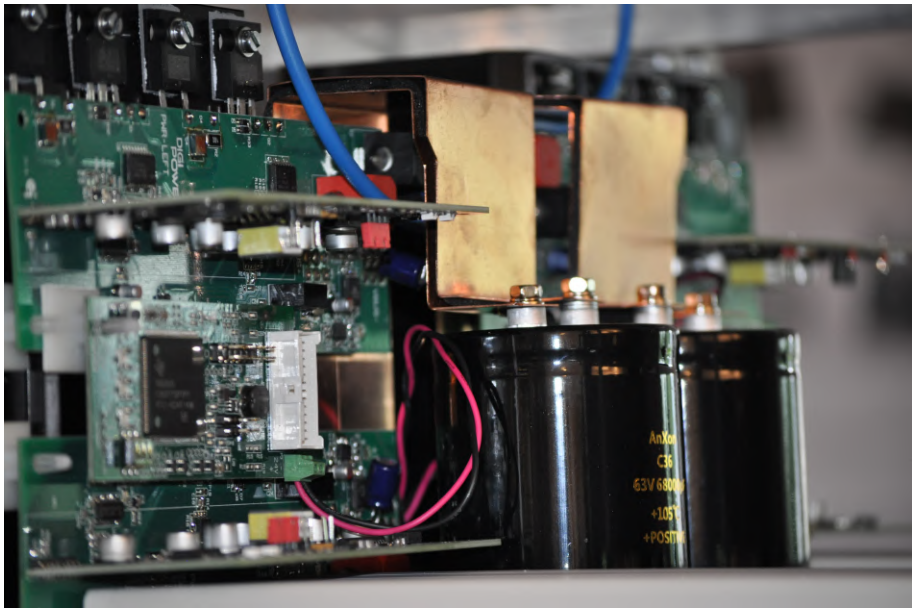


Figure 7.17

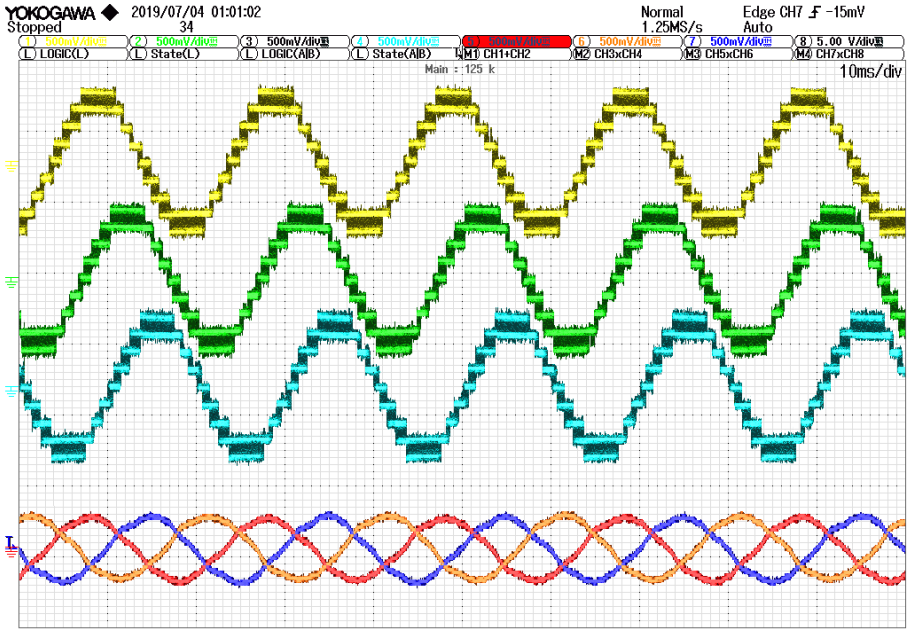


Figure 7.18: Voltage and current waveform for a 9 level three-phase configuration with multilevel space vector modulation.

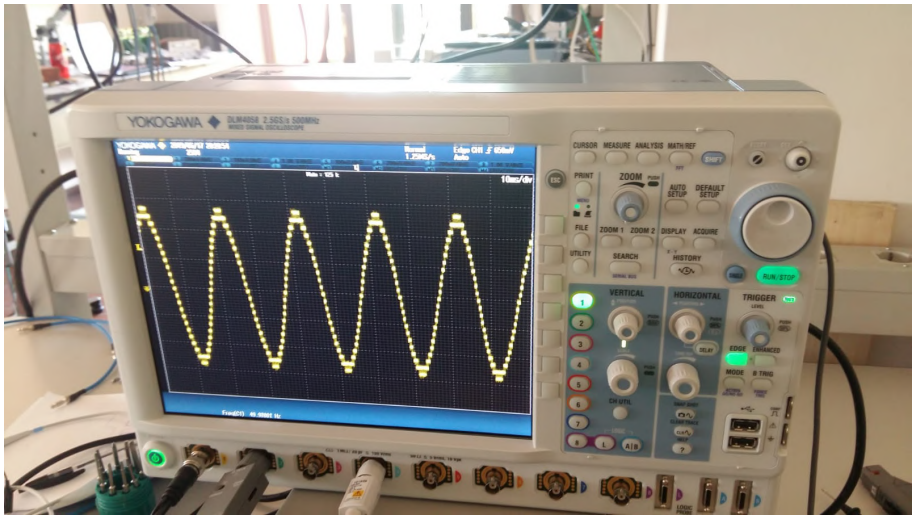


Figure 7.19: Voltage output of a 25 level single-phase configuration with phase shifted modulation technique.

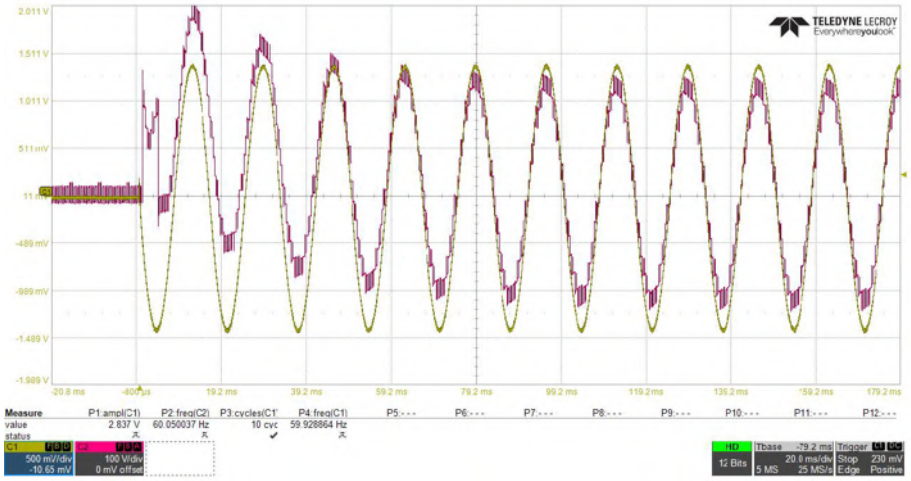


Figure 7.20: PLL synchronization test performed in the ENEA research center of Portici (NA). In yellow the grid voltage, in purple the multilevel output voltage of the converter prototype.

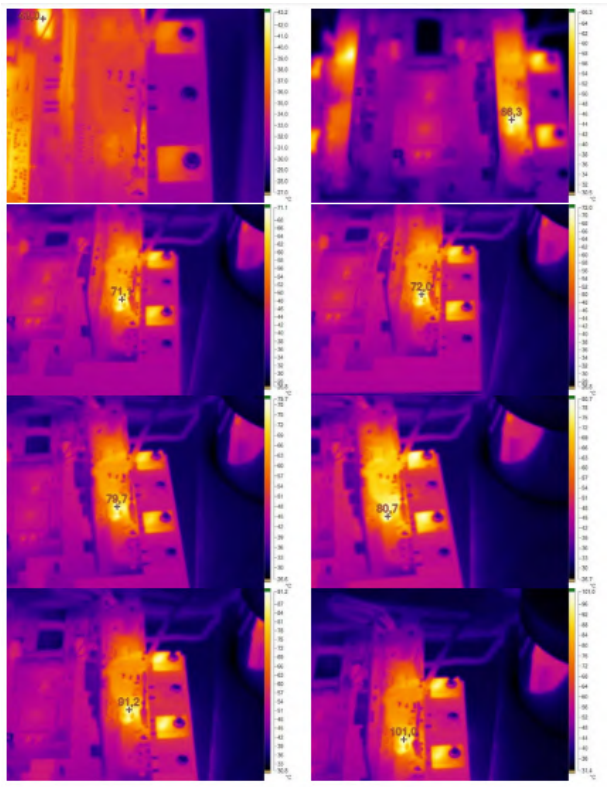


Figure 7.21: Thermal tests performed on the single H.-bridge module in the ENEA research center of Portici (NA).

8 Multilevel Converter Prototype Applications

Among all the multi-level topologies presented in chapter 3, the cascaded type is considered to be the most attractive due to its modularity and fewer component count since it is built by stacking a number of H-bridge (each with its own isolated dc source) to form a stepped output waveform [334, 338, 363]. By increasing the number of H-bridge, more output steps are synthesized, resulting in higher output voltage. In this way, a low THD is achieved as well as ensuring the utilization of low-rated switches which are cheaper and very common.

For all the above mentioned reasons, the realized multilevel CHB prototype lends itself very well to applications where a high voltage level is required and outstanding performances are mandatory. In this section, are presented two applications in which the multilevel converter prototype described in chapter 8has been used: a D-STATCOM application and a motor drive application. Both the proposed implementations are still under development and they need to be improved and refined but the first results shown good performances and they are shown and discussed in deep in the sections below.

8.1 D-STATCOM Application

8.1.1 Overview

Rapid development in power electronics and control offers P-Q improvement using flexible AC transmission system (FACTS) controllers [347]. At the electrical distribution level, the D-STATCOM, which is in the family of FACTS devices, has been frequently used for power factor correction, load balancing, voltage regulation and stabilization. These functions are achieved by means of the reactive power compensation [331, 332, 333]. Traditionally, the low cost, two-level voltage source inverter (VSI) with a series coupling inductor, is used as the main building block of the DSTATCOM [344, 345].

However, the output voltage of the VSI is characterized by high harmonics that require bulky and costly filtering. Furthermore, for high and medium voltage interconnections, it is mandatory to use the line frequency (50 Hz) step-up transformer to match the output voltage of the VSI to the utility grid. This increases the cost,

size, weight and power losses of the overall D-STATCOM. Thus, the multilevel VSI (MVSI) is being exploited to replace the two-level VSI [348, 334, 335].

Since the MVSI is sufficiently capable of providing high voltage, the use of step-up transformer can be avoided [349, 351]. As a result, the weight and cost of the hardware are reduced significantly. For example, with the absence of the transformer, the weight of 3-phase cascaded MVSI, rated at $6.6\,kV/1\,MVA$ can be reduced three to four times compared to its transformer counterpart [349, 341]. In [341], it is reported that the transformer and its ac inductor is about half of a 360 kVA D-STATCOM weight. Additionally, the efficiency of the system can be increased; in a typical D-STATCOM system, approximately 70% of overall power loss per MVA rating is attributed to the transformer [351].

In this section the main aspects of a D-STATCOM application are described and several multilevel solutions are proposed and compared.

8.1.2 D-STATCOM Model

The D-STATCOM is a distribution network compensator device connected in parallel to the grid at the point of common coupling (PCC). A single line diagram of a typical connection of D-STATCOM to the power source is shown in Fig. 8.1. The main building block of the D-STATCOM is the Voltage Source Inverter (VSI). It converts the dc input voltage to a balanced 3-phase voltage with controllable magnitude and phase angle [336]. The VSI is connected to the line through a series coupling inductor LAC. The voltage difference across LAC creates the reactive power (Q) exchange between the D-STATCOM and the grid system. In the inductive mode operation, the D-STATCOM absorbs Q by making $V_C < V_{PCC}$. During the capacitive mode, where $V_C > V_{PCC}$, the flow of Q is reversed.

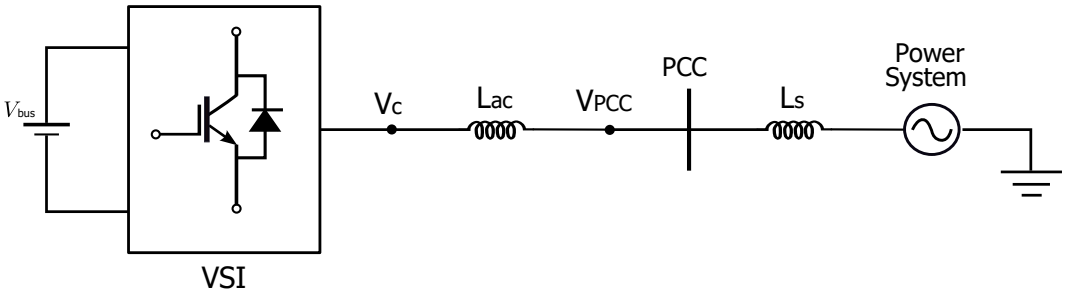


Figure 8.1: Single line diagram of D-STATCOM.

The exchange of active power P and Q between the D-STATCOM and the line are governed by:

$$P = \left(\frac{V_{PCC}V_c}{X_{AC}}\right) sin\delta \tag{8.1}$$

$$Q = \frac{V_{PCC}}{X_{AC}}(V_{PCC} - V_C) \tag{8.2}$$

Since P is always positive, the P exchange in steady-state is achieved by a small shift of δ. The active power compensates for the dc voltage decrease across the capacitors (V_{DC}) due to the losses. Furthermore, from 8.2, it is expected that Q exchange can be obtained by properly controlling the output voltage of the VSI (V_C). In a close loop system, the variation of V_C is achieved by adjusting the value of modulation index M_I. Fig. 8.2 illustrates the phasor diagram of active and reactive power exchange between the D-STATCOM and the grid in the 4-quadrants of P-Q-plane [337]. It reveals the two control laws of D-STATCOM:

1. For reactive power exchange, the output voltage (V_C) is controlled to allow the compensation in capacitive and inductive modes as illustrated in quadrants I & II and quadrants III & IV accordingly.:
2. For active power exchange, the phase angle between STATCOM's output voltage and the voltage at PCC is adjusted to allow the exchange of active power in capacitive and inductive modes as shown in I & IV and II & III respectively.

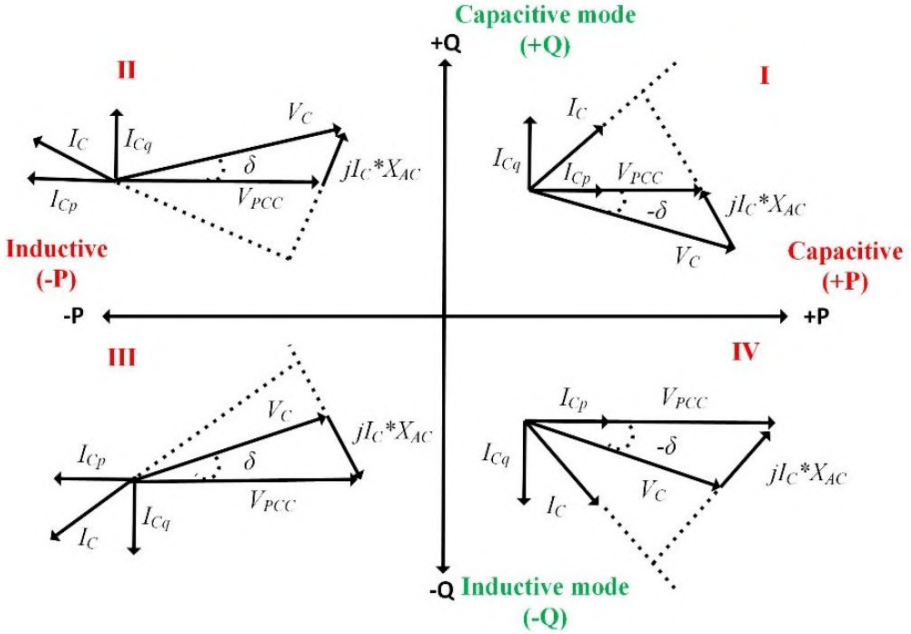


Figure 8.2: Phasor diagram for power exchange in D-STATCOM.

8.1.3 Multi-level VSI for D-STATCOM

Since the 1980s, STATCOMs have been increasingly used at a higher voltage level, i.e. in transmission [338, 339, 340], high voltage distribution [341, 342, 343] and energy utilization. Traditionally, the two levels voltage source inverter (VSI) (Fig. 8.3) with a series transformer form the main building block of the D-STATCOM [344, 345, 342]. The main objective of using a VSI is to utilize the input dc voltage to synthesize ac output waveform [346]. By proper modulation of VSI output voltage, the output current changes simultaneously; thus, the dynamic exchange of active and reactive power between the STATCOM and the utility grid is attained [347]. The popularity of VSI is due to its simplicity and low cost. However, its output voltage is characterized by high harmonics contents, which require bulky and costly filtering. Furthermore, it is mandatory to use step-up transformers to allow the connection of the VSI to high and medium voltage level. This increases the cost, size, weight and losses of the overall system [348]. Alternatively, a zigzag transformer is utilized to suppress the low order harmonic components and avoid the use of bulky filters. However, such transformers are usually bulky and expensive; they occupy more space and produce high losses.

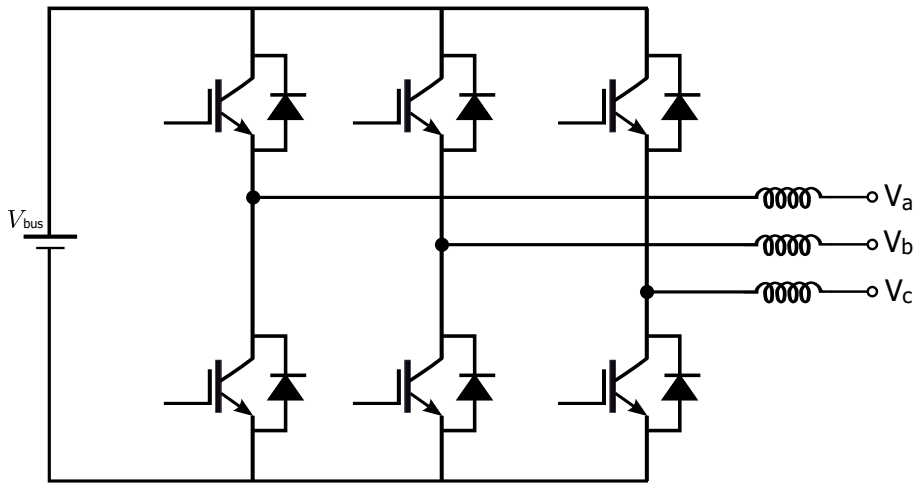


Figure 8.3: Three-phase two-level VSI.

More recently, the multilevel VSI (MVSI), [348], are being exploited to replace the conventional VSI for D-STATCOM applications. Since the MVSI is capable of providing sufficiently high voltage, the bulky, lossy and costly step-up transformer can be avoided [349, 350, 351]. For instance, with the absence of the line frequency (50 Hz) transformer, the weight of a 3-phase cascaded MVSI at 6.6 kV/1 MVA rating is reduced by three to four times [349, 341]. Furthermore, [349, 341], reported that for a 360 kVA D-STATCOM, weight is about half of the overall system size, while [351] noted that approximately 70% of the total loss per MVA rating is due to the transformers.

In addition, implementation of MVSI in D-STATCOM [352, 353, 354] allows the

utilization of much lower rated semiconductor switches for high voltage generation [355]. For example, a medium voltage (11 kV) converter can be constructed using a 23 level MVSI, in which each level contributes a voltage of 1 kV. In this case, an IGBT switch rated at 1.5-2 kV is adequate to realize the converter. In addition, the stepped output nature of MVSI not only reduces the stress on the switching devices, it also improves the frequency spectra profile resulting in lower harmonics distortion [356, 357].

In theory, the number of level for MVSI is infinite, but for practical purposes, it is limited by the complexity of the circuit. The minimum number of level to be considered as a MVSI is three, i.e. –V, 0 and +V. Over the years, various MVSI topologies have been proposed for DSTATCOM: among others, the diode clamped [358, 359], flying capacitor [358, 360] and cascaded inverters [358, 361] are the most popular and they have been described in deep in chapter 3.

8.1.4 Comparison Between MVSI Topologies for D-STATCOM

Tab. 8.1summarizes the number of components required to produce N phase voltage levels of MVSI [362]. Even though the number of the main components are the same in the three configurations, the overall number of components is different. For diode-clamped MVSI, $(N-1)*(N-2)$ clamping diodes per phase are needed to produce N voltage level. For STATCOM, this increases the cost and causes packaging problems. In addition, special control is needed to balance the voltages across the capacitors. Thus, practical applications of diode-clamped MVSI topology are limited to five levels. For flying-capacitor MVSI, a number of $(N-1)*(N-2)/2$ flying capacitors is needed per phase to construct N per phase levels. Consequently, high switching frequency and complex control are necessary to balance the voltages across the capacitor. For high voltage utility applications, a large number of capacitors is needed.

Table 8.1: Comparison of component number requirement per phase voltage level among MVSI topologies [362].

MVSI Topology/ Component	Diode-clamp	Flying capacitors	Cascaded Type
Switches	$2*(N-1)$	$2*(N-1)$	$2*(N-1)$
Main diodes	$2*(N-1)$	$2*(N-1)$	$2*(N-1)$
Clamping diodes	$(N-1)*(N-2)$	0	0
DC-bus capacitor	$(N-1)$	$(N-1)$	$(N-1)/2$
Balancing capacitor	0	$(N-1)*(N-2)/2$	0
Total Number of component	$N^2+(2*N)-3$	$(N^2+(8*N)-8)/2$	$(9/2)*(N-1)$

Unlike the diode-clamped and flying-capacitor topologies, the cascaded H-bridge MVSI requires the least number of components and does not need clamping diodes or balancing capacitors [354]. Fig. 8.4 presents the number of total component required

by the MVSI as a function of phase voltage levels (N). For high MVSI (e.g. 25 levels), cascaded H-bridge MVSI requires fewer components comparing to the diode-clamped MVSI and flying-capacitor MVSI. Thus, the reliability of this topology is higher.

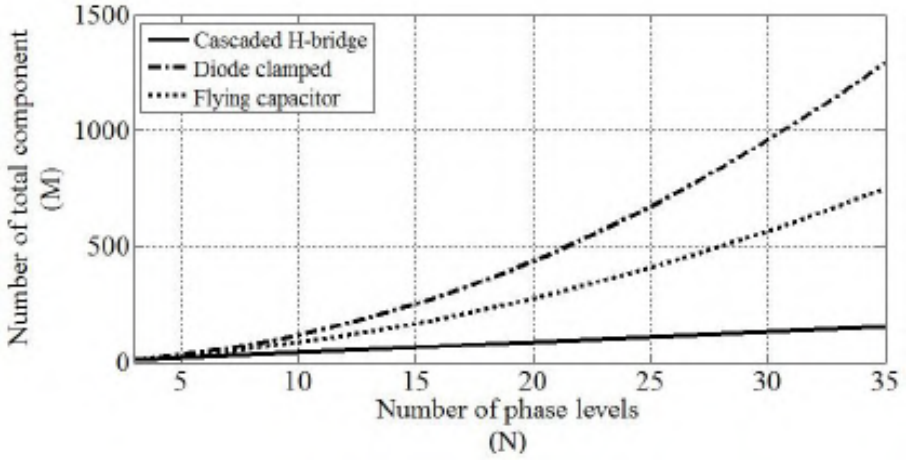


Figure 8.4: Total number of components (M) as a function of phase voltage level (N) in MVSI [362].

Another fundamental advantage of the cascaded H-bridge MVSI circuit is its layout flexibility. Its modular structure allows easier maintenance and provides a very convenient way to add redundancy into the system [363]. Thus, the number of output voltage levels can be easily adjusted by properly selecting the number of H-bridge units to be used in according to the required voltage magnitude. Due to the modularity and the low components number, packaging is easy compared to other tow topologies. Furthermore, the number of dc capacitors utilized for cascaded H-bridge MVSI based STATCOM can be considered an advantage. By integrating the energy storage systems (e.g. fuel cell or ultra-capacitors) with each H-bridge unit, D-STATCOM can provide both active and reactive power compensation.

In conclusion, among the three MVSI structures, the cascaded is the most viable for D-STATCOM due to its modularity, simplicity and fewer component count [351, 338, 363], hence it has been considered for the realization of the experimental prototype presented in this thesis.

8.1.5 Control Strategies for D-STATCOM

The D-STATCOM is mainly used for reactive power compensation. This is achieved by controlling its output to produce a synchronous voltage waveform that forces the reactive power exchange with the utility grid. The governing equations

of the active and reactive power by D-STATCOM to the grid are given by:

$$P = \frac{|V_{PCC}| * |V_c|}{X_{AC}} sin\alpha \tag{8.3}$$

$$Q = -\frac{|V_{PCC}|^2}{X_{AC}} + \frac{(|V_c| * |V_{PCC}|)}{X_{AC}} cos\alpha \tag{8.4}$$

To simplify the analysis [[364]], let $V_{PCC} = 1$, thus, the following equations are obtained:

$$P = \frac{|V_c|}{X_{AC}} sin\alpha \tag{8.5}$$

$$Q = -\frac{1}{X_{AC}} + \frac{|V_c|}{X_{AC}} cos\alpha \tag{8.6}$$

Based on these equations, the sensitivity analysis test is performed to examine the effectiveness of voltage magnitude V_C and phase angle α in controlling the active and reactive power [364]. By taking the derivatives of the equations, the following sets of equations are derived:

$$\frac{\partial P}{\partial |V_c|} = \frac{1}{X_{AC}} sin\alpha \tag{8.7}$$

$$\frac{\partial P}{\partial \alpha} = \frac{|V_c|}{X_{AC}} cos\alpha \tag{8.8}$$

$$\frac{\partial Q}{\partial |V_c|} = \frac{1}{X_{AC}} cos\alpha \tag{8.9}$$

$$\frac{\partial Q}{\partial \alpha} = -\frac{|V_c|}{X_{AC}} sin\alpha \tag{8.10}$$

Note that V_c is close to unity and α is approximately zero in normal operation [365]. So, $cos\alpha \approx$ 1ans $sin\alpha \approx 0$. As a result, $|\frac{\partial P}{\partial V_c}| << |\frac{\partial P}{\partial \alpha}|$ and $|\frac{\partial Q}{\partial V_c}| >> |\frac{\partial P}{\partial \alpha}|$. Thus, to control the reactive power, it is concluded that varying the voltage magnitude is more viable than the phase angle. On the other hand, the phase angle is more effective when active power control is concerned.

Normally, D-STATCOM without storage devices is used only for reactive power compensation. Thus, for a proper exchange of reactive power with the electrical grid, an efficient control of the output voltage amplitude is crucial. For any type of inverter, the output voltage is given by:

$$V_c = M_I * V_{DC} \tag{8.11}$$

Where M_I is a modulation index that relates the input dc voltage to the amplitude of output voltage of the inverter. Based on 8.11, the output voltage of D-STATCOM can be change by controlling the dc input voltage (V_{DC}) or the M_I value. Therefore, two control schemes (i.e. direct and indirect) can be used.

For high power applications, the VSI of the D-STATCOM should operate under low switching frequency to reduce the switching losses. In addition, it should exchange a high-quality current (i.e. THD less than 5%) with the utility grid. To meet these requirements, the indirect control strategy [366, 365, 367] is used in which the output voltage of the VSI is indirectly controlled by changing the magnitude of the dc capacitor voltage. In this scheme, the phase angle of the VSI output voltage (δ) is the control variable, while M_I is held constant at maximum value. Thus, the output voltage distortion (reflected by the THD value) is kept to a minimum due to the exploitation of maximum value of M_I. In addition, line-frequency inverter can be easily utilized; hence, low switching frequency operation is possible. However, a rapid adjustment of reactive power is unachievable since the output voltage control using δ is restricted by the time constants of charging and discharging of the VSI capacitor.

This limitation is addressed by the direct control approach [350, 365, 338]. In this scheme, the capacitor voltages are fixed, while the reactive power control is achieved by varying the amplitude of the output voltage using M_I. The latter is directly influenced by the PWM switching of the VSI. Despite the improved performance, two problems exist with the direct control, namely 1) the THD changes with the variation of M_I and, at low M_I, poor harmonics profile of the output voltage can result, and 2) high losses due to the high switching frequency of the PWM scheme. To overcome these limitations, a PWM with low switching frequency and good harmonics characteristics should be utilized. Fig. 8.5 shows direct control strategy implemented on the FPGA main control board of the experimental prototype presented in chapter 7. accordingly.

8.1.6 Simulation Results

The proposed D-STATCOM has been used to regulate the voltage at the PCC by exchanging reactive power with the grid. The main objective of the control is to maintain the voltage at the PCC at a nominal value. To test the viability of the proposed D-STATCOM in the capacitive and inductive modes, the voltage at the

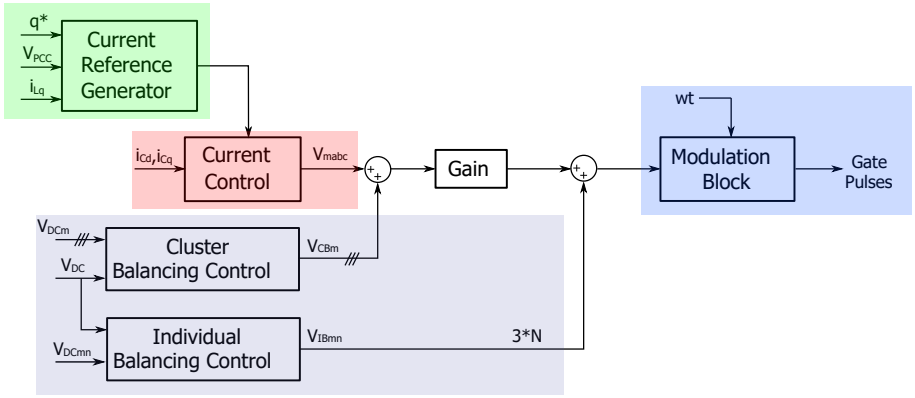


Figure 8.5: STATCOM direct control scheme.

PCC has been increased by 3% at $0.2\,s$ and decreased by 2% at$0.4\,s$ for$0.1\,s$. This has been done using a programmable ac power supply block in Simulink/Matlab[2]. As a response to the step change, the V_{PCC} increases/decreases by $0.33/0.22\,kV$.

The simulation has been performed with the connection of D-STATCOM at PCC. As depicted in Fig. 8.6 and in Fig. 8.7, the V_{PCC} is effectively recovered to the nominal targeted value ($1\,p.u.$). For sag problem, the controller reacts by increasing MI to $8.00\,p.u.$ Therefore, the required reactive power is injected to compensate the dropped voltage. Whereas, for swell, the M_I is set to $5.45\,p.u.$ The D-STATCOM absorbs the required reactive power. In this way, the voltage is restored to its nominal value.

8.2 Motor Drive Application

8.2.1 Overview

Presently, automobile industry is facing challenges to reduce vehicle emissions/km and to eliminate the dependency on dwindling fossil fuels. This has become the pivotal reason for the orientation of automobile technology for further development of hybrid electric vehicles (HEV) and full electric vehicle (EV). This emerging technology is not only clean but also offers advantages like fast driving response, smooth operation, high efficiency and independent control of each wheel due to the in-wheel technology as compared to the traditional internal combustion engine (ICE). One of the main reasons, that prevents EV from being extensively used is its shorter range compared to ICE. A study was carried out in [368] for the improvement of electric motors and EV range extension.

Large electric vehicles have huge power demand which can be fulfilled

1. by implementing traditional converter topologies with conventional semiconductor technology,

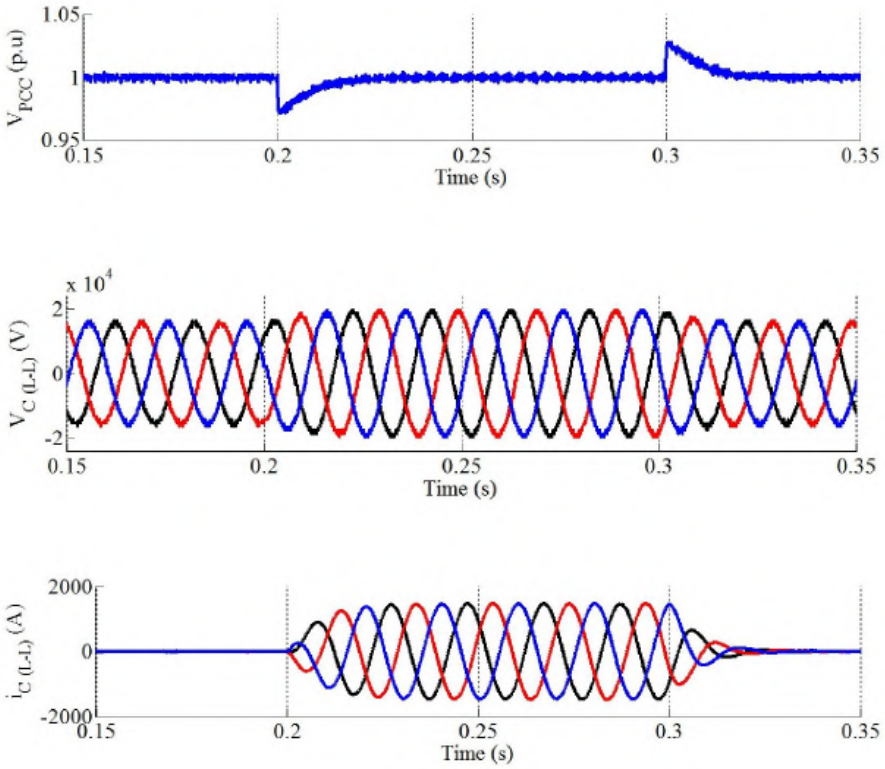


Figure 8.6: Performance of the proposed D-STATCOM for sag mitigation.

2. by developing new multilevel topologies with the use of easily available lower voltage rating semiconductor devices, including the innovative wide band gap devices.

Traditional 2-level inverter (TLI) suffers from high dv/dt, common mode voltage across motor winding and higher blocking voltage across each device. Also, obtaining higher voltages and currents with former method is a challenge for semiconductor industry [369, 370]. Multilevel inverter (MLI) eliminates the disadvantages associated with TLI, and has attractive features such as sinusoidal output voltage profile, lower dv/dt which accounts for less stress on switches, higher power handling capacity, available redundancy for transferring power to less used module, reduced switching losses, lower total harmonic distortion (THD), less common mode voltage which decreases stress in the motor bearings [371], and increases longevity of the motor.

Among multilevel topologies, Cascaded H-Bridge (CHB) topology sec. 3.4 appears to be the most appropriate for EV application as on-vehicle low voltage battery modules can be arranged in such a way that each H-bridge has its own dc source. In addition, CHB guarantees reliable operation of EV. Because, if any module suffers failure, the vehicle can be transported to desired location with reduced speed and faulty module can be easily repaired and replaced due to the modularity in structure of CHB MLI. Also, charging of battery modules could be faster due to simultaneous

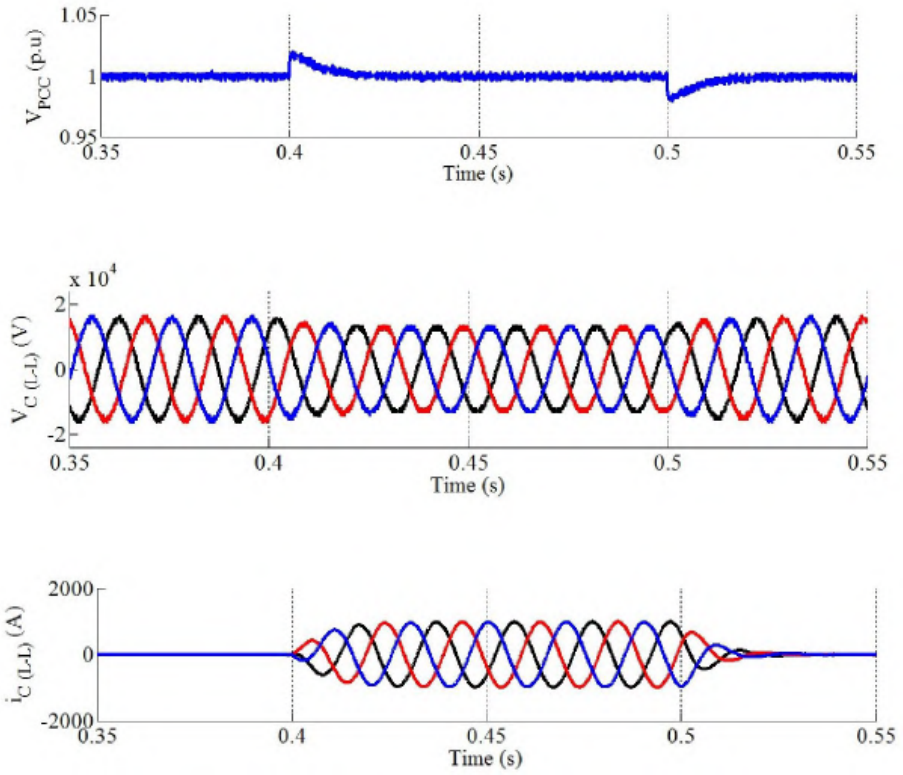


Figure 8.7: 4.12: Performance of the proposed D-STATCOM for swell mitigation.

charging of each module resulting in reduced wait time of consumer. In contrast, charging of differently arranged battery modules requires greater attention when compared to 2-level inverters which consists of only one battery pack.

In [372] we conduced a comparative study of electric power train between TLI and MLI (different levels like 2, 5, 7, and 9). The research presents two fold solution for developing a prototype of EV. Firstly, it discusses the trade-offs to decide the best suitable level and secondly, validates the same with the simulation studies presented. Torque ripple, THD and switching losses are evaluated using different inverter levels for electric power train. This investigation includes complex trade-offs among performance, safety, reliability, and feasibility and cost for EV using different level of MLI. The optimal choice of the voltage levels is made based on the simulations to point out the features that can improve overall efficiency, reduced charging time of the energy storage, better THD and reliability.

8.3 Control of PMSM for EV

To compare different inverter topologies, the conventional FOC has been adopted in this work and it is presented as shown in Fig. 8.8. The PMSM is modeled in synchronous rotating reference frame. The d and q-axis stator voltages (V_{sd} and

V_{sq}) are,

$$V_{sd} = L_d I_{sd} + R_d I_{sd} - \omega_r L_q I_{sq} \tag{8.12}$$

$$V_{sq} = L_q I_{sq} + R_q I_{sq} + \omega_r L_d I_{sd} + \omega_r \lambda_{af} \tag{8.13}$$

The electromagnetic torque is given by,

$$T_e = \frac{3}{2}\frac{N_p}{2}\left[\lambda_{af} + (L_d - L_q)\, I_{sd}\right] I_{sq} \tag{8.14}$$

The mechanical equation of motor is,

$$\frac{d\omega_{rm}}{dt} = \left(\frac{1}{J}\right)\left(T_e - T_l - T_d - B\omega_{rm}\right) \tag{8.15}$$

Where, V_{sd} and V_{sq}, I_{sd} and I_{sq}, L_d and L_q, R_d and R_q are voltages, currents, stator self inductances, stator resistance of d and q axes respectively. N_p is number of poles of machine. T_l, T_d, B, J are load torque, dry friction, viscous friction coefficient, moment of inertia of the machine respectively. ω_{rm} is mechanical speed of motor. The electrical angular speed of motor can be written as, $\omega_r = \frac{N_p}{2}\omega_{rm}$. The position of rotor (θ) is obtained by integrating electrical speed, i.e. $\theta = \int \omega_r dt$.

For surface mounted PMSM $L_d = L_q$. Hence, the equation 8.14 is simplified as,

$$T_e = \frac{3}{2}\frac{N_p}{2}\lambda_{af} I_{sq} \tag{8.16}$$

This ensures maximum torque of motor. In FOC, I_{sd} component of stator current is made to zero, as flux is generated by PM which increases the efficiency by obtaining maximum torque per ampere of drive. FOC decouples the flux and torque components of stator currents, thus gives independent control of flux and torque, which gives better dynamics.

It uses classical PI controllers and has three closed loops: I_{sd}, I_{sq} and speed control loop which controls flux, torque and speed of drive respectively. Current controller of FOC uses feed forward decoupling term to get better dynamic performance by eliminating the interdependence between torque and flux component. FOC features transformation of non linear system into linear system, fast dynamic response, good transient and steady state performance, high torque and low current at starting, high speed range because of flux weakening, and high efficiency [374, 375].

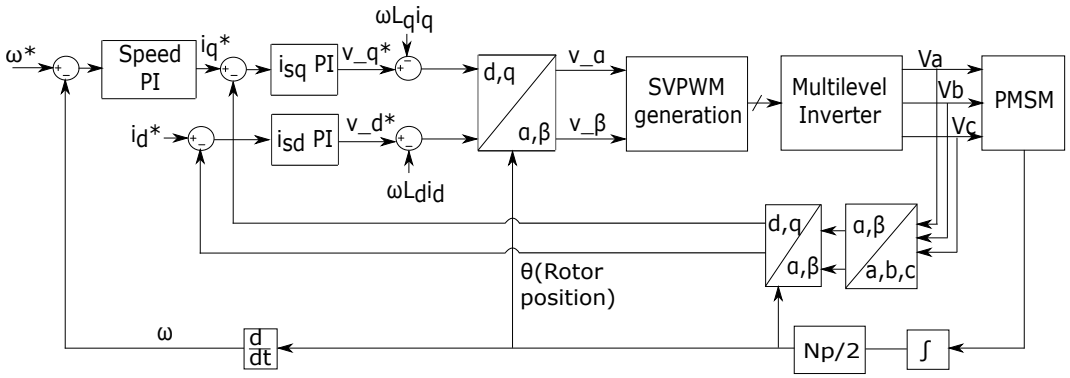


Figure 8.8: Control structure for FOC of PMSM.

8.4 Cascaded H-bridge Multilevel Inverters

The scope of this paper is to evaluate the best number of level for the power train of electric vehicle. In depth analysis based on complexity, cost, and availability of dc sources, etc., 5, 7, 9-levels have been selected as the most appropriate for this study and a comparison with conventional TLI is consequently provided. Fig. 8.9(a) shows traditional TLI, which is used in existing automotive application like most popular models Tesla S, and Nissan Leaf as it is easy to implement and cost effective. Each CHB in itself is a 3-level structure, thus desired multi levels can be obtained by cascading number of same CHB modules. Fig. 8.9(b) shows generalized circuit diagram of CHB multilevel inverter. The number of H-bridges and isolated dc sources required per phase are, $n = \frac{1}{2}(m-1)$, where, m is a odd number and represents the number of desired level.

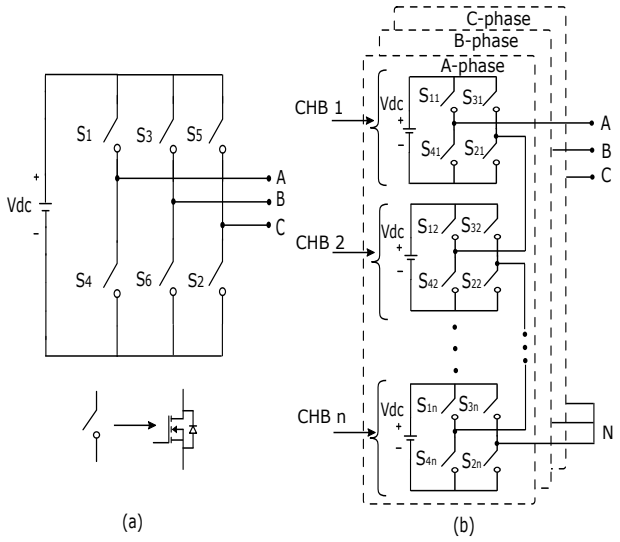


Figure 8.9: Circuit diagram of (a) 2-level inverter (b) generalized multilevel inverter.

Table 8.2: Pole voltage redundancies for 5-level inverter.

Level	Pole voltage	Switching states							
		S_{11}	S_{21}	S_{31}	S_{41}	S_{12}	S_{22}	S_{32}	S_{42}
4	2Vdc	1	1	0	0	1	1	0	0
3	Vdc	1	1	0	0	1	0	1	0
		1	1	0	0	0	1	0	1
		1	0	1	0	1	1	0	0
		0	1	0	1	1	1	0	0
2	0	1	0	1	0	1	0	1	0
		0	1	0	1	0	1	0	1
		1	1	0	0	0	0	1	1
		0	0	1	1	1	1	0	0
		1	0	1	0	0	1	0	1
		0	1	0	1	1	0	1	0
1	-Vdc	0	0	1	1	1	0	1	0
		0	0	1	1	0	1	0	1
		1	0	1	0	0	0	1	1
		0	1	0	1	0	0	1	1
0	-2Vdc	0	0	1	1	0	0	1	1

The number of voltage levels in line voltage waveform becomes, $L = 4n + 1$ for symmetrical CHB topology. The switches S_{1n}, $S_{4n}$and S_{3n}, S_{2n} of each H-bridge

operates in complimentary manner to avoid the short circuiting of dc sources. For example, 5-level inverter can be obtained by cascading two H-bridges CHB 1 and CHB 2 of Fig. 8.9(b) per phase. It gives five pole voltage levels 2Vdc, Vdc, 0, -Vdc and -2Vdc which are obtained using switching sequence as shown in Tab. 8.2. Similarly, levels for 7 and 9 can also be realized. Hence, as the number of levels increases the H-bridges per phase allows to use lower VA rated devices.

8.5 Simulation Results

Aforementioned power train with different multilevel inverters is simulated using FOC with level shifted SVPWM technique using motor parameters of Tab. 8.3.

Table 8.3: PMSM parameters.

PMSM parameters	
Stator self inductances, L_d, L_q	0.85 mH
Stator resistances, R_d, R_q	0.15 Ω
Number of poles, N_p	6
Nominal speed, ω	6000 RPM
Permanent magnet flux, λ_{af}	0.0557 Wb
EMF constant, K_e	17.5 $V/1000$
Torque constant, K_t	0.29 N·m/A
Rotor inertia, J	2.9 Kg $\cdot$ m^2

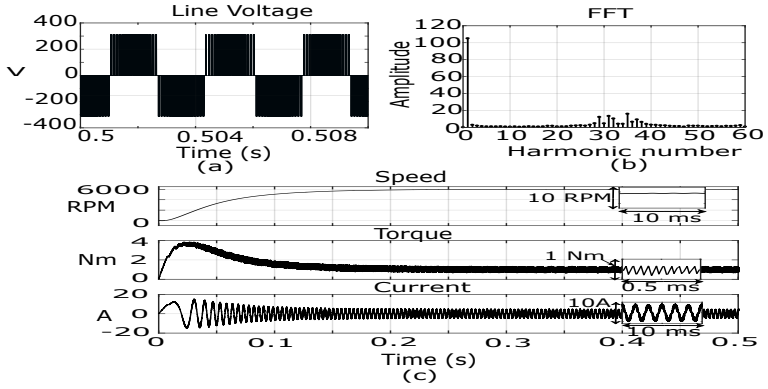


Figure 8.10: Simulation result of 2-level inverter with PMSM drive: (a) line to line voltage (b) harmonic spectrum (c) speed, torque and current of drive at nominal value.

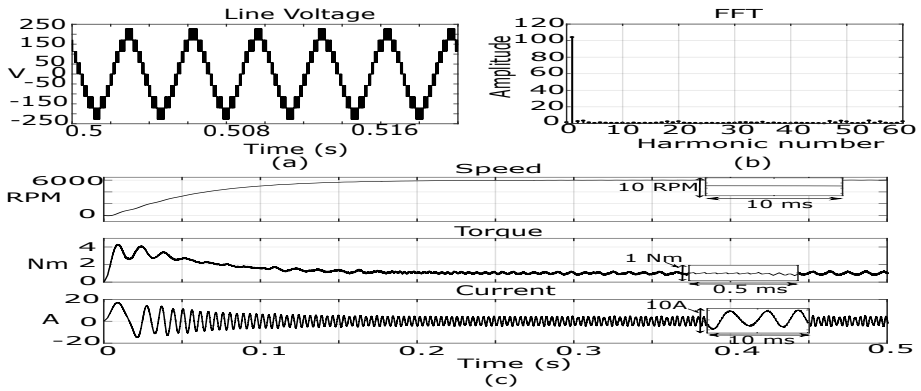


Figure 8.11: Simulation result of 5-level inverter with PMSM drive: (a) line to line voltage (b) harmonic spectrum (c) speed, torque and current of drive at nominal value.

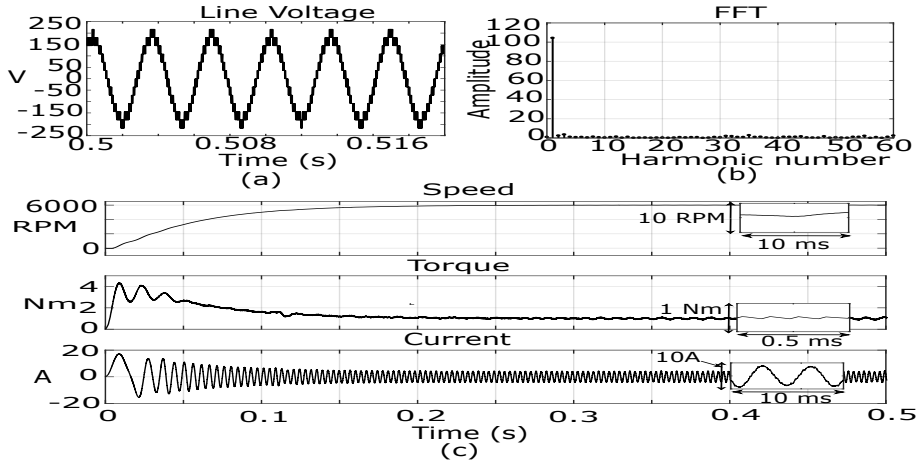


Figure 8.12: Simulation result of 7-level inverter with PMSM drive: (a) line to line voltage (b) harmonic spectrum (c) speed, torque and current of drive at nominal value.

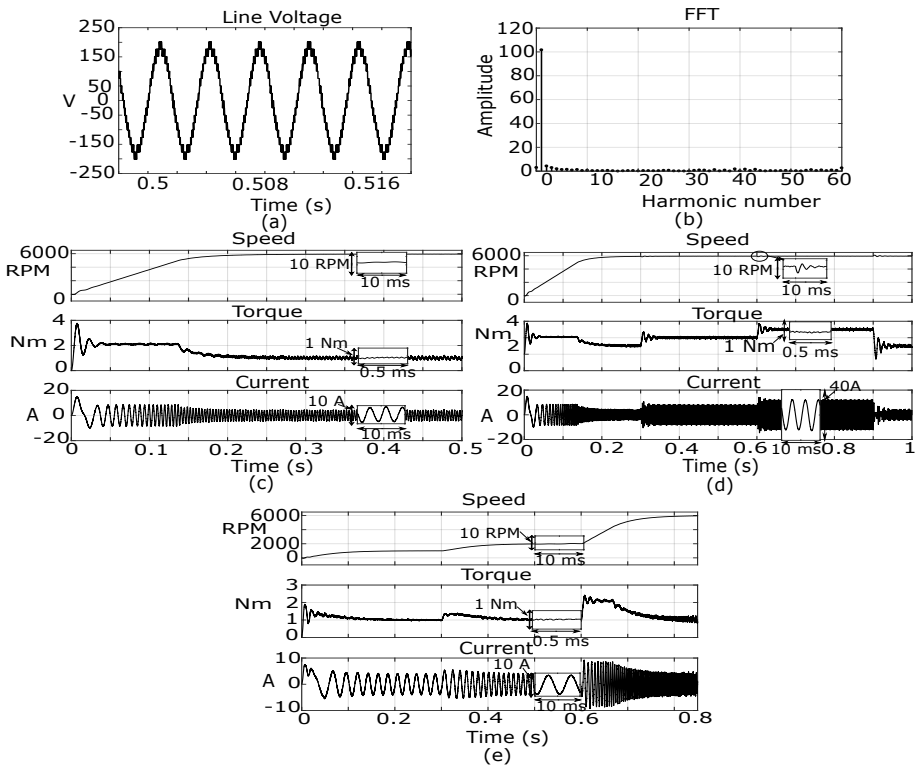


Figure 8.13: Simulation result of 9-level inverter with PMSM drive: (a) Line to line voltage (b) harmonic spectrum (c) speed, torque and current of drive at nominal value (d) speed, torque and current of drive with varying torque (e) speed, torque and current of drive with varying speed.

The Fig. 8.10(a), Fig. 8.11(a), Fig. 8.12(a) and Fig. 8.13(a) show the line to line voltage of motor. It is evident from the result that as the number of level of inverter is increased, the output voltage of inverter shifts towards sinusoidal giving better performance as seen in respective harmonic spectrum. The Fig. 8.10(b), Fig. 8.11(b), Fig. 8.12(b) and Fig. 8.13(b) give FFT of the machine phase voltage, whose fundamental is at 300 Hz. The Fig. 8.10(c), Fig. 8.11(c), Fig. 8.12(c) and Fig. 8.13(c) show the speed, torque and current of the drive. The nominal speed of drive is 6000 RPM, and the load torque value is kept at 1 Nm, as seen in results. It is also evident that the torque ripple of TLI drive is higher than that of drive with different levels of CHB. Torque ripple and harmonics have adverse effect on longevity and performance of motor, which is discussed in detail in sec. 8.6. If the vehicle is deployed uphill, it has to bear more torque than that of driving on plain surface, because, it has to overcome the inclination and aerodynamic resistance including its own load torque. The Fig. 8.13(d) shows that speed is stable at its nominal value while load torque of drive is varied. The Fig. 8.13(e) shows drive operations at different speed. The torque increases to meet the speed command and then settles at steady state value. Thus, this shows the decouple FOC of PMSM drive, which gives better dynamics.

8.6 Evaluation of CHB Multilevel Topologies for Power Train

The determination of specific level among the available multilevel topologies for power train is critical for developing a prototype of EV. In this section, impact of number of levels on drive considering crucial parameters such as torque ripple and harmonics on electric motor, switching losses, and charging time of batteries are evaluated and discussed in detail.

A critical parameter for use of MLI in EV is designing strategy for arrangement of the multiple battery modules. CHB MLI has multiple distributed battery modules acting as dc source for each H-bridge, while power train in TLI has single stack with battery modules connected in series for same kWh capacity, as shown in Fig. 8.14(a). In order to realize the same kWh capacity using TLI, battery pack with higher voltage is used to reduce current level. It is achieved by series connection of low voltage battery cells which require additional charge balancing or equalizing circuits. Also in TLI, IGBT devices needs to be used due to high dv/dt. While, in battery pack of MLI has lower voltage battery modules connected in hybrid manner hence MOSFET devices can be used.

Another decisive parameter that stops EV from being popular is the charging time of EV. When the battery modules are distributed then the charging time can be minimized as each module will charge simultaneously. For instance, suppose that in a battery pack of 200 cells, there is one cell that accounts for 80% of its total capacity compared to the other cells. Then, the capacity of that battery pack is bounded to 80% of total nominal capacity. Also, let's assume that this particular cell takes longer time to charge, then the total charging time for the battery pack increases as the user has to wait until it is fully charged. Now, if the battery pack is divided into 10 modules with 20 in each and charged simultaneously using BMS, then only one of the modules will account for 80% of its capacity and the rest modules can yield 100% of their total capacity. This would boost the overall capacity of battery pack to 98% of total nominal capacity. In this way, charging of battery will be faster compared to the charging time taken by one battery bank formed by series connections of battery cells. Hence, use of MLI for EV can drastically change the current scenario related to the problems of charging time [373].

Also, the life of energy storage is an another substantial aspect for EV from maintenance point of view in long term use. The high temperature in cells due to losses in batteries will shorten the battery life. Of course, temperature of the battery also depends on the way battery modules are mounted, but there can be an uneven temperature in battery stack during operation. The MLI has capability to transfer the losses to less used part of battery stack at certain load conditions due to redundancy available for switching [376]. Tab. 8.2 shows all the redundancies to obtain voltage levels for 5-level inverter. For example, when the vehicle is running at lower speed, the converter works in lower voltage level (suppose level 3). To achieve

this level, out of 2 CHBs only one CHB module is in operation in accordance to the switching sequence selected from available voltage redundancies. Therefore, the battery module of that CHB is drained whilst battery module of second CHB maintains its charge. After sometime in order to balance the temperature, second CHB can be operated using other switching sequence from available pole voltage redundancies. In this way, a uniform temperature can be maintained throughout the stack resulting in the increased durability of the energy storage and hence improved reliability of the vehicle is achieved in the long run. Thus, maintenance can be reduced as replacement of battery module of EV is fiscally immoderate.

If any module fails, fault detect algorithm can help the vehicle to continually run on healthy modules by bypassing the faulty one. Of course, the speed of vehicle reduces as the MLI will work with lower number of levels and reduced modulation index. But, it does not stop like conventional ICE engine as well as EV using TLI technology, which can prevent the vehicle from severe accidents and damages and is called "limp-home-mode (LHM)". A faulty module can be replaced quickly and easily without affecting other modules [377]. Thus, the reliability and availability of drive scheme in case of faults is ensured.

One of the key feature of using CHB is that it gives multilevel operations along with the use of identical H-bridges with reduced harmonics. As shown in Fig. 8.14(b), THD reduces with increase in level of inverter and feeds motor with smoother output voltage. Since, if the stator current has harmonics then the motor is derated and requires large filter to mitigate the harmonics. THD is analyzed at different modulation indices for each inverter level. Modulation index (MI) 1 refers to nominal speed (6000 RPM) of the drive. Lower modulation indices refer to the lower speed of the drive. Elimination of bulky filters reduces cost, power loss and overall volume. Hence, use of MLI for electric vehicles also reduces size and weight of the vehicle. Higher amount of harmonics increases heating due to iron and copper losses at high harmonic frequencies. The insulation of motor windings deteriorates due to heating and thus reduces life of motor. Hence, the harmonic components affects the efficiency, torque developed and life of machine. The drive is expected to produce low torque ripple which avoids vibrations, noise and wear in EV. Increase in torque ripple damages the shaft and also gearbox of motor, which will increase the maintenance of vehicle. The Fig. 8.14(c), illustrates that as the number of level increases, sinusoidal voltage leads to reduction in THD, torque of drive smoothens and performance of drive is improved.

In power train with existing TLI, the switches have to block high dc-link voltage and have higher switching losses and hence higherdv/dt as show in Fig. 8.14(d). While in MLI each H-bridge has lower dc-link voltage across it, switches have to block lower voltage reducing switching losses and hence lower dv/dt. Due to lower blocking voltage of switches, their conduction resistance decreases, moreover MLI can operate at lower switching frequency, further reducing switching losses. Hence, the efficiency of the system can be increased by reducing the losses in the system. However, the number of switches also increases with increase in level. High dv/dt

leads to electromagnetic interference and over voltage at motor terminal, which results in failure of motor bearings and shortens motor life. Lower rated devices will need lower rated gate drivers, sensors, and low value capacitor for dc-link. Thus proposed MLI reduce the requirement of bulky and heavy heat sink.

Hence, according to the discussion and results, 5-level inverter has lowest THD, torque ripple and switching losses compared to TLI. Management of energy storage system for 5-level does not increase the complexity as compared to higher levels. The implementation of the higher number of level has direct impact on the initial cost of switches of the drive. However, the limiting factor that stops to implement highest number of MLI could be conduction losses as more number of semiconductor devices are switched on simultaneously. On the other side, low voltage devices also exhibit very low conduction resistance, resulting very low losses. Also, since low rating MOSFETs can be used, paralleling of MOSFETs can be implemented to reduce conduction losses further. The Fig. 8.14(e) shows the cost of switches used for different levels of CHB topology. as the number of level increases, device count will increase and will obstruct to go for highest level. Trade-off between the performance and initial cost of drive has to be made depending on the application.

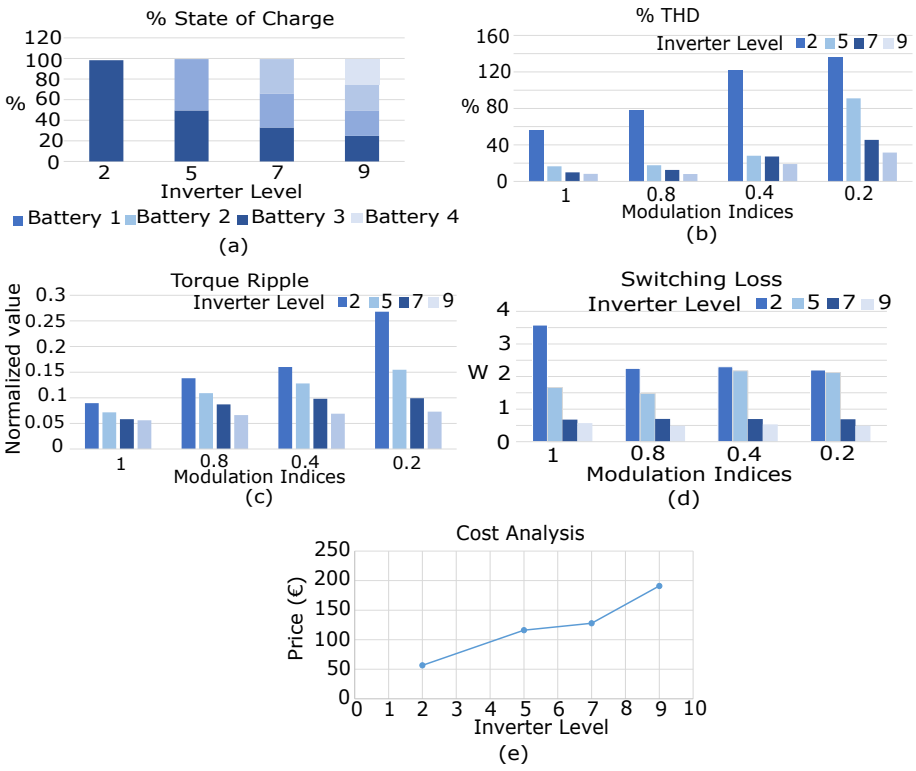


Figure 8.14: (a) % SOC of battery modules for different inverter levels, analysis of (b) % THD (c) torque ripple (d) switching loss for each inverter level at modulation indices 1, 0.8, 0.4, 0.2 (e) cost analysis of switches for each inverter level.

9 Summary and Future Work

9.1 Conclusions

Nowadays power conversion is an integral component of any electrical infrastructure. They are ubiquitous and have myriad applications ranging from high-voltage power distribution to low-voltage residential automation. Due to the increasing system efficiency demands, the need of power converters have accentuated over the years and it has emerged as a proliferating industry. The increasing need toward high power density is emphasizing the need of advanced converter topologies and in recent years multilevel converters structures successfully replaced traditional VSI in many medium/high power applications.

This PhD thesis work presented a three-phase 33-level CHB multilevel inverter prototype. The hardware design of its main parts has been discussed, several innovative modulation techniques (with an emphasis on grid-connected and low switching frequency applications) have been presented and implemented on the converter prototype and the carried out experimental results have been shown and discussed.

The testing results were examined in terms of granting high efficiency, reliability and flexibility of the converter and in terms of meeting the requirements of IEEE standards for the power grid connection. According to these standards, an inverter cannot be directly connected to the grid if the strict THD requirements in the line to neutral voltage and current are not satisfied. The developed multilevel converter prototype successfully passed the tests in low power conditions and it is now ready to be tested in medium and high power applications.

Among all the innovative modulation techniques presented in this thesis, the Pulse Active Width Modulation (PAWM) is the one which shown the best results in comparison with the literature well-know fundamental frequency modulations such as Selective Harmonic Elimination (SHE) and Selective Harmonic Mitigation (SHM).

The developed fundamental frequency modulations have been proposed in chapter 5, while the state of the art of the modulation techniques has been described in chapter 4.

The main topologies of multilevel converters have been presented in chapter 3.

In chapter 7 the 33 level three-phase CHB converter realized in the DigiPower Ltd labs has been presented and in chapter 8 some of its more suitable applications have been discussed.

9.2 Future Work

The described configuration of the multilevel power converter prototype is expected to be very useful in medium/voltage applications. However, the design of a such complex hardware and its control and modulation concepts are a relatively new approach for power electronic converters that will affirm their main role only in the next years.

Until now, it is possible to confirm that the system has not presented any unexpected behavior with only one exception. During the tests performed in the Digipower Ltd labs, it was discovered the presence of circulating current between the H-bridge modules. A first investigation highlighted that the origin of this current can be found in the snubber circuits. While in a conventional H-bridge the current that is released during the snubber capacitor discharging phase is forced to circulate directly into the load, when more than one H-bridge module are connected in series this current can flow through different paths, depending on the applied switching pattern (which changes during the time on the base of the modulation index M and on the chosen modulation technique).

When the operating region, circulating currents, dc-side quantities, and ac-side quantities are analyzed, the capacitor voltages are often assumed to be well balanced which is equivalent to assume an infinite switching frequency. However, as already discussed in chapter 4 and in chapter 5 of this thesis, one of the key features of the multilevel converter is the possibility to operate at low switching frequencies. Therefore, the lower limit of the switching frequency was investigated. It was found that when the switching frequency is reduced, it is possible to control and reduce the circulating currents to a value equal to $\sim 10\%\, I_n$. However, this will increase the capacitor voltage ripple, meaning that there is a trade-off between the switching frequency and the capacitor voltage ripple and size. This problem has never been investigated in literature and it will need further investigations to be overcome.

Obviously, the implemented topology and its possible variations need more research efforts, especially in the field of high power applications with low switching frequency modulations. Future research should be focused on examining the following aspects:

- Perform a test with the nominal phase voltage of $10\,kV$.
- Reach the nominal power of the converter equal to $1MW$.
- Perform a thermal stability studies with special attention to the reliability evaluation for different thermal cycling with experimental verification.
- Fix the circulating current issue.
- Continue the tests of the converter prototype in the high power motor drive field.
- Continue the tests of the converter prototype for STATCOM applications.

- Optimize and improve the converter hardware.
- Evaluate the replacement of the cables used for the connection between the H-bridge modules and the main controller board with an optical fiber connection.

All these studies may lead to minimize both, the harmonic content of the output voltage and current and the dynamic power losses, enhancing the overall efficiency and reliability of the power converter.

Further improvements in the implemented control algorithm could also grant a better stability and superior dynamic performances of the whole system.

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