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Development of a Low Cost Power Meter Based on A Digital Signal Controller

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Abstract:
The monitoring of power quality is a central topic for both household electrical and industrial equipment. Typically, the lacks of quality in a power system (both a public mains and an industrial power supply network) involve interruptions and deviations of the actual supply signals from the nominal characteristics, with potential annoying effects in electrical power systems and problems in industrial and communication apparatus. In this paper, the design and implementation of a measuring system based on a high-performance microcontroller that carries out the power quality analysis of the mains is presented. The system measures the fundamental parameters related to the system under monitoring, that can be a single or a three phase network. The proposed measurement instrument is mainly based on the Microchip PIC32MZ2048ECH100 Digital Signal Controller (DSC) and the Texas Instruments ADS8558 A/D converters (ADCs). Starting from voltage and current sampled values, simultaneously acquired by the converters, the DSC calculates the following parameters: frequency; RMS voltage; RMS current; phase shift; active power; reactive power; apparent power; THD. The measured parameters are also externally transmitted via a serial link. In the paper a prototype of the proposed instrument is described. It is linked to a PC and results shown on a LabVIEW based user interface, reporting also results from lab tests during the metrological characterization phase. Its main features (cost effectiveness, reduced dimensions and low power consumption) make it suitable for installation into existing electric cabinet of civil and commercial users. The continuous and real-time monitoring capability, managed both locally or remotely, is one of the most interesting features.

Keywords: power quality, power measurement, digital signal controller

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1 Introduction

The real-time monitoring of electrical energy consumption, or production from renewable sources, is an essential feature for improving energy efficiency in the domestic, commercial and industrial applications [1–4]. In the actual scenario of bidirectional energy flow to and from the grid, the energy users have become energy "prosumers" [5–9], making it even more important the power quality measurements. For the choice of a suitable monitoring device, features as cost effectiveness, reduced dimensions and low power consumption are critical issues [7].

Different instruments and small devices are today commercially available, even if both of these typologies present some disadvantages. High performance instruments are able to measure the different parameters in real-time and to operate a continuous monitoring of the supply network, but both the cost and the physical dimensions make impossible their adoption in some applications. On the other hand, small low-cost systems are not able to continuously monitor the network and to guarantee reduced measurement uncertainties.

In this paper we present the design and implementation of a low cost measurement system that is able to continuously analyze and monitor basic parameters of single-phase or three-phase mains. The proposed transducers are designed to be installed into existing electric cabinet, in which it is not easy and cost effective to install new and large equipment. Voltage and current ranges make possible its adoption in many civil and commercial applications.

As part of the development phase, a prototype of the proposed system has been implemented. This is a DSC based data acquisition and processing system that converts current and voltage signals, executes the measurement algorithm and transfers data to a remote computer. The proposed instrument presents a simple design, based on widely used components. Its main advantages are reduced cost and dimensions, and high performances. The implemented prototype has been metrological characterized using a Fluke 6100A Power Standard.

Edoardo Fiorucci is the corresponding author.

The system presented in this paper has been designed and developed in the Edison Laboratory "New technologies for energy monitoring" of the University of L'Aquila.

2 The proposed Power Meter

The proposed system architecture, shown in Figure 1, is mainly composed of three blocks: (i) the signal conditioner, that adapts both voltage and current input analog signals; (ii) the data acquisition section, that synchronously samples and converts the six input signals; (iii) the DSC-based processing section, that processes the digital signals to evaluate the electrical indexes of system to test.

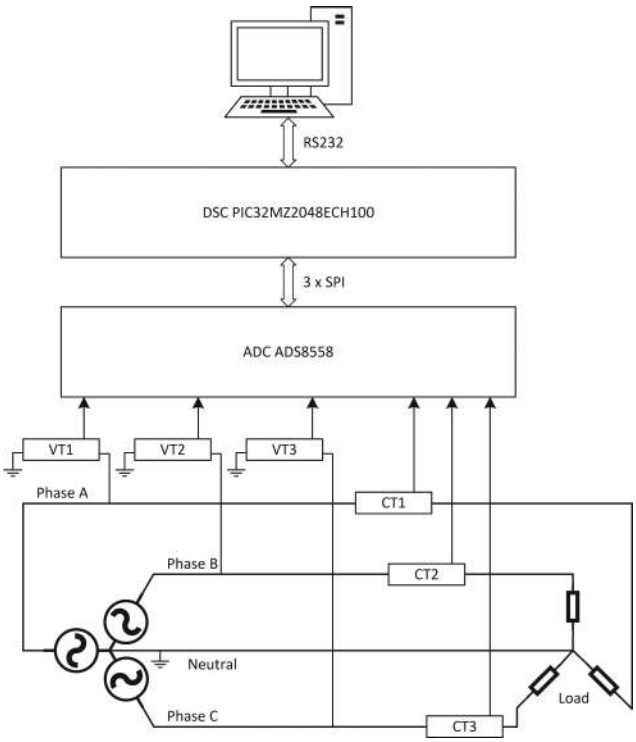

Figure 1: The proposed system architecture.

Core of the system is the DSC Microchip PIC32MZ2048ECH100, a high-performance microcontroller [10–13]. The DSC is a 200 MHz/330 DMIPS PIC, that embodies 2MB Flash memory, 512KB SRAM memory, 8 DMA Channels, 6 SPI interfaces, 5 I^2C interfaces, 2 CAN interfaces, 9 PWMs, Hi-Speed USB 2.0 Device/Host/OTG, 0/100 Mbps Ethernet MAC with MII and RMII interface.

Even if it includes ADC internal peripherals, it has been interfaced to an external ADC in order to improve the A/D conversion performance in terms of both number of bits and sampling frequency, and to synchronize all the channel sampling. The adopted converter is the Texas Instruments ADS8558 [7] that embodies six 12-bit SAR converters and six sample-and-hold circuits, operating at up to 500 kSample/s per channel. The six-independent ADCs acquire the three-phase current and voltage signals.

The DSC communicates with the ADC using three Serial Peripheral Interfaces (SPIs): each SPI channel transfers two ADC channels (phase voltage and current). The acquired signals are stored in the DSC internal memory, and processed. Finally, the measurement results are serially sent to a host PC and displayed on a suitable graphical interface developed in the NI LabVIEW environment.

2.1 The transduction and conditioning sections

The power range of the proposed system mainly depends on the adopted voltage and current transducer range [14, 15]. It has been configured to meet typical low voltage AC requirements: the nominal ranges have been set at 20 A_{rms} for the current and at 250 V_{rms} for the voltage, with a nominal power range of 5 kW. The adopted current transducer can measure up to 30 A_{rms}, with a maximum power of 7.5 kW.

2.1.1 The current measurement section

The current measurement section consists of a current transducer, and a fixed gain amplifier.

The transducer is the YHDC model SCT-013-030, suitable to transduce AC currents up to 30 A_{rms}, with a nominal ratio of 1800:1, and a nominal nonlinearity lower than ±1 % [16]. Working temperature is from -25 °C to +70 °C. The current transducer has a split-core and reduced dimensions (32x34x22 mm), for an easy installation inside existing electrical cabinet. The output current is applied to a 62 Ω resistor, to generate a voltage up to ±1 V, as shown in Figure 2. The overall transduction scale factor is 29.03 A/V.

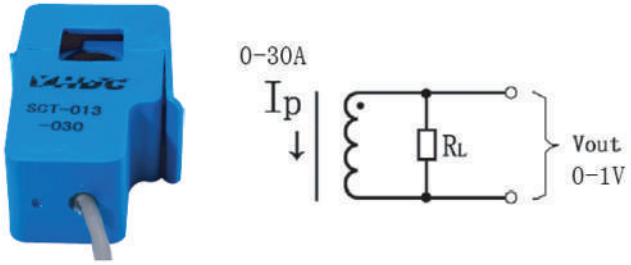

Figure 2: Current transducer and electrical equivalent circuit.

The current conditioning circuit shown in Figure 3 amplifies this signal up to ±10 V.

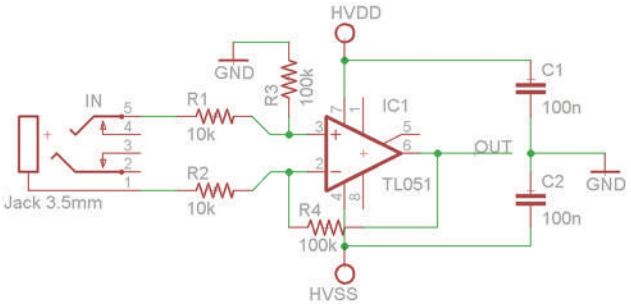

Figure 3: Current transducer conditioning circuit.

2.1.2 The voltage measurement section

In order to mainly reduce the cost, an active voltage transducer has been implemented. It attenuates the nominal 250 V_{rms} input phase voltage to ±10 V output voltage, with a transduction scale factor of 35.35 V/V. The circuit, based on a differential amplifier, is shown in Figure 4.

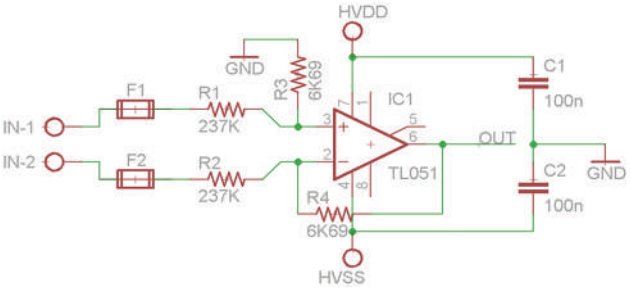

Figure 4: Voltage transduction and conditioning circuit.

2.2 The developed conditional board

A prototype of the voltage and current conditioning circuits has been implemented on the board shown in Figure 5. The board embodies input connectors, for connecting the three current transducer signals and the three phase voltages, and an output connector, for the connection to the processing board.

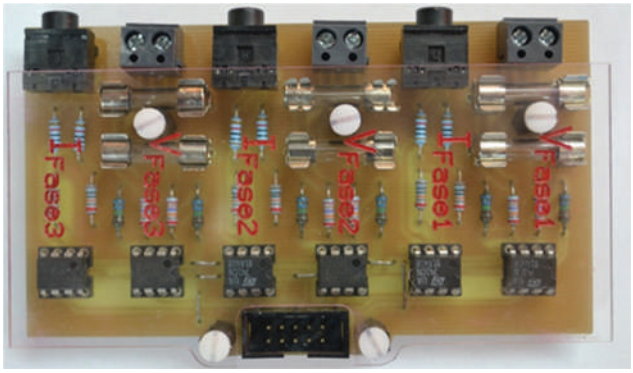

Figure 5: Signal conditioning board.

3 The developed DSC board

The Texas Instruments ADS8558 samples and converts the six channels at 12 bits. The sampling is synchronous, in order to avoid the time shifting between the channels. This requirement is very important because the proposed system measures time sensing electrical indexes. The start of conversion (CONVST), driven by the DSC, defines the sampling instants.

The overall sampling time has been chosen to store 10 periods of a 50 Hz signal, in order to have $N = 2048$ samples for each channel, according to the requirements for Class A instruments in IEC 61000-4-30 [17]. So, the sampling rate for each channel is 10,240 Hz. When the 2048 samples are stored into software buffers, implemented in the DSC, the processing routines start. Simultaneously, the system continues to acquire another set of 2048 samples in a second buffer. In Figure 6 a simplified data-flow diagram is reported: at each sampling time the SPI 1–3 transfer the six samples from the ADS8558 to the DSC, that are stored in the internal buffers. As an example, in Figure 7 the of CONVST, BUSY, FS and SCLK signals during an A/D conversion and related data transfer to the DSC is reported. The CONVST is the sampling signal: after its low-to-high transition, the ADS8558 starts the six synchronous sampling and conversion. When CONVST returns low, the ADS8558 transfers data to the DSC using the SCLK signal, driven by the DSC.

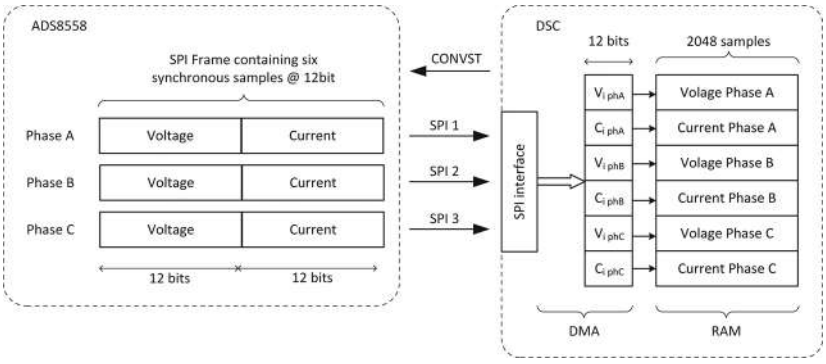

Figure 6: Simplified data-flow diagram.

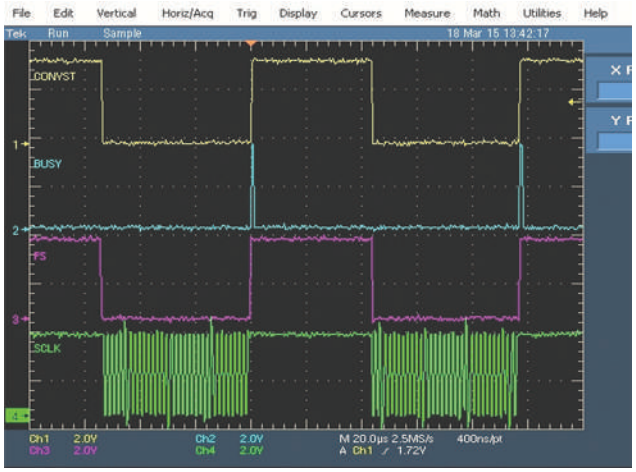

Figure 7: Signals acquired during a conversion and a transfer.

The six samples received from SPI interface are moved into the six 2048-buffers using the DMA controller. At the end of these 2048 transfers the CPU runs the measurement algorithms. In this way, the DMA executes the data transfer and the CPU the data processing: the two tasks are independent and executed in parallel. The time required to transfer and store the six 2048-samples is 200 ms, while the processing time is 180 ms. This result shows that the whole system can process all the 2048 sample for each channel without losing the real-time: the measurement is carried out continuously.

The implemented signal acquisition and processing board is shown in Figure 8; Figure 9 shows the top layer of this board.

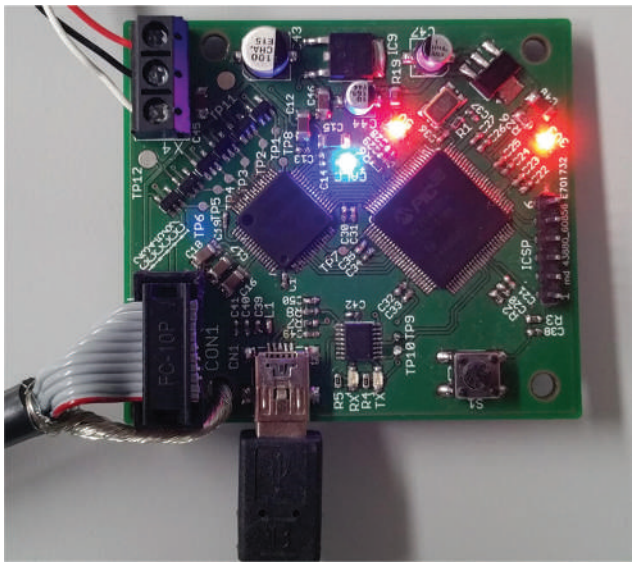

Figure 8: The implemented DSC board.

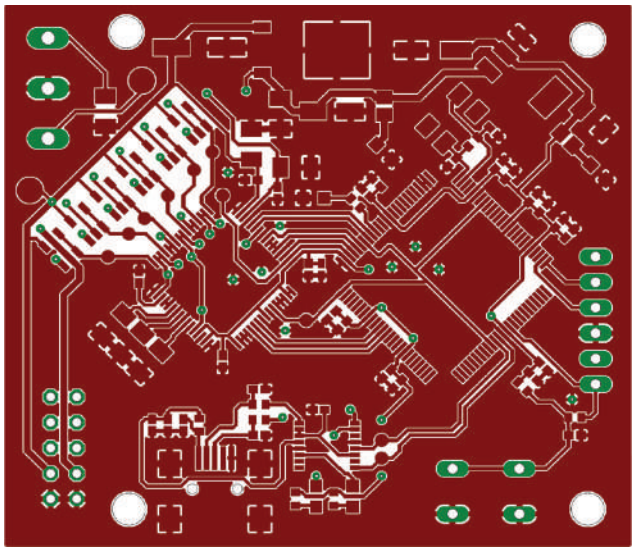

Figure 9: Top layer of developed DSC board.

4 The software measurement architecture

The implemented measurement algorithms evaluate the following quantities: RMS voltage and current, total harmonic distortion indexes, frequency, power factor, apparent power, active power and reactive power. Some parameters (e. g. the power) are calculated for each phase and then for the overall system. In the following sections, the algorithms are presented in details.

4.1 Frequency measurement algorithm

The period (or frequency) is measured by applying the zero crossing method. This technique presents many advantages: simple implementation, reduced computational load, and fast execution.

A simplified block representation of this algorithm is depicted in Figure 10. Before applying it, the 2048 12-bit acquired samples (Data Buffer in Figure 10) are processed by means of a moving average filter and stored in the Mean Data Buffer. This low-pass filtering helps to restrict the bandwidth to the frequencies close to the signal frequency and to reduce the superimposed noise. The zero crossing algorithm has been implemented using the eq. (1). When the two conditions are true (at the zero crossing from negative to positive values) the algorithm store 1 at the actual (i) position of the One-Zero Buffer, and 0 in the other cases. The number of 1 corresponds to the number of acquired cycles N_{cycles}, while the distance between two ones is the DIM_{cycles} .

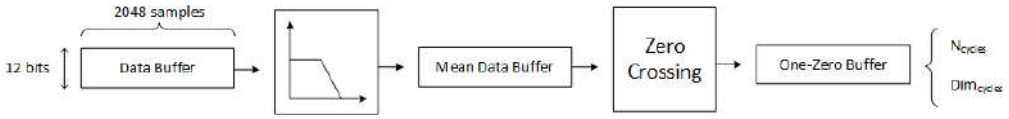

Figure 10: The frequency measurement algorithm.

The mean value of the frequency is obtained by applying the eq. (2), where 10240 is the sampling frequency.

$$\begin{cases} DataBuffer\,(i-1) \cdot DataBuffer\,(i) < 0 \\ DataBuffer\,(i) > DataBuffer\,(i-1) \end{cases} \tag{1}$$

$$Freq = \frac{N_{cycles}}{\sum_{i=0}^{N_{cycles}-1} Dim_{cycle}\,(i)} \cdot 10240\,Hz \tag{2}$$

4.2 Root Mean Square (RMS) algorithm

The root mean square (RMS) values of the acquired voltage and current samples are evaluated using the following formulas ($N = 2048$):

$$V_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} V_i^2} \ [V_{\mathrm{RMS}}] \tag{3}$$

$$I_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} I_i^2} \ [A_{\mathrm{RMS}}] \tag{4}$$

4.3 The power measurement algorithms

Starting from the acquired voltage and current waveforms the active single-phase and three-phase power are evaluated using the following formulas

$$P_{(1,2,3)} = \frac{\sum_{i=1}^{N} V_{(1,2,3)\,i} \cdot I_{(1,2,3)\,i}}{N} \ [W] \quad P_t = P_1 + P_2 + P_3 \ [W] \tag{5}$$

The single-phase reactive power is evaluated by the following formula

$$Q_{(1,2,3)} = \sqrt{S_{(1,2,3)}^2 - P_{(1,2,3)}^2}\,[VAR] \tag{6}$$

while the three-phase reactive power is:

$$Q_t = Q_1 + Q_2 + Q_3\,[VAR] \tag{7}$$

The apparent single-phase power is evaluated by multiplying the RMS voltage across the load with the RMS current through the load:

$$S_{(1,2,3)} = V_{RMS(1,2,3)} \cdot I_{RMS(1,2,3)}\,[VA] \tag{8}$$

The apparent three-phase power is evaluated as:

$$S_t = \sqrt{P_t^2 + Q_t^2}\,[VA] \tag{9}$$

The power factor for single-phase and three-phase systems is the ratio between the related active and apparent powers:

$$pf_{(1,2,3,t)} = \frac{P_{(1,2,3,t)}}{S_{(1,2,3,t)}} \tag{10}$$

4.4 The Total Harmonic Distortion (THD) algorithm

The Total Harmonic Distortion (THD) level for voltage signals is obtained by applying a Hanning window to the voltage signal and by calculating the Fourier Transform using the FFT algorithm. The voltage THD is then calculated as the effective value of all the harmonics (up to the 40^{th}) divided by the effective value of the fundamental.

$$THD_{(1,2,3)} = \frac{\sqrt{\sum_{i=2}^{40} V_{i_{(1,2,3)}}^2}}{V_{1_{(1,2,3)}}} \cdot 100\ [\%] \tag{11}$$

5 Metrological characterization of the proposed system

The primary overall metrological characterization of the power analyzer has been carried out using a Fluke 6100A Power Standard, making trimming adjustments of the amplifiers and attenuator resistors, in order to obtain the desired gains. After these internal adjustments, the measured values were compared against the known external source references, and the coefficients adjusted to match these parameters.

The first test has been carried out setting the input voltage at 230 V and the input current at 5 A and measuring the instrumental constants for the RMS of input voltage and current, and for the active power. These values have been saved as internal constants in the microprocessor memory and applied for the measurement compensation.

Figure 11 shows a phase of the tests, while Figures 12 and 13 show the signals of voltage and current transduction and conditioning sections, for an input voltage of 250 V, an input current of 30 A, at 50 Hz.

Several tests of the proposed instrument have been performed to highlight its performance varying the different input parameters. More in details, we analysed the system performance in terms of uncertainty of measured quantities changing the related measurement parameter.

Figure 14 shows the percent error related to the input voltage measurement, for the three phases, for a voltage ranging from 25 V to 250 V. The error in mainly lower than 0.7 % and increase to 2.2 % in the lower part of the input range.

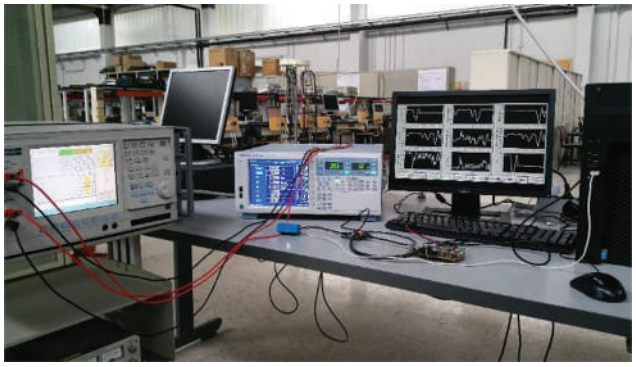

Figure 11: Metrological characterization of the proposed instrument.

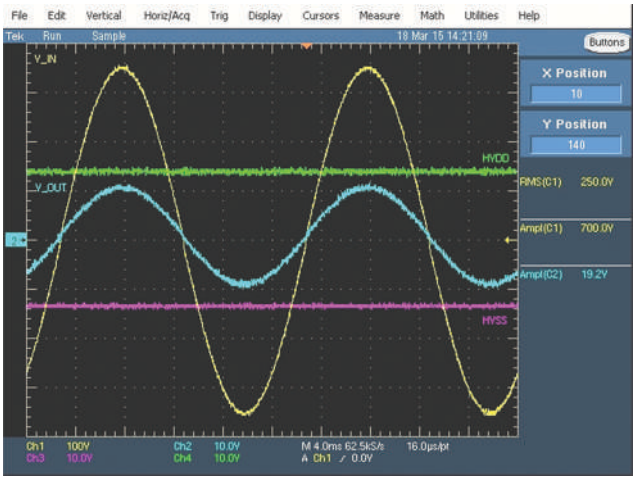

Figure 12: Signals acquired during the characterization of a voltage input section.

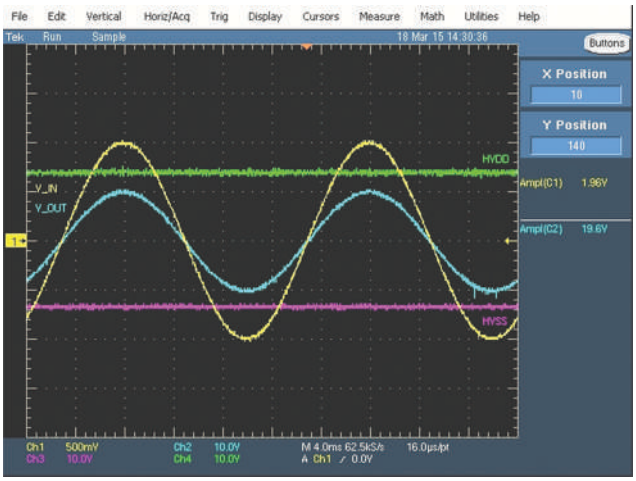

Figure 13: Signals acquired during the characterization of a current input section.

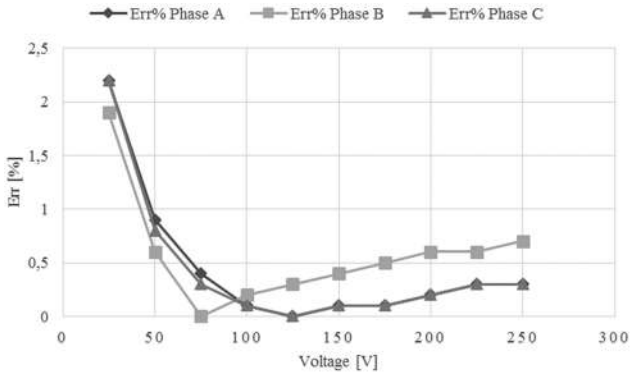

Figure 14: Percent error during voltage variation.

Figure 15 shows the percent error related to the input current measurement, for the three phases, for a current ranging from 2.5 A to 20 A. The error in always lower than 0.2 %.

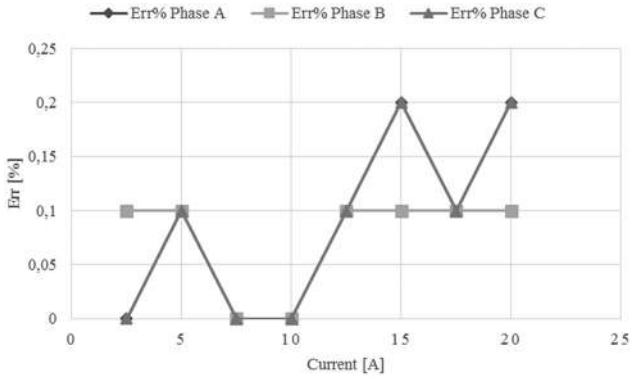

Figure 15: Percent error during current variation.

In Figure 16 the error related to the frequency measurement is shown, for the frequency in the range between 33 Hz and 63 Hz. The error, lower than 0.7 % is around zero at the nominal frequency value.

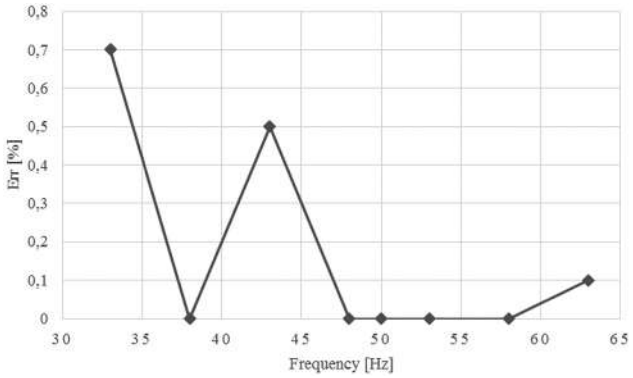

Figure 16: Percent error during frequency variation.

Figure 17 show the active power measurement error in the range from 500 W to 5000 W; the error is generally lower than 1.2 % in quite all the measurement interval. The apparent power (Figure 18) has a maximum error of 1.3 %, but only in one point and only for phase A. In the other measurement point is less than 1 %.

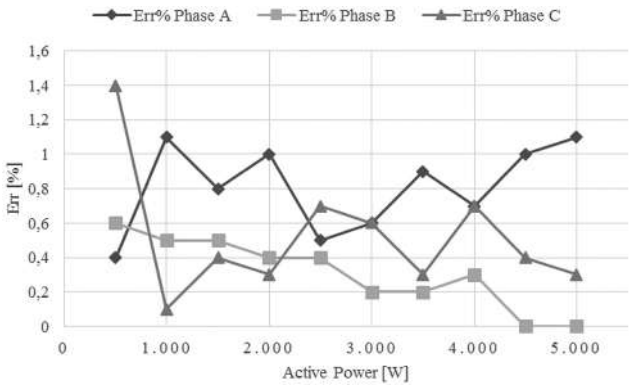

Figure 17: Percent error during active power variation.

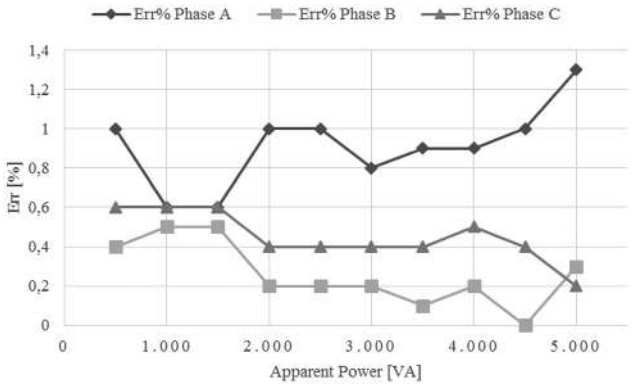

Figure 18: Percent error during apparent power variation.

As concerning the reactive power (Figure 19) the error is lower than 1.2 %, except for the point corresponding at 500 VAR.

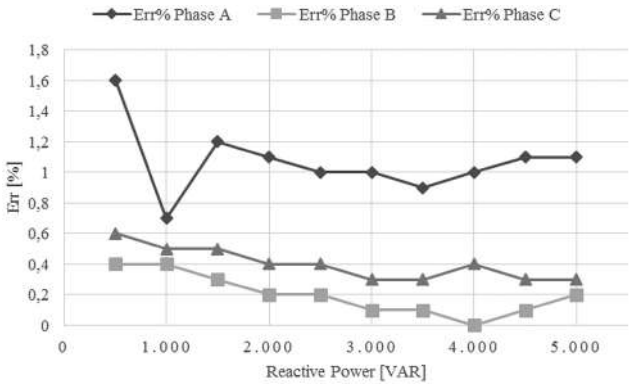

Figure 19: Percent error during reactive power variation.

Errors in the measurement of both power factor and phase have been reported respectively in Figure 20 and Figure 21,

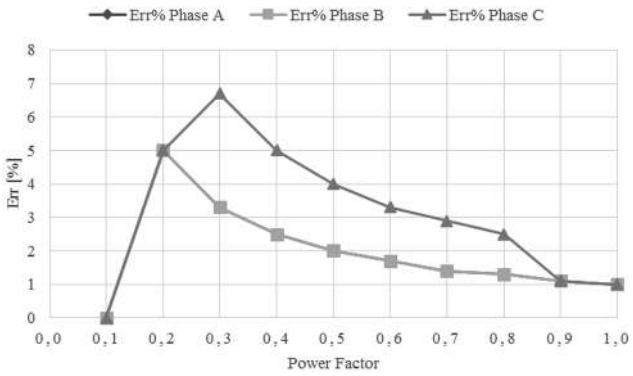

Figure 20: Percent error during power factor variation.

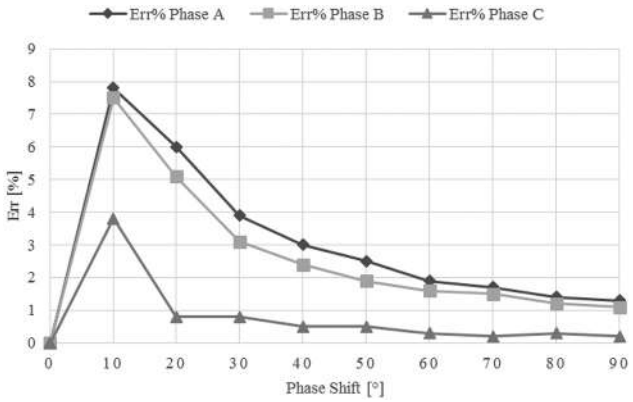

Figure 21: Percent error during phase shift variation.

The Figure 22 shows the errors related to THD measurement, always lower than 0.8 %.

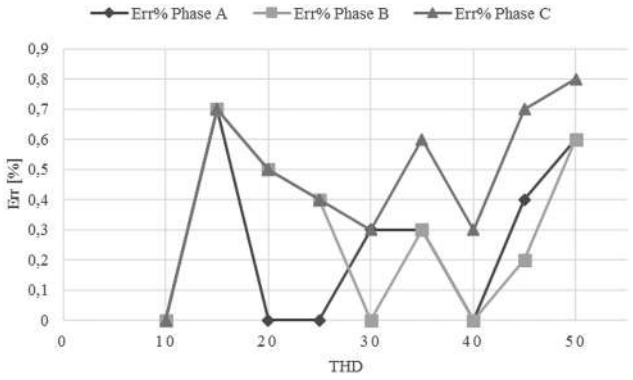

Figure 22: Percent error during THD variation.

As a general comment to the reported results, the system shows a quite good behavior.

6 Results obtained under non-sinusoidal condition

The performance of proposed system under non-sinusoidal conditions has been investigated according to the EN 62053–21 [18]. This standard refers to static watt-hour meters (accuracy classes 1 and 2) for the measurement of alternating current electrical active energy. According to it, we carried out the tests under the following main conditions:

1. current at the fundamental frequency: $I_1 = 0.5 \cdot I_{max} = 8$ A;
2. voltage at the fundamental frequency: $U_1 = U_n = 230$ V;
3. power factor at the fundamental frequency: 1;
4. 5th voltage harmonic: $U_5 = 0.1 \cdot U_n$;
5. 5th current harmonic: $I_5 = 0.4 \cdot I_1$;
6. power factor at the fundamental frequency: 1.

During the tests, we configured the Fluke 6100A to generate the signals with the characteristics specified in Table 1, adopting the Budeanu [19] definitions of power quantities. We obtained the results reported in Table 2, for the each phase of the measurement system.

Table 1: Setting for the proposed system test under non-sinusoidal conditions.

#	V_{rms} [V]	I_{rms} [A]	cos ϕ_1	pf	P [W]	S [VA]	D [VAR]	THD$_V$	THD$_I$	f [Hz]
	$230 + U_5$									47
1		8.0	1.0	0.99	1830.78	1840	184	10 %	0%	50
	231.1									52
		$8 + I_5$								47
2	230		1.0	0.92	1686.39	1840	736	0%	10 %	50
		8.6								52
	$230 + U_5$	$8 + I_5$								47
3			1.0	0.95	1751.53	1840	563	10 %	10 %	50
	231.1	8.6								52

Table 2: Results obtained under non-sinusoidal conditions.

#	f [Hz]	Phase	V_{rms} [V]	e$_V$ %	I_{rms} [A]	e$_I$ %	P [W]	e$_P$ %	S [VA]	e$_S$ %	D [VAR]	e$_D$ %	pf	e$_{pf}$ %
	47	L1	227,4	1,60	8,0	0,00	1820	0,59	1829	0,60	186	−1,09	0,99	0,00
		L2	227,7	1,47	8,0	0,00	1818	0,70	1830	0,54	184	0,00	0,99	0,00
1		L3	227,6	1,51	8,0	0,00	1817	0,75	1826	0,76	181	1,63	0,99	0,00
	50	L1	228,3	1,21	8,0	0,00	1826	0,26	1836	0,22	183	0,54	0,99	0,00
		L2	228,2	1,25	8,0	0,00	1825	0,32	1837	0,16	183	0,54	0,99	0,00
		L3	228,3	1,21	8,0	0,00	1826	0,26	1837	0,16	182	1,09	0,99	0,00
	52	L1	228,3	1,21	8,0	0,00	1819	0,64	1828	0,65	188	−2,17	0,99	0,00
		L2	228,1	1,30	8,0	0,00	1818	0,70	1829	0,60	187	−1,63	0,99	0,00
		L3	228,3	1,21	8,0	0,00	1815	0,86	1830	0,54	188	−2,17	0,99	0,00
	47	L1	228,3	0,74	8,4	2,33	1667	1,15	1825	0,82	736	0,00	0,92	0,54
		L2	228,2	0,78	8,3	3,49	1670	0,97	1828	0,65	738	−0,27	0,92	0,54
2		L3	228,3	0,74	8,4	2,33	1667	1,15	1826	0,76	737	−0,14	0,92	0,54
	50	L1	228,2	0,78	8,4	2,33	1683	0,20	1815	1,36	740	−0,54	0,92	0,00
		L2	228,1	0,83	8,5	1,16	1682	0,26	1820	1,09	738	−0,27	0,92	0,00
		L3	228,1	0,83	8,6	0,00	1683	0,20	1818	1,20	739	−0,41	0,92	0,00
	52	L1	228,4	0,70	8,6	0,00	1684	0,14	1826	0,76	737	−0,14	0,92	0,54
		L2	228,3	0,74	8,5	1,16	1682	0,26	1824	0,87	736	0,00	0,92	0,54
		L3	228,3	0,74	8,5	1,16	1683	0,20	1826	0,76	736	0,00	0,92	0,54
	47	L1	227,5	1,56	8,3	3,49	1732	1,12	1819	1,14	572	−1,60	0,94	1,05
		L2	227,6	1,51	8,2	4,65	1737	0,83	1823	0,92	570	−1,24	0,94	1,05
3		L3	227,7	1,47	8,3	3,49	1736	0,89	1821	1,03	570	−1,24	0,94	1,05
	50	L1	228,1	1,30	8,4	2,33	1742	0,54	1814	1,41	568	−0,89	0,94	1,05
		L2	227,9	1,38	8,4	2,33	1746	0,32	1815	1,36	569	−1,07	0,94	1,05
		L3	228,1	1,30	8,4	2,33	1744	0,43	1814	1,41	569	−1,07	0,94	1,05
	52	L1	227,2	1,69	8,3	3,49	1731	1,17	1812	1,52	578	−2,66	0,94	1,05
		L2	227,4	1,60	8,3	3,49	1735	0,94	1815	1,36	573	−1,78	0,94	1,05
		L3	227,2	1,69	8,2	4,65	1733	1,06	1811	1,58	575	−2,13	0,94	1,05

7 Data transmission between DSC and PC

After completing the signal processing task, the DSC transmits an array of 31 float (32 bits) measured parameters to a PC, via a serial communication link. The transfer rate is set at 115,200 bit/s. The data are packetized in a small bundle that consists of a start word, the sequence of measured data and a stop word, as shown in Figure 23. The total transferred bits are 1320, while the transfer time is 11.45 ms. This time interval is very short when compared with both the processing time (180 ms) and the acquisition and conversion time (200 ms). This means that data are transferred before the system completes the new measurement process, so the system can operate in a strong kind of real-time.

(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
Start	Frequency Phase 1	Frequency Phase 2	Frequency Phase 3	RMS Voltage Phase 1	RMS Current Phase 1	RMS Voltage Phase 2	RMS Current Phase 2	RMS Voltage Phase 3
(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)	
RMS Current Phase 3	Active Power Phase 1	Active Power Phase 2	Active Power Phase 3	Total Active Power	Reactive Power Phase 1	Reactive Power Phase 2	Reactive Power Phase 3	
(17)	(18)	(19)	(20)	(21)	(22)	(23)	(24)	
Total Reactive Power	Apparent Power Phase 1	Apparent Power Phase 2	Apparent Power Phase 3	Power Factor Phase 1	Power Factor Phase 2	Power Factor Phase 3	Power Factor 3-Phase	
(25)	(26)	(27)	(28)	(29)	(30)	(31)	(32)	
Phase Shift Phase 1	Phase Shift Phase 2	Phase Shift Phase 3	Phase Shift 3-Phase	THD Phase 1	THD Phase 2	THD Phase 3	Stop	

Figure 23: The packet of measures transmitted to the PC.

A LabVIEW VI has been implemented on the PC to interface the Power Analyzer and visualize the measured parameters. Figure 24 shows the front panel from which the operator can set the data rate, select the communication port and visualize the results, while graphical visualization of measured parameters are in Figure 25.

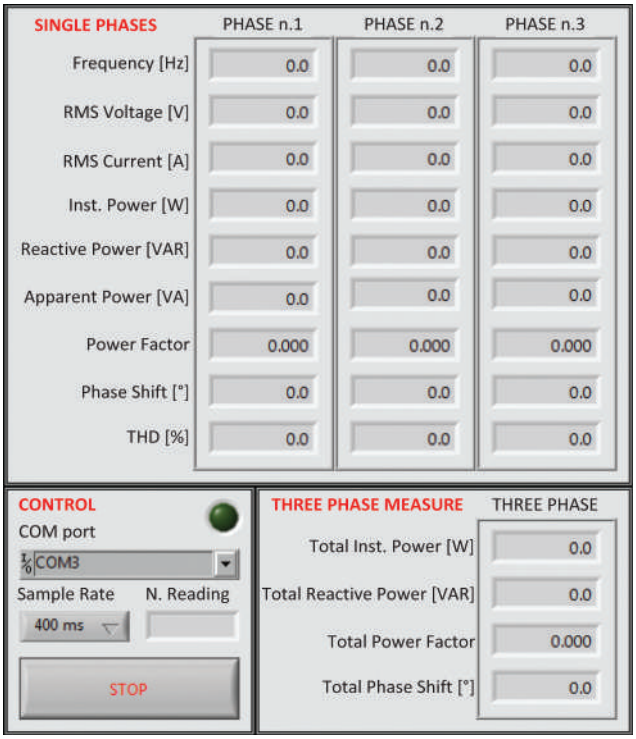

Figure 24: The PC operator front panel.

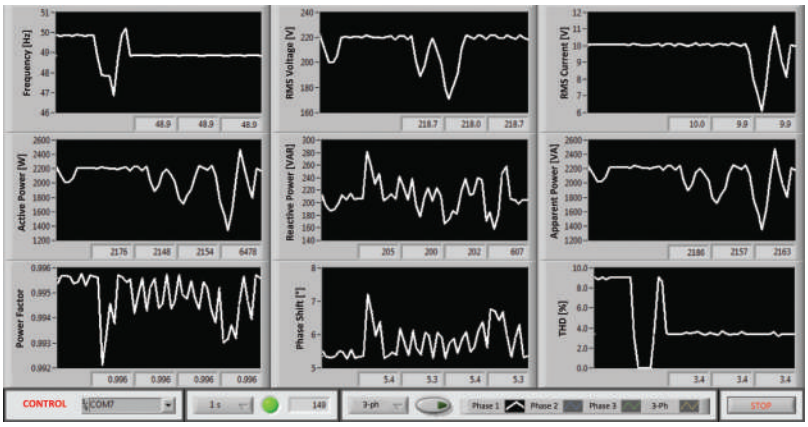

Figure 25: Graphical visualization of measured parameters.

8 Conclusions and discussion

In this paper a DSC based Power Quality analyzer has been presented. It allows for the continuous and real-time monitoring of a single or three phase network. Voltage and current ranges make possible its adoption in many civil and commercial applications. Current transducer size and split core feature make it possible to insert it inside existing electrical cabinet. The proposed analyzer can also be applied inside power electronic equipment, where the supplied measurements are required for some technical reasons. This justify the adopted hardware architecture, that allows for quick changes as concerning the parameters under measurement.

In this paper we propose a connection of the analyzer to an external PC, via a serial communication link to display measurement data. A direct connection to a small internal display (e. g. a touchscreen) has been analyzed as a possible solution, but it is our opinion that the adopted one presents different application advantages. As concerning its application inside a cabinet, it is infrequent the necessity to directly read the supplied results. More often a remote transmission is required. The overall data transfer requires just 11.45 ms, for a total of around 192 ms, maintaining the real-time operation.

As concerning its application inside an equipment or an apparatus, as a type of OEM system, the serial communication is the most common required interface. Works are in progress to implement a wireless data transmission for an easy installation of the analyzer.

Some results obtained during the test of the first prototype, according to the EN 62053–21, have been reported and discussed.

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