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Design and Control Implementation of Single Star Bridge Cell Multilevel converter for Static Synchronous Compensator

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DEDICATION

Dedicated to my parents and my wife for their endless love, motivation and support, and to my daughters, ***Wafa*** and ***Sama*** who have been born during the Ph.D. process.

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Undertaking the Ph.D. has been a truly life-changing experience for me, and it would not have been possible to do without the support and guidance of several people. I would, therefore, like to sincerely thank all of them.

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L'Aquila, Italy

Ahmed Majed Saif

ABSTRACT

Modular multilevel cascaded converters (MMCC) prove to be well-suitable for high and medium voltage systems due to their lower cost and high-redundance design. For STATCOM, Single-Star Bridge-Cell (SSBC) topology is well-applied for its satisfactory performance and superior component count. The feasibility of the adoption of SSBC-STATCOMs relies strictly on their performance and cost-effectiveness. Theoretically, harmonics performance improves with increasing the number of levels. However, this has a direct effect on their design and hence on overall complexity and cost. Besides, when the number of levels increases, more switches are required to be parallelly controlled. Therefore, software-based microcontrollers (e.g. DSPs) show limitations in terms of I/O built-in pins as well as performance. Alternatively, field-programmable gate-arrays (FPGAs), with their parallelism capability, are suitable for implementing the control of SSBC-STATCOM which is composed of output voltage control, internal current control, and capacitor voltage balancing. Although PI regulators are commonly used for their simplicity and ease in implementation, STATCOM system is essentially nonlinear, therefore, a nonlinear controller can effectively improve performance and robustness. Hence, this work initially focuses on investigating some key factors in STATCOM design with an emphasis on their impact on the overall cost in low and medium voltage applications. Then, a backstepping nonlinear control based on Lyapunov function design is proposed to regulate the overall capacitor voltage. Besides, detailed control design and implementation of the proposed control using FPGA is discussed. Hardware set-up of 142 V 9-level SSBC-STATCOM was designed to verify the results. The performance of the proposed method under V_{dc} step change and variation of system impedance has been analyzed and results were compared with the traditional PI controller. Besides, under fault operation, the unbalanced real power within the converter phases of SSBC results in more divergence of capacitor voltages and failure of the control system which affects the safety of the devices or leads to serious system collapse. The method of Zero-sequence voltage v_z is utilized to balance the capacitor voltage by adding its waveform to the three-phase ac voltages of the SSBC converter. It can redistribute the active powers between the three clusters without drawing a negative sequence current. Mathematical derivation of the v_z using positive and negative sequence is provided and control of STATCOM is simulated with the dual synchronous current control scheme.

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LIST OF ABBREVIATIONS

STATCOM	–	Static synchronous compensator
MMCC	–	Modular Multilevel Cascaded Converter
DER	–	Distributed energy resources
PV-STATCOM	–	Photovoltaic Static synchronous compensator
V2G	–	vehicle-to-grid
FACTS	–	Flexible AC transmission systems
SSBC	–	Single-Star Bridge-Cell
SDBC	–	Single-Delta Bridge-Cell
DSCC	–	Double-Star Chopper-Cells
DSBC	–	Double-Star Bridge-Cells
PWM	–	Pulse width modulation
HEPWM	–	Harmonics elimination PWM
PS-PWM	–	Phase shifted PWM
SVM	–	Space vector modulation
M_I	–	Modulation index
PSO	–	particle swarm optimization
AVC	–	outer voltage control
DVC	–	$dc-$link voltage control
MPC	–	Model predictive control
FPGA	–	Field programmable gate array
DSP	–	Digital signal processor
PLL	–	phase-locked loop
THD	–	Total harmonics distortion
TCPS	–	Thyristor-controlled phase shifter

TCSC	–	Thyristor-controlled series capacitor
SVC	–	Static VAr compensator
VSC	–	Voltage source converter
CSC	–	Current source converter
SSSC	–	Static synchronous series compensator
DVR	–	Dynamic voltage restorer
UPFC	–	Unified power flow controller
D-FACTS	–	Distribution FACTS
TCR	–	Thyristor-Controlled Reactor
TSC	–	thyristor switched capacitor
T-STATCOM	–	Transmission STATCOM
D-STATCOM	–	Distribution STATCOM
HF	–	High voltage
EHF	–	Extra-high voltage
MV	–	Medium voltage
LV	–	Low voltage
PCC	–	Point of common coupling
MVSI	–	Multilevel voltage source inverter
PD	–	Phase detector
LF	–	Loop filter
VCO	–	Voltage-controlled oscillator
SRF-PLL	–	Synchronous reference frame PLL
DDSRF-PLL	–	Decoupled double SRF-PLL
DSOGI-FLL	–	Double second-order generalized integrator FLL
WBG	–	Wide-bandgap semiconductor
SiC	–	Silicon carbide

GaN	–	Gallium nitride
	–	

CHAPTER 1

INTRODUCTION

1.1 Research Background

Recently, increasing attention is given to smart grids in which top-down electrical transfer from remote power plants to consumers is replaced by distributed energy resources (DERs). Increasing number of DERs has direct impact on reliability and stability of the power grid. This is due to (1) location of the DER, (2) varying size and operations, (3) intermittent and uncontrollable renewable energy sources, and (4) un-coordination among different DERs, which might cause voltage oscillations, reverse power flows on circuits with unidirectional flows, and cause other power quality problems. DERs are connected to grid network by power converters (Fig. 1.1 shows grid connection of wind farm), which flexibility allows, in addition to their main task, to mitigate power quality issues. Photovoltaic Static Compensator (PV-STATCOM) [6, 7] and vehicle-to-grid (V2G) [8] concepts are good examples in which sources in their idle mode can be utilized to perform other multiple functions involving reactive power compensation. Therefore, nowadays, grid codes and standards are being revised to facilitate such paradigm shift (e.g. IEEE 1547 [9]).

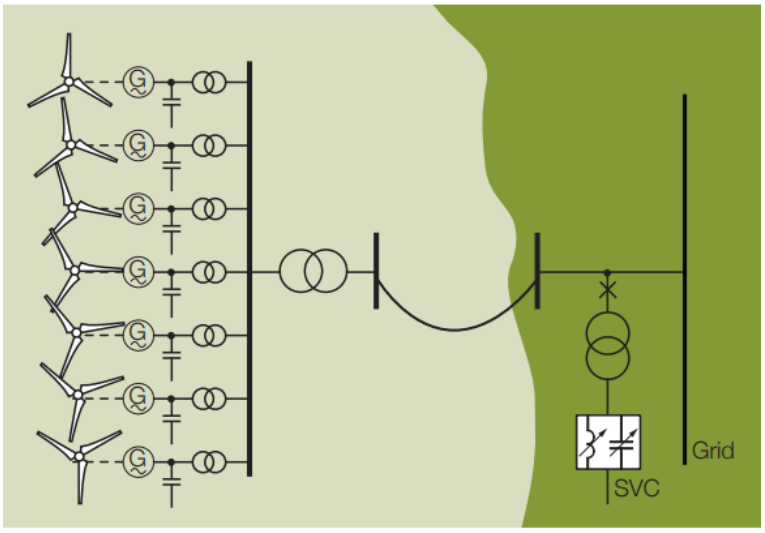


Figure 1.1: Grid integration of wind farm

Reactive power compensation is an important solution that was introduced to fulfill the demands concerning phase unbalance, voltage fluctuations, and harmonics distortion at the point of common connection of the grid [10, 11, 12] but, although for some limits, it can be considered as an attractive solution in many practical cases for avoiding the construction of new transmission lines, with significant and immediate benefits in terms of environmental and a concessional point of view as well as cost and time savings [13].

Static compensator (STATCOM) provides instantaneous and continuous reactive power in response to voltage fluctuation; it is also used for active harmonics filtering and flicker mitigation. Usually, it operates according to the voltage source inverter principle in which high operation speed of power semiconductors leads to unequaled performance. Among important research directions for STATCOM are: lower capacitor STATCOM [14, 15], DER based STATCOM [7, 8], and multiple STATCOM operation and stability [16]; structure-wise MMCC based STATCOM gains more interest [17, 18]. For instance, since May 2019, combined technologies scheme of MMC and thyristor switched capacitor (TSC) along with a High Voltage Mechanically Switched Capacitor Dynamic Network (MSCDN) was installed by GE to support the 400 kV Bolney substation in the UK which delivers dynamic reactive power range from -100 MVAr inductive (absorbing vars) to +225 MVAr capacitive (injecting vars). The scheme ensures stable operation of Bolney substation which is dedicated to supporting a highly-populated area of the south of London as well as high-voltage direct-current interconnectors with Europe.

Traditionally, the two-level voltage source inverter (VSI) with a series coupling inductor, is used as the main building block of the STATCOM. However, the output voltage of the VSI is characterized by high harmonics that require bulky and costly filters. Furthermore, for high and medium voltage interconnections, it is mandatory to use the line frequency (50 or 60 Hz) step-up transformer to match the output voltage of the VSI with the utility grid. This increases the cost, size, weight, and power losses of the overall system as well as affects its dynamics.

Thus, the multilevel VSIs (MVSIs) is being exploited to replace the two-level VSI [2]. The salient features of these topologies include: 1) modularity and scalability, to fulfill high-voltage level requirements, 2) feasibility of the direct connection to high-voltage networks without using transformers, therefore, reducing system size, cost, losses, and footprint, 3) superior harmonics performance due to the high level of the output voltage waveform in which a large number of submodules with low rating switches are used, thereby allowing a significant reduction in the filtering requirement, and 4) low expense for fault-tolerant operation due to utilization of standard, low voltage components, such as 600V-1200V IGBT. Among the others, modular multilevel cascaded converter topologies family (i.e. MMCC) proves to be more attractive for STATCOM due to its modularity and fewer component counts in addition to the general multilevel advantages of reduction of filtering requirements and consequently footprint and losses. The modularity concept of MMCC enables high prefabrication and in-factory testing, bringing to an overall reduction of project lead−time and enhancement of product quality.

Different topologies of MMCC have been presented in the literature which include Single-Star Bridge-Cells (SSBC), Single-Delta Bridge-Cells (SDBC) and Double-Star Chopper-Cells (DSCC) with either half or full bridge units structure. Among them, the SSBC-STATCOM (shown in Fig. 1.2) proves to be more applicable for positive sequence current injection and voltage regulation. Increasing the number of levels has positive impact on the overall performance of the system. However, it greatly affects the cost. Assuming SSBC as the reference basic module topology, for multilevel STATCOM, the controlling factor is the number of bridges (N) in each phase [19]. The selection of N accounts for the blocking voltage of the switches and consequently the input capacitor size. Therefore, with a higher number of levels, lower-cost switches and smaller capacitors can be utilized. In addition, this allows system operation with low switching frequency. Thus, filtering and thermal requirements can be reduced due to low losses. However, the number of components (switches, gate drivers, and voltage sensors) rises; consequently complexity of the system increases. The selection of N needs to be optimally selected to fulfill the cost and performance requirements.

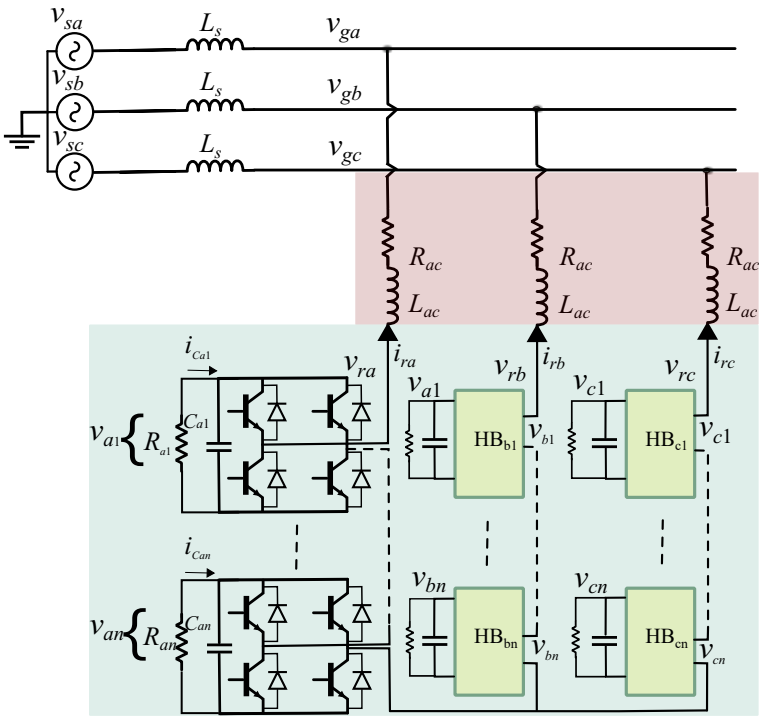


Figure 1.2: Three-phase SSBC based STATCOM

STATCOM performance is interrelated to the applied control strategy. Generally, it has two objectives: (1) it should be able to absorb small active power for compensating losses for charging the capacitors, and (2) it should rapidly compensate the reactive power by supplying or absorbing the required reactive current. A third objective is added for MMCC based STATCOM in which the capacitor voltage for each converter should be balanced under all operation for stable performance. Commonly, a hierarchical approach with different layers is considered to achieve these objectives [19]. By this approach, outer voltage control generates reference currents for the inner layer for maintaining capacitor voltages, while inner current control loop yields the required reference voltage for producing suitable driving pulses. For MMCC, due to sudden load changes, different losses of each H-bridge unit, measurement errors in voltage and current sensors, and tolerance of passive elements, the voltages of $dc-$link capacitors are unbalanced. In addition, under fault operation, the unbalanced power flow in each phase cluster of SSBC results in more divergence of capacitor voltages. Thus, ensuring the right voltage amplitude and balancing capacitors for SSBC STATCOM are fundamental and critical issues. Then, an additional control layer has to be implemented.

Different modulation techniques were proposed for MMCC which includes harmonics elimination PWM [20, 5, 21, 22, 23, 24, 25], space vector modulation [26], and multicarrier PWM modulations [17, 27, 28, 29, 30]. However, selection of the proper modulation techniques relies on their performance and ease of implementation. Phase shifted pulse width modulation (PS-PWM) is utilized due to its inherited capability of equal distribution of power and semiconductor stress among H-bridge units, easy to be implemented and perfectly suitable for the afore-discussed control scheme. However, performance of PS−PWM technique deteriorates under unbalance operation of the capacitors [27]. In [31], authors have investigated impact of switching harmonics on active power distribution and, accordingly, suggested selection of noninteger frequency modulation. Although it helps to alleviate phase-shifted angle errors between the carriers, the technique can not replace the individual balancing control [32, 33]. In unbalanced operation, an additional layer (i.e. cluster balancing) is required to equally share active power between the three phases [19].

Many works were conducted to balance capacitors voltages during fault operation and several methods were proposed which can be summarized as [34]: (1) independent clustered voltage control for each phase [19], (2) zero sequence injection control [35, 18], and (3) negative sequence injection control [34, 36]. The independent controllers are utilized to generate the required compensating voltage in phase with grid voltages which are then added to the outputs of the inner current control layer to produce suitable reference voltages for the modulation stage. However, the use of an isolated controller may result in control coupling with the inner current control layer [34]. Alternatively, a fundamental-frequency zero-sequence voltage (v_z) is added to the three-phase ac voltages of the SSBC converter. It can redistribute the active powers between the three clusters without drawing a negative sequence current. Since v_z only changes the virtual reference potential point of the SSBC, it does not affect the line to line voltages and correspondingly currents, thus it produces no effect on the total power [17]. The third category uses negative sequence injection control to fulfill the cluster balancing requirement. It has a higher regulation capability than the zero-sequence method due to controlling both negative-sequence voltage and current to redistribute the active powers among the phases. However, it limits the function of using negative-sequence current for other purposes such as current compensation under unbalanced load conditions.

In terms of the hierarchical control scheme, the majority of the works were dedicated to traditional linear control methods, eventually using P and PI controllers, however, since they are designed based on a linearized model, the system might lose its stability with external disturbance. In addition, tuning the controllers needs to be done for each design case separately. Several methods were proposed in the literature for the adaptive tuning of PI parameters. For instance, in [37] and [38] self-tuning PI controller based artificial neural networks and particle swarm optimization (PSO) techniques were proposed for the outer voltage control (AVC) of STATCOM. In [39, 40], dead-beat current control was applied for its high bandwidth and fast current tracking speed.

MMCC SSBC STATCOMs include a relevant number of cascaded cells resulting potential possibility of failure's occurrence which may lead to expensive downtime [41]. Therefore, assuring the continuous operation of STATCOM under partial faulty components is essential [42, 29]. Favourably, the modularity and redundancy characteristics of SSBC configuration allow the design of fault-tolerance control. Many methods have been proposed which can be categorized to hardware or software-based approaches [29, 42, 43, 44, 45, 46, 47, 48]. The main idea of all methods is to bypass the fault devices and to provide alternative patterns to maintain the operation of the system, either by the redundant design of the converter or by reconfiguring the system to operate according to the required current and voltage level. With the second approach, consideration during the design should be paid to allow fault-tolerant operation by giving a suitable design margin for related components (e.g. power switches, capacitors). In addition, in terms of control, the transition from different voltage levels due to the loss of the faulty units output voltage might affect the stability of the PI controllers. Thus, to guarantee the reliability of the operation the outer voltage control has been designed to provide enough phase margin in the fault-tolerant transition from the five-level to three-level operation [42].

Other methods that directly utilized nonlinear controllers to compensate system nonlinearities were introduced to increase robustness and performance. Among these controllers, model predictive control gains more interest to be used in multi-objective and nonlinear systems such as multilevel STATCOM. The main advantages of this

control include: (1) provide optimal control, (2) fast dynamic response, (3) easy inclusion of nonlinearities and constraints of the system, (4) simultaneous control of various variable, and (4) flexibility in adding more requirements and limitation to the control. There are some works presented in the literature on predictive control for multilevel STATCOM [40, 49, 50], however, computation time of the controllers is considerably high, and their stability is not guaranteed, hence impeding their implementation and adoption in the industrial world. On the other hand, exploiting Lyapunov's theory, a robust nonlinear controller can be designed since these controllers are designed based on large-signal nonlinear mathematical models. The complexity of such controllers depends on demanded objectives, model order size, and simplified assumptions [51].

In a normal STATCOM, a capacitor bank is used to maintain the dc voltage of the VSI. For SSBC, the number of capacitors is proportional to the number of synthesized levels. Due to sudden load changes, different losses of each H-bridge unit, measurement errors in voltage and current sensors, and tolerance of passive elements, the voltages of $dc-$link capacitors are unbalanced. In addition, under fault operation, the unbalanced real power within the converter phases of SSBC results in more divergence of capacitor voltages and failure of the control system which affects the safety of the devices or leads to serious system collapse [30]. Thus, ensuring the capacitor voltages balancing for SSBC-STATCOM is a fundamental and critical issue. Generally, the cluster balancing layer is utilized to achieve this control objective. Several methods were introduced in the literature which can be categorized into independent clustered voltage control for each phase, zero sequence injection control, and negative sequence injection control [18, 19, 34, 35, 36].

In the first category, the independent controllers are utilized to generate the required compensating voltage in phase with grid voltages which then added to the outputs of the inner current control layer to produce suitable reference voltages for the modulation stage. The use of an isolated controller may result in control coupling with the inner current control layer [34]. In the second category, a fundamental-frequency zero-sequence voltage (v_z) is added to the three-phase ac voltages of the SSBC converter. It can redistribute the active powers between the three clusters

without drawing a negative sequence current. Since v_z only changes the virtual reference potential point of the SSBC, it does not affect the line to line voltages and correspondingly currents, thus it produces no effect to the total power [17]. Under large cluster voltage imbalance, this method has a limited regulation capability. The third category uses negative sequence injection control to fulfil the cluster balancing requirement. It has a higher regulation capability than the zero-sequence method due to controlling both negative-sequence voltage and current to redistribute the active powers among the phases. However, it limits the function of using negative-sequence current for other purposes such as current compensation under unbalanced load conditions.

A relevant problem that affects the harmonics performance of STATCOM is the low-switching frequency oscillations that appear across capacitor voltage. These oscillations produce third harmonic components in the output voltages of STATCOM which deteriorate overall performance. Recently, some works propose a reduction of capacitor size in STATCOM [14, 52], which indicates higher ripple if not properly controlled.

Correspondingly, this work is dedicated to the design and control implementation of Single-Star Bridge-Cell (SSBC) based STATCOM using FPGA and DSP. A study of the optimal selection of the number is conducted to figure out its impact on the design and cost of the system. Single Star Bridge Cell topology with four H-bridge converter units in each phase is selected for the work. For improving the stability of the system, a backstepping control design is proposed. Besides, a study of the system's operation under unbalance conditions is presented. For validation, 142 V 9-level SSBC STATCOM set-up is used.

1.2 Research Motivation and Objectives

With more installation of electronic loads and distributed renewable energy sources, static compensators gain more interest to encounter the resulting power quality issues in low and medium voltage grids. The commercial deployment of high power semiconductors devices (such as Insulated Gate Bipolar Transistors, IGBTs) enables the development of STATCOM systems. The technology platform utilizes the two-level inverters, eventually with bulky step-up transformer for medium and

high voltage systems. However, due to the low harmonics performance and the requirement for bulky filtering, the multilevel converters topologies become more attractive. Different topologies have been introduced during the last few decades and among the others, the Single-Star bridge cell is well applied to this application for its satisfactory performance and superior component count. Direct connection to medium voltage range without transformers brings outstanding advantages in terms of cost and performance. The footprint of STATCOM installation utilizing SSBC topology is smaller than a conventional SVC installation of the same rating. The technology offers great flexibility regarding the design and layout of converters and substations. The modularity concept of this topology enables high prefabrication and in-factory testing, bringing to an overall reduction of project lead-time and enhancement of product quality while scalability allows easy adaptation of the system to different voltage levels. To cope with these requirements, commonly, a modular control approach with phase-shifted pulse width modulation (PS-PWM) is utilized.

The feasibility of adoption of STATCOMs for low and medium voltage systems relies strictly on their performance and cost-effectiveness. Theoretically, the harmonics performance improves with increasing the number of levels. However, this has a direct effect on their design and hence on their overall complexity and cost. In addition, for SSBC STATCOM, when the number of levels increases, more switches are required to be parallelly controlled. Therefore, software-based microcontrollers (e.g. DSPs) show limitations in terms of I/O built-in pins as well as performance. Alternatively, field programmable gate arrays (FPGAs), with their parallelism capability, are suitable for implementing control of SSBC-STATCOM. Multilevel SSBC-STATCOM control, as shown in Fig. 1.3, is composed of three layers which are output voltage control layer, internal current control layer, and capacitor voltage balancing layer. A *dq* control based on PI regulators is commonly used for its simplicity and ease in implementation. Although PI regulators are commonly used for its simplicity and ease in the implementation, the STATCOM system is essentially nonlinear, therefore, a nonlinear controller can effectively improve performance and robustness. Besides, the performance of multilevel single-star bridge-cell (SSBC) STATCOM is affected by the low-frequency oscillation in the dc capacitors' voltages which is originated due to the double line frequency component on the absorbed active power. To avoid using big capacitors to limit this oscillation.

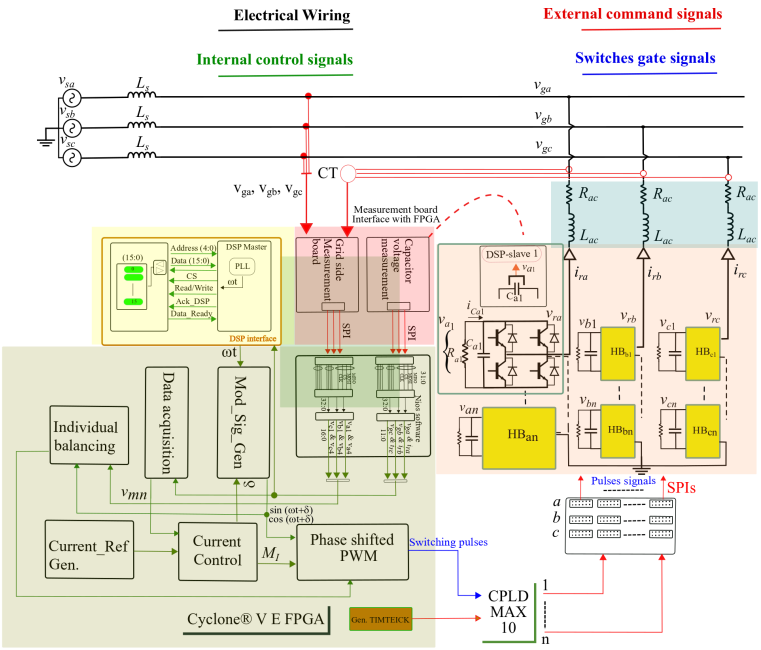


Figure 1.3: Control implementation of SSBC STATCOM

Therefore, this work is focused on the application of MMCC-SSBC topology for STATCOM considering all aspects of the system and control design and implementation. By considering the aforementioned background, the objectives of this research are formulated as follows:

1. to investigates some key factors in STATCOM design with emphasis on their impact on the overall cost in low and medium voltage applications.
2. to design the control of SSBC STATCOM and implement it using Cyclone® V FPGA.
3. to propose a backstepping nonlinear control based on Lyapunov function design for improving the stability of 9-level SSBC STATCOM.
4. to verify the results experimentally using 9-level SSBC STATCOM Hardware set-up (as shown in Fig. 1.4).
5. to investigate the performance of STATCOM under unbalanced operation.

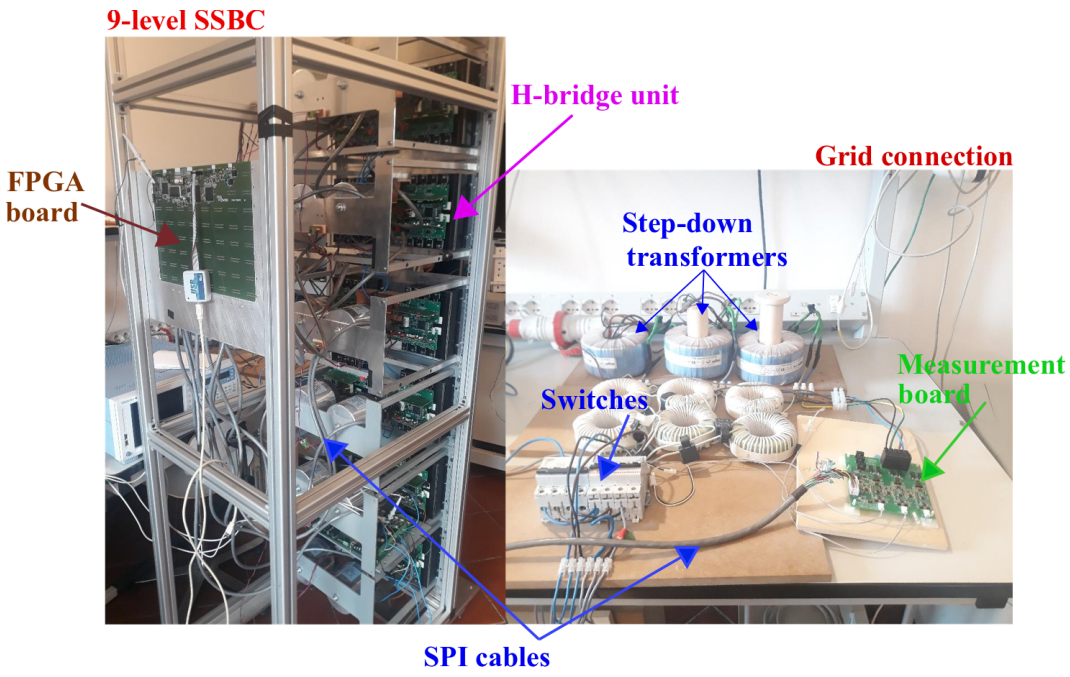


Figure 1.4: Hardware set-up of 9-level SSBC STATCOM

Matlab/Simulink is used for developing the 9-level STATCOM model to verify the performance of all control in this work before conducting the experimental results. A control board specifically designed to control Modular Multilevel Converter and employing Intel Cyclone® V FPGA, a MAX10 C-PLD, and a Texas Instruments DSP 320F28377S, produced by DigiPower [53], is used to implement the STATCOM control.

1.3 Scope of the Research

The scope and limitations of this research are as follows:

1. The SSBC STATCOM connection using three single phase step-up transformers.

   The laboratory test of the SSBC STATCOM was performed under the use of step-up transformer for isolation and reducing the voltage level of the point of common coupling. This was considered to avoid any hazard for the individuals and the system. As the final product of STATCOM should incorporate protection units. In this work, the protection was not considered due to the limitation of time and resources.

2. Simulation using Simulink/Matlab.

   To validate the effectiveness of the proposed control scheme, STATCOM is modeled in Simulink/Matlab. This step is an important step for fast and successful final implementation of the control in the real system.

3. Testing under grid faults is supported with simulation results.

   In this work, the operation of the SSBC STATCOM under grid faults has been investigated under cluster balancing control. The results are supported in simulation. The hardware implementation under this case is out of the scope of the work due to the shortage of resources.

1.4 Significance of the Work

The advantages of the proposed work on SSBC STATCOM can be summarized as:

1. Reduction in the size and cost of the STATCOM using multilevel converter technology.

   This work presents a STATCOM based on 9-level SSBC which allows the elimination of the bulky and costly step-up transformer which, for industrial application, is used to connect the STATCOM to distribution and transmission levels. Besides, due to the good harmonics performance of the output voltage of the proposed STATCOM, a smaller series-coupling inductor can be used, hence the lower size and cost of the overall system.

2. Impact of number of levels on the design and cost of SSBC STATCOM.

   The feasibility of adoption of static compensators for low and medium voltage systems relies strictly on their performance and cost-effectiveness. Theoretically, the harmonics performance improves with increasing the number of levels. However, this has a direct effect on their design and hence on their overall complexity and cost. The work tries to disclose the relationship between the STATCOM implementation cost and the number of levels in both low and medium voltage systems.

3. Fast reactive power compensation due to the adoption of direct control based structure.

The utilization of direct control scheme instead of the indirect control scheme allows for fast compensation of the reactive power. The control of reactive power is achieved by using PS-PWM switching to vary the amplitude of the SSBC output voltage by varying the modulation index (M_I) values.

4. Enhance stability and robustness of SSBC STATCOM control.

   Multilevel SSBC-STATCOM control is composed of three layers which are output voltage control, internal current control, and capacitor voltage balancing. Although PI regulators are commonly used for its simplicity and ease in implementation, STATCOM system is an essentially nonlinear system, therefore, a nonlinear controller can effectively improve performance and robustness. Therefore, in this work, a backstepping nonlinear control based on Lyapunov function design is proposed to regulate the overall capacitor voltage. It achieves an efficient and satisfactory performance of the $dc-$link voltage regulation (DVC) via systematic and recursive design methodology while maintaining the hierarchical control approach. In addition, it proves its viability to improve the stability of system under system impedance variation and during fault-tolerance operation. hence enhancing both system reliability and availability.

5. Control implementation using field programmable gate array (FPGA).

   A higher number of levels in SSBC STATCOM increase modulation complexity due to the higher number of switches that need to be controlled. For the digital implementation of the system control, digital signal processors (DSPs) and field-programmable gate arrays (FPGAs) are preferred options. However, due to the limitation of I/O built-in pins in typical DSPs, FPGAs are becoming dominant to be used for pulse modulation in MMCC based systems [54, 55, 56, 57]. Therefore, in addition to the achieved cost reduction from the easy configuration of FPGA hardware resources for specific applications, a dramatic reduction of execution time can be achieved due to the potential parallelism offered by FPGAs, hence significant performance is obtained compared to software-based processors. Besides, due to the modularity feature in the FPGA design, it is very suitable for the proposed layers control structure of the SSBC STATCOM. This is also advantageous for extending the designed control for higher levels.

This work describes an implementation methodology for 9-level SSBC based STATCOM using FPGA in which Cyclone® V (5CEBA7F31C7) is used for the implementation of the control blocks while the phase-locked loop (PLL) is built on DSP for synchronization of STATCOM output with the grid.

1.5 Thesis Outline

The thesis is comprised of six chapters. The remaining chapters are organized as follows:

- **Chapter 2:** Overview of Multilevel Converters for STATCOM

  In this chapter, a review of the topologies, control, and modulation methods used for STATCOM is made. It provides important background knowledge regarding the research. The chapter starts by comparing the STATCOM to the other types of FACTS devices. Then, the MVSI topologies, control strategies, and modulation techniques utilized for STATCOM are presented alongside a comparative analysis between them. It points out the superiority of SSBC against others when STATCOM is considered. Furthermore, PWM methods used for the direct control of STATCOM are presented alongside a critical discussion. In the end, the discussion is given to the operation of STATCOM under unbalance operation considering the balancing techniques for both harmonics elimination PWM and phase-shifted PWM methods.

- **Chapter 3:** Design and Analysis of SSBC based STATCOM

  SSBC topology is most suitable for STATCOM application for its satisfactory performance and superior component count. Generally, the feasibility of adopting static compensators for low and medium voltage systems strictly relies on their performance and cost-effectiveness. Theoretically, the performance of the harmonic improves with increasing the number of levels. However, this has a direct effect on their design and hence on their overall complexity and cost. Thus, in this chapter, some key factors in STATCOM design are investigated, with emphasis on their impact on the overall cost in low and medium voltage applications.

- **Chapter 4:** Control Design and Implementation of SSBC based STATCOM

Multilevel Single-Star Bridge-Cell STATCOM control is usually accomplished with three layers which are output voltage control, internal current control, and capacitor voltage balancing. In this chapter, a backstepping nonlinear control based on Lyapunov function design is proposed to regulate the overall capacitor voltage. Besides, detailed control design and implementation of the proposed control of SSBC-STATCOM using FPGA is discussed. Experimental set-up was designed to verify the results practically which confirmed the robustness and stability of the proposed control approach. In addition, the performance of the proposed method under V_{dc} step change and variation of system impedance has been analyzed and results were compared with the traditional PI controller. Besides, simulation results is presented to demonstrate the advantage of the proposed control for post-fault operation, which will enhance both system reliability and availability.

- **Chapter 5:** Operation of SSBC-STATCOM under Unbalanced Conditions

  This chapter focuses on cluster balancing control for the unbalanced operation of SSBC STATCOM. Zero-sequence voltage (v_z) injection is utilized to maintain the mean *dc* capacitors voltages balanced under faults. It can redistribute the active powers between the three clusters without drawing a negative sequence current. Since v_z only changes the virtual reference potential point of the SSBC, it does not affect the line to line voltages and correspondingly currents, thus it produces no effect on the total power. Analysis and modeling of cluster balancing control with a low-pass filter and moving average filter are presented. Besides, extensive simulation is carried out to verify the performance of control for zero-voltage ride-through performance.

- **Chapter 6:** Conclusion and Future Work

  This chapter concludes the work and provides a suggestions and directions for the future work.

CHAPTER 2

OVERVIEW OF MULTILEVEL CONVERTERS FOR STATCOM

2.1 Introduction

In this chapter, an overview of FACTS devices is presented. In addition, a detailed literature review about STATCOM is covered. The topics covered include; inverter topologies, control and modulation techniques. The chapter also provides a comparison between the available MVSI topologies and points out the superiority of SSBC topology against others when STATCOM is considered. Furthermore, common PWM methods that are used for the direct control of STATCOM are presented alongside a critical discussion between them. In the end, the discussion is given to the operation of STATCOM under unbalance operation considering the balancing techniques for both harmonics elimination PWM and phase-shifted PWM methods.

2.2 Overview about FACTS Devices

With the ongoing expansion and growth of the electric utility industry including deregulation in many countries, the generation and transmission systems are being pushed closer to their stability and thermal limits [10, 58]. Meanwhile, the focus on the quality of power distribution has gained significant attention. In addition, the environmental impacts play a major role in the decision-making at all levels of power systems investment. Reformation in the power system can be grouped into three major sectors: 1) optimization of the existing established transmission system (TS), 2) utilization of DER and 3) deployment of new technologies. Notwithstanding the advantages that it offers, the interconnection of unstable renewable energy sources and the proliferation of various kinds of loads have imposed serious power quality (PQ) problems to the electrical grid. These problems can be mitigated or attenuated by adequate compensation of reactive power.

Traditionally, electro-mechanical technologies (i.e. phase shifting transformers, transformer tap changers and passive reactive compensators) or rotating synchronous

condensers are used for reactive power compensation. Despite its simplicity, in fast fluctuating operation conditions, they are highly prone to fail [59]. The rapid development of the semiconductor devices and power electronics have opened up opportunities to improve power system networks via flexible AC transmission system (FACTS) controllers [60]. These controllers, which are commonly referred to as compensators, have been defined by the IEEE [61] as a *"power electronic based system and other static equipment that provide control of one or more ac transmission system parameters to enhance controllability and increase power transfer capability"*. Since their introduction in the 1970s [60], FACTS devices have been used in the control of power flow, voltage and frequency which yield an increase of transmission capacity, and controllability. They also facilitate the integration of more DER into the grid.

Component-wise, FACTS can be grouped based on the availability of the power semiconductor switches. The two groups have distinctly different operation and performance characteristics. The first generation employs conventional thyristor-switched capacitors and reactors, in addition to the quadrature tap-changing transformers. With proper coordination of the reactor control and capacitor switching, they can be used for reactive compensation in the capacitive and inductive modes. However, due to the use of passive components, they are bulky in size. After this generation, the thyristor-controlled phase shifter (TCPS), thyristor-controlled series capacitor (TCSC) and static VAr compensator (SVC) have been developed. The second generation of FACTS employs more sophisticated power electronics converters, such as voltage source converters (VSC) and current source converters (CSC). The static synchronous series compensator (SSSC), static synchronous compensator (STATCOM) and unified power flow controller (UPFC) are the common devices listed under the second generation.

Modern FACTS controllers are classified based on the way of connection [60, 10]; they are broadly categorized into three categories:

1. The series type compensators such as the dynamic voltage restorer (DVR) and the static synchronous series compensator (SSSC).

2. Shunt type compensators such as static VAr compensator (SVC) and static synchronous compensator (STATCOM).

3. Combined series-shunt (hybrid) compensators such as unified power flow controller (UPFC).

2.3 Reactive Power Compensation Principle

In a linear circuit, reactive power is defined as the ac component of the instantaneous power with frequency equals to $2\omega t$. The generated reactive power from the source is stored in a capacitor or a reactor during a quarter of the cycle, and sent back to the power source in the following quarter. In other words, it oscillates between the ac source and the reactive components, and between these components, at double rated frequency. Therefore, to avoid the VAr circulation between loads and source, it can be compensated using reactive generators which improve the voltage stability of the power system. These generators can be connected in parallel or in series; the principles of both are described in the following subsections.

2.3.1 Series-Connected Compensators

Transmission lines have inductive reactances which can be reduced by connecting capacitors in series with the lines. Consequently, functionality of the power system is improved through: 1) increased angular stability which means reducing risk that generators and other synchronous machines lose synchronism in the event of a serious short-circuit, 2) improved grid voltage stability, 3) optimized power-sharing between parallel circuits and 4) increased transmission capability.

Thus, typical series compensators consist of capacitors to lower the equivalent reactance of the power line X_L (in 2.1) at rated frequency for balancing part of line's reactance.

$$P_{12} = \frac{V_1 V_2 \sin \delta}{X_L} \tag{2.1}$$

where V_1 and V_2 are the bus voltage magnitudes at the sending and receiving ends, δ is the voltage phase difference. If we assume the effective line impedance is given be

$$X_{eff} = X_L - X_C = (1 - \kappa)\, X \tag{2.2}$$

where k represents the degree of series compensation given that

$$\kappa = \frac{X_C}{X_L}, \qquad 0 \leq \kappa < 1 \tag{2.3}$$

Accordingly, with assumption that $V_1 = V_2 = V$, the real power considering series compensator can be derived in the following form:

$$P_{12} = \frac{V^2 \sin\delta}{(1 - \kappa)\, X} \tag{2.4}$$

and the reactive power supplied by the series compensator can be expressed as

$$Q_C = I^2 X_C = \frac{V^2}{X} \frac{\kappa}{(1 - \kappa)^2} (1 - \cos\delta) \tag{2.5}$$

To demonstrate the effectivenss of series compensation, the relationship between real power (2.4), series capacitive reactive power (2.5) and power angle (δ) is plotted at various values of the degree of series compensation (i.e. κ). As shown in Fig. 2.1, increasing the value of degree of compensation results in more transmittable real power. It is also demonstrate that, reactive power sharply increases with higher values of κ. Therefore, the physical explanation, that impedance of the series compensation cancels portion of the line impedance the effective transmission impedance is reduced, is valid to understand the power converters based compensators. Generally, to increase

the flowing current in the transmission line (consequently the transmittable power) voltage across the line impedance must be increased which can be accomplished by an appropriate series circuit element which can be envisioned as an ac voltage source which directly control the desired compensating voltage that required to be connected with the line. The physical nature of the series circuit is irrlevant as low as it is capable to produce the related voltage.

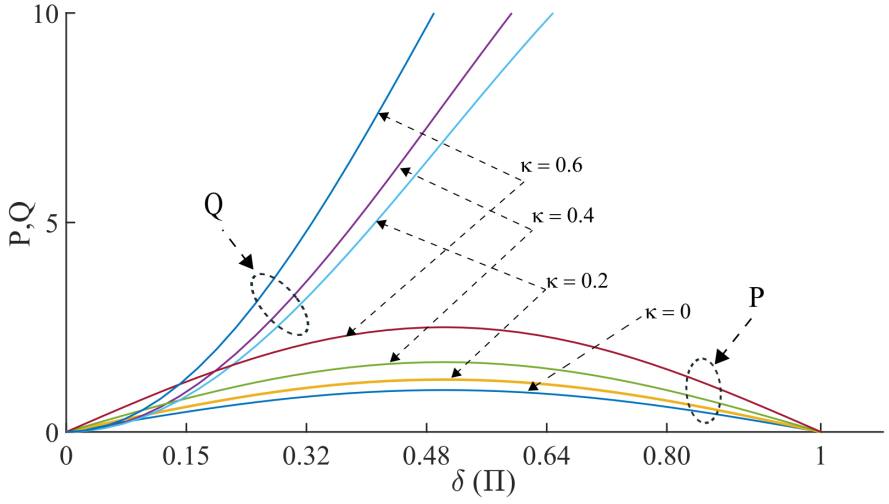


Figure 2.1: Real power and series capacitive power vs power angle characteristics

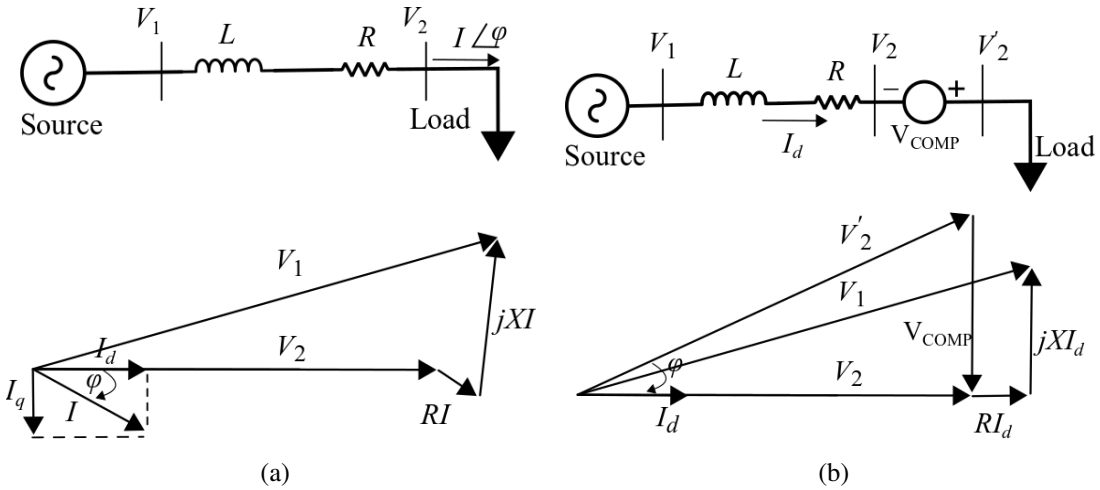


Figure 2.2: Operation principle of series-connected compensators (a) without compensator (b) with compensator

Series compensators can be implemented with current- or voltage- source devices. Fig. 2.2 describes the operation principle of series-type compensators where it can be envisioned as a voltage source inserted in series with the power system line to obtain a unity power factor operation at V_2. In this case, V_{COMP} is added between the line and the load to control $V_2^{'}$ angle. It generates a voltage with opposite direction to the voltage drop across the line inductance

A controlled variable impedance can be obtained by using series-connected FACTS controllers such as the Thyristor-Controlled Seried Capacitor (TCSC) and Static Synchronous Series Compensator (SSSC). This gives the advantage of power flow control and power oscillation damping that cannot be achieved using uncontrolled compensation. Fig. 2.3 shows the schematics of the available series-connected reactive power compensators.

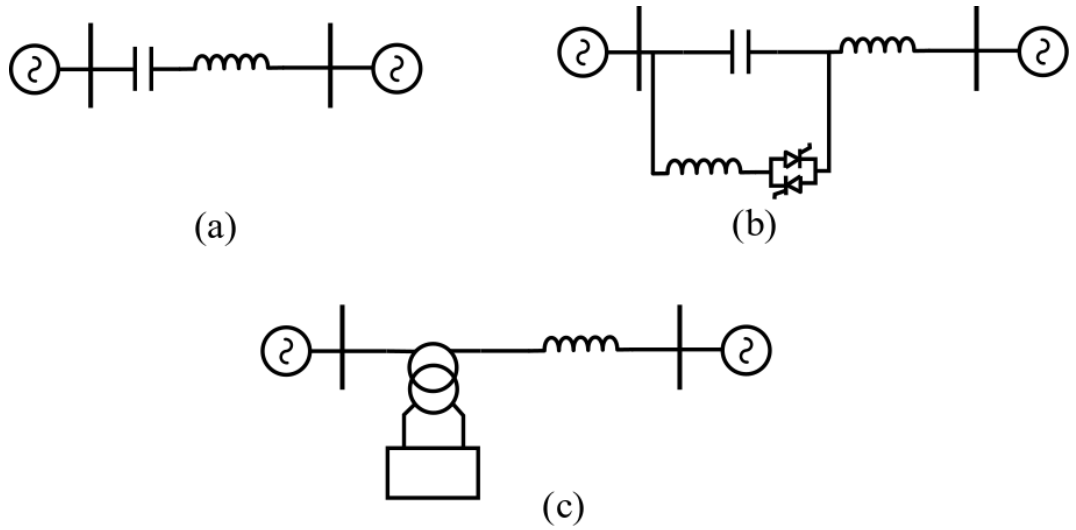


Figure 2.3: Series-structure of reactive power compensators (a) fixed series capacitor (b) Thyristor controlled series capacitor (c) static synchronous series capacitor (SSSC)[4]

To increase power flow and consequently the transfer capacity of a meshed transmission, subtransmission, and distribution network, The concept of distribution FACTS (D-FACTS) [62, 4] presents high potential (shown in Fig. 2.4) . In a meshed Transmission and Distribution network, the power transfer capacity of the system is

constricted by the first line that reaches the thermal limit. The inability to effectively control power flow in such a network results in significant underutilization of the overall system. D-FACTS devices offer the ability to improve the transfer capacity and grid utilization by routing power flow from overloaded lines to underutilized parts of the network. Capacitive compensation on underutilized lines would make them more receptive to the inflow of the current, while inductive compensation on overloaded lines would make them less attractive to current flow. In both cases, the throughput of the system is increased by diverting additional power flow from the congested parts of the network to the lines with available capacity.

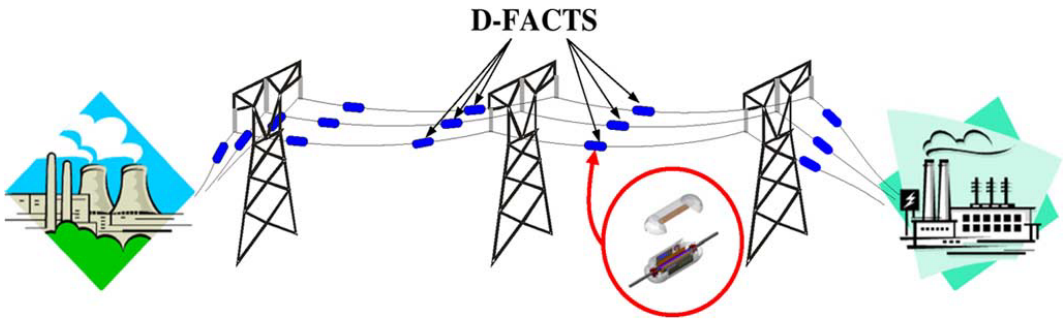


Figure 2.4: Distribution FACTS [4]

2.3.2 Shunt-Connected Compensators

In the previous section, it has been confirmed that the reactive power compensation is effective in increasing the steady-state transmittable power and voltage profile. Similar to series-type, shunt compensators have the capability to change the natural electrical characterisitcs of the transmission line to make it more compatible with the prevailing load demand. Thus, shunt-compensators, fixed or mechanically switched reactors/capacitors are conventionally used to maintain line voltage under

fluctuating load conditions. This section provides the fundamental concept of reactive power compensation using shunt devices.

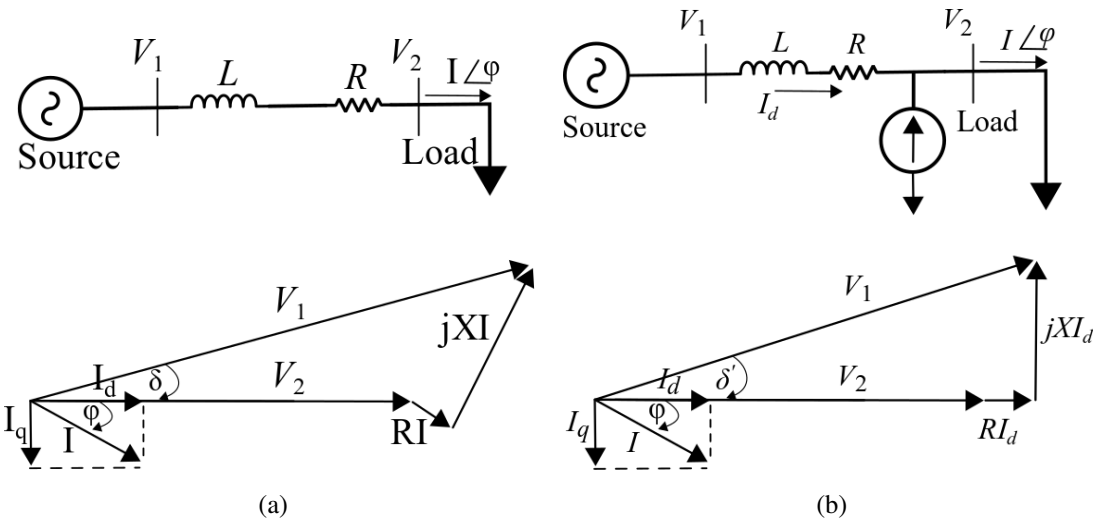


Figure 2.5: Operation principle of shunt-connected compensators (a) without compensator (b) with compensator

Fig. 2.5 shows the principles and theoretical effects of shunt reactive power compensation in a basic *ac* system, which comprises a source, a power line, and a typical inductive load. Fig. 2.5a shows the system without compensation and its associated phasor diagram. In the phasor diagram, the phase angle of the current has been related to the load side, which means that the active current is in phase with the load voltage . Since the load is assumed inductive, it requires reactive power for proper operation and hence, the source must supply it, increasing the current from the generator and through power lines. If reactive power is supplied near the load, the line current can be reduced or minimized, reducing power losses and improving voltage regulation at the load terminals. This can be done in three ways: 1) with a capacitor; 2) with a voltage source; or 3) with a current source. In Fig. 2.5b, a current-source device is being used to compensate the reactive component of the load current . As a result, the system voltage regulation is improved and the reactive current component from the source is reduced or almost eliminated. If the load needs leading compensation, then an inductor would be required. Also, a current source or a voltage source can be used for

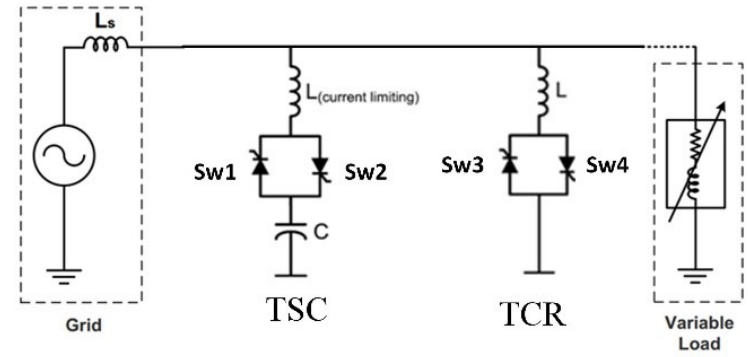
inductive shunt compensation. The main advantage of using voltage- or current-source Var generators (instead of inductors or capacitors) is that the reactive power generated is independent of the voltage at the point of connection.

Shunt compensation is commonly used to maintain the voltage at various connection points of the transmission system. This helps to increase the transmittable power and hence improve system stability. Depending on the system loading, the voltage profile along the transmission line can be controlled using controlled compensation by shunt-connected FACTS controllers such as Thyristor-Controlled Reactor (TCR), Static Var Compensator (SVC), and Static Synchronous Compensator (STATCOM).

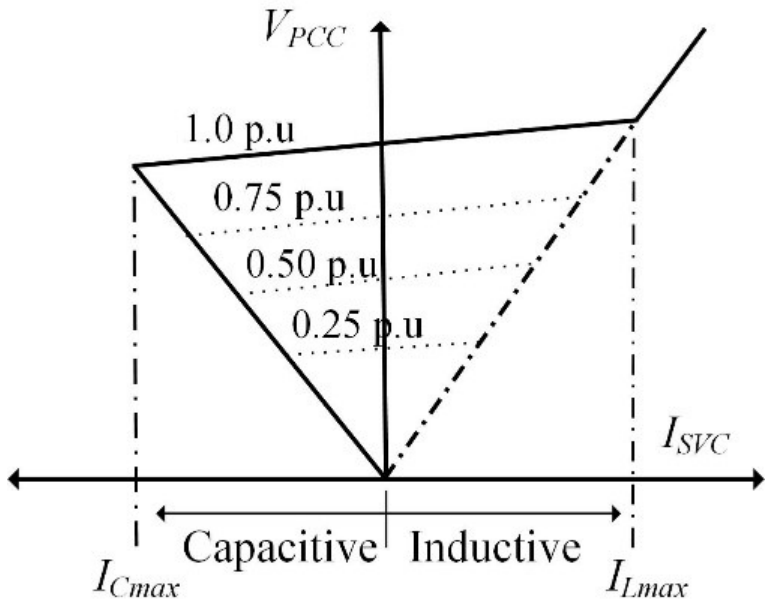
2.4 Static VAr Compensator

The main role of the static VAr compensator (SVC) is to adjust the reactive power according to the system needs and consequently control the bus voltage. In the earlier days, SVCs are built using thyristors. Among the first applications of the SVC, was the EPRI-Minnesota Power & Light in 1974 and Westinghouse project commissioned in 1975, in which SVCs enabled a 25% power increase along the line where they were installed [60]. From then, the number of SVC installations is increasing steadily.

Basically, SVCs consist of power switches that are used to control passive shunt components, i.e. inductor and/or capacitor. Two main SVC devices, namely the thyristor switched capacitor (TSC) and the thyristor controlled reactor (TCR) [10] are shown in Fig. 2.6a. In the TSC configuration, the connection between the capacitor and the grid is controlled by two back-to-back connected thyristors (Sw1 and Sw2). The reactive power flow is achieved by firing or blocking the thyristors accordingly, which consequently causes the capacitor to be fully connected or disconnected. On the other hand, the TCR control is achieved by introducing a delay angle between the firing signal of thyristors (Sw3 and Sw4) and the line-to-line voltage. The reactive power can be varied by holding the delay angle between 90º and 180º.



(a)



(b)

Figure 2.6: (a) Single line diagram of SVCs basic configurations, (b) SVC's V-I characteristics

Using these two configurations, the magnitude of reactive power can be controlled at a desired value in the capacitive and inductive modes. However, the capacity of these controllers is limited by the line voltage, as the reactive power is directly affected by the square value of voltage magnitude [10]. Because the capacity of SVC needs to be de-rated, the controller might experience saturation condition. Consequently, the response time is prolonged [63] , i.e. between 0.5 to 2 cycle [10].

Typical V-I characteristics of SVC is given in Fig. 2.6b. It shows the relationship between the SVC reactive current (I_{SVC}) and the applied voltage (V_{PCC}). Note that the capability of SVC is degraded under lower voltage. Thus, any reduction in voltage magnitude results in diminishing the reactive power compensation capability of SVC.

2.5 Static Synchronous Compensator

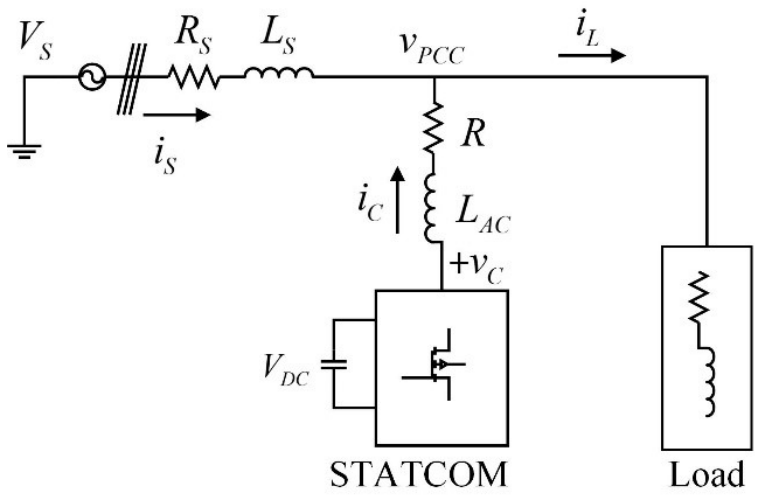
The limitations of SVC, namely bulky, high installation cost and slow response time are overcome by the application of the static synchronous compensator (STATCOM) [63, 10]. In one sense, the STATCOM can be considered as an advancement of the SVC systems. Instead of using passive components in SVC, STATCOM generates a controllable reactive power directly using power inverters. STATCOM is also known as the static condenser (STATCON), advanced SVC (ASVC), GTO-SVC or static VAr generator (SVG) [60].

In principle, the desired reactive power compensation is provided in a similar way to the SVC. However, instead of using the capacitor and reactor components, it utilizes a voltage source inverter (VSI). By a proper modulation of the VSI output voltage, the STATCOM's voltage and current waveforms are altered simultaneously. Doing so allows the reactive power exchange with the grid. The basic line diagram of D-STATCOM is presented in Fig. 2.7a.

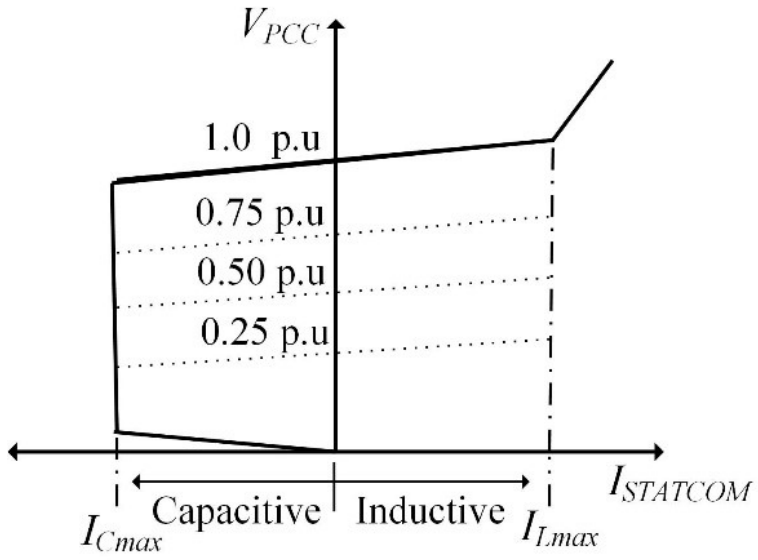
Unlike the SVC, the STATCOMs can provide full capacitive reactive current independently, up to 0.15 p.u. of the system voltage. This is illustrated in Fig. 2.7b. Thus, it offers a voltage support and transient stability margin at lower voltage level. In addition, the replacement of bulky inductors and capacitors with VSI allows for the STATCOM size to be reduced and this makes the system more stable with respect to the variations in system impedances [10].

STATCOM devices can be classified into either transmission (T-STATCOM) or distribution (D-STATCOM) types. This classification is based on its connectivity to the source. If the connection is made to the high or extra-high voltage (HV or EHV), the system is called T-STATCOM. On the other hand, medium voltage (MV) requires a D-STATCOM. For T-STATCOM, the connectivity to the transmission level is via

a step up transformer, while it is possible to operate D-STATCOM without using the transformers. Normally, the STATCOM is installed in the distribution or transmission lines to perform the following functions: voltage regulation, reactive power control in overhead or load lines, flicker mitigation and stability improvements [22, 64, 65].



(a)



(b)

Figure 2.7: (a) Single line diagram of SVCs basic configurations, (b) SVC's V-I characteristics

2.5.1 Power Exchange in D-STATCOM

The D-STATCOM is a distribution network compensator device connected in parallel at the point of common coupling (PCC). A single line diagram of a typical connection of D-STATCOM to the power source is shown in Fig. 2.8. The main building block of the D-STATCOM is the VSI. It converts the dc input voltage to a balanced 3-phase voltage with controllable magnitude and phase angle [10]. The VSI is connected to the line through a (series) coupling inductor L_{AC}. The voltage difference across L_{AC} creates the reactive power (Q) exchange between the D-STATCOM and the grid system. In the inductive mode operation, the D-STATCOM absorbs Q by making $V_C < V_{PCC}$. During the capacitive mode, where $V_C > V_{PCC}$, the flow of Q is reversed.

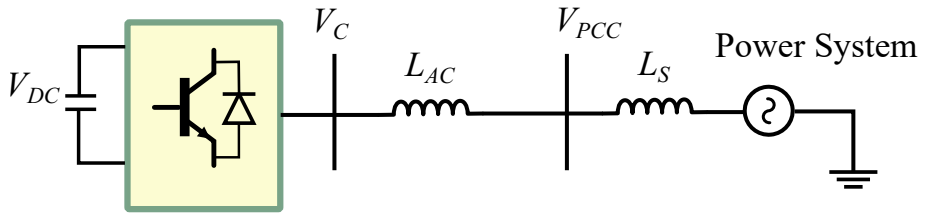


Figure 2.8: Single line diagram of D-STATCOM.

The exchange of active power (P) and Q between the D-STATCOM and the line are governed by;

$$P = \frac{V_{PCC}V_C}{X_{AC}} \sin\delta \tag{2.6}$$

$$Q = \frac{V_{PCC}}{X_{AC}} (V_{PCC} - V_C) \tag{2.7}$$

The active power compensates for the dc voltage decrease across the capacitors (V_{DC}) due to the losses. Furthermore, from (2.7), it is expected that Q exchange can be obtained by properly controlling of the output voltage of the VSI (V_C). In a close loop

system, the variation of V_C is achieved by adjusting the value of M_I. Fig. 2.9 illustrates the phasor diagram of active and reactive power exchange between the D-STATCOM and the grid in the 4−quadrants of $P - Q$ plane [65]. It reveals the two control laws of D-STATCOM:

1. For reactive power exchange, the output voltage (V_C) is controlled to allow the compensation in capacitive and inductive modes as illustrated in quadrants I & II and quadrants III & IV accordingly.
2. For active power exchange, the phase angle between STATCOM's output voltage and the voltage at PCC is adjusted to allow the exchange of active power in capacitive and inductive modes as shown in I & IV and II & III respectively.

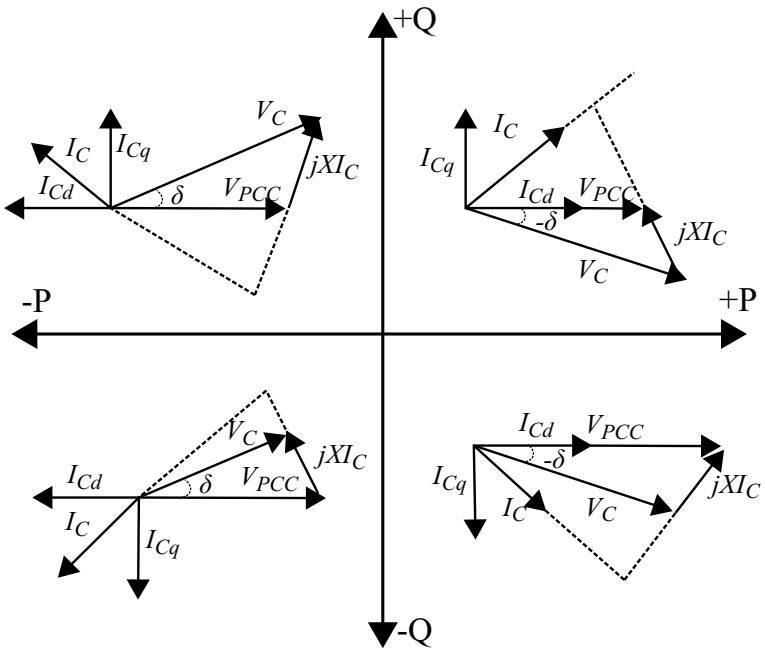


Figure 2.9: Phasor diagram for power exchange in D-STATCOM

2.6 Multilevel Converters for STATCOM

Since the 1980s, STATCOMs have been increasingly used at a higher voltage level, i.e. in transmission [66], high voltage distribution [7, 67, 22] and energy utilization. Traditionally, the two levels voltage source inverter (VSI) (i.e. Fi.g 2.10)

with a series transformer form the main building block of the D-STATCOM. The main objective of using a VSI is to utilize the input dc voltage to synthesize ac output waveform. By proper modulation of VSI output voltage, the output current changes simultaneously; thus, the dynamic exchange of active and reactive power between the STATCOM and the utility grid is attained [60]. The popularity of VSI is due to its simplicity and low cost. However, its output voltage is characterized by high harmonics contents, which require bulky and costly filtering. Furthermore, it is mandatory to use step-up transformers to allow the connection of the VSI to high and medium voltage level. This increases the cost, size, weight and losses of the overall system [68]. In addition, such transformers are usually bulky and expensive; they occupy more space and produce high losses.

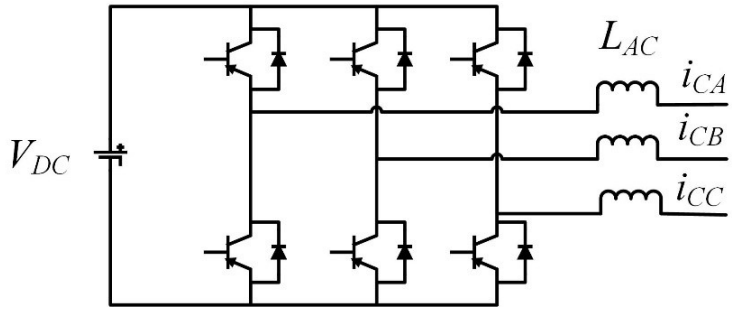


Figure 2.10: Two level VSI topology

The multilevel VSI (MVSI), [69, 2, 70, 71], are being exploited to replace the conventional VSI for D-STATCOM applications. Since the MVSI is capable of providing sufficiently high voltage, the bulky, lossy and costly step-up transformer can be avoided [72, 73, 21]. For instance, with the absence of the line frequency (50 Hz) transformer, the weight of a 3-phase cascaded MVSI at 6.6 kV/1 MVA rating is reduced by three to four times [74, 73]. Furthermore,[74, 73], reported that for a 360 kVA D-STATCOM, weight is about half of the overall system size, while [75] noted that approximately 70% of the total loss per MVA rating is due to the transformers.

In addition, implementation of MVSI in D-STATCOM [76] allows the utilization of much lower rated semiconductor switches for high voltage generation.

For example, a medium voltage (11 kV) converter can be constructed using a 23 level MVSI, in which each level contributes a voltage of 1 kV. In this case, an IGBT switch rated at 1.5-2 kV is adequate to realize the converter. In addition, the stepped output nature of MVSI not only reduces the stress on the switching devices, it also improves the frequency spectra profile resulting in lower harmonics distortion. In theory, the number of level for MVSI is infinite, but for practical purposes, it is limited by the complexity of the circuit. The minimum number of level to be considered as a MVSI is three, i.e. $-V, 0$ and $+V$. Over the years, various MVSI topologies have been proposed for D-STATCOM: among others, the diode-clamped, flying-capacitor and modular cascaded converters are the most popular [77, 76, 2, 17]. The main features of each topology are summarized in the following subsections.

2.6.1 Comparison of MVSI Topologies

Table 2.1 summarizes the number of components required to produce N phase voltage levels of MVSI [78]. Even though the number of the main components are the same in the three configurations, the overall number of components is different. For diode-clamped MVSI, clamping diodes per phase are needed to produce N voltage level. For STATCOM, this increases the cost and causes packaging problems. In addition, special control is needed to balance the voltages across the capacitors. Thus, practical applications of diode-clamped MVSI topology are limited to five levels. For flying-capacitor MVSI, a number of flying capacitors is needed per phase to construct N per phase levels. Consequently, high switching frequency and complex control are necessary to balance the voltages across the capacitor. For high voltage utility applications, a large number of capacitors is needed.

Table 2.1: Comparison of component number requirement per phase voltage level among MVSI topologies

MVSI topology/Component count	**Diode-clamped**	**Flying-capacitor**	**Cascaded H-bridge**
power switches	$2 \times (N-1)$	$2 \times (N-1)$	$2 \times (N-1)$
main diodes	$2 \times (N-1)$	$2 \times (N-1)$	$2 \times (N-1)$
clamping diodes	$(N-1)(N-2)$	–	–
dc-input capacitors	$(N-1)$	$(N-1)$	$(N-1)/2$
balancing capacitors	–	$(N-1)(N-2)\ /2$	–
Total number of components	$N^2 + (2N) - 3$	$\left(N^2 + (8N) - 8\right)/2$	$9/2\,(N-1)$

Unlike the diode-clamped and flying-capacitor topologies, the cascaded H-bridge MVSI requires the least number of components and does not need clamping diodes or balancing capacitors. Fig. 2.11 presents the number of total component required by the MVSI as a function of phase voltage levels (N). For high MVSI (e.g. 25 levels), cascaded H-bridge MVSI requires fewer components comparing to the diode-clamped MVSI and flying-capacitor MVSI. Thus, the reliability of this topology is high.

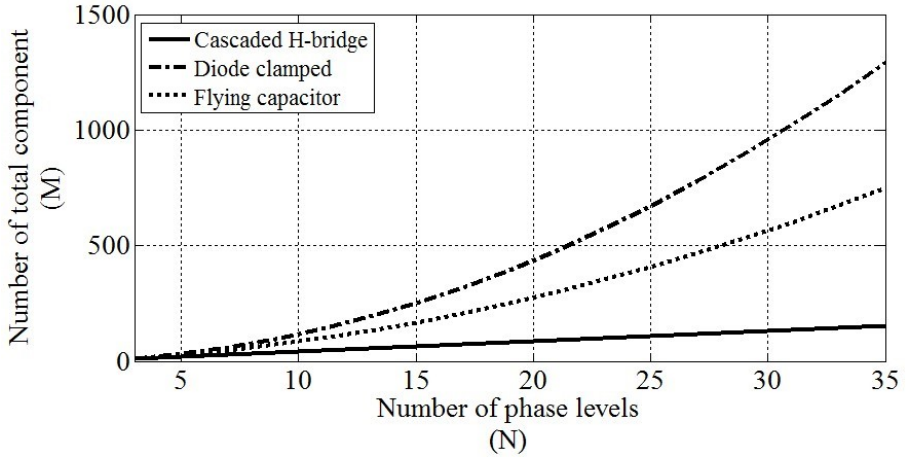


Figure 2.11: Total number of components (M) as a function of phase voltage level (N) in MVSI

Another fundamental advantage of the cascaded H-bridge MVSI circuit is its layout flexibility. Its modular structure allows easier maintenance and provides a very convenient way to add redundancy into the system. Thus, the number of output voltage levels can be easily adjusted by properly selecting the number of H-bridge units to be used in according to the required voltage magnitude. Due to the modularity and the low components number, packaging is easy compared to other tow topologies. Furthermore, the number of dc capacitors utilized for cascaded H-bridge MVSI based STATCOM can be considered an advantage. By integrating the energy storage systems (e.g. fuel cell or ultra-capacitors) with each H-bridge unit, D-STATCOM can provide both active and reactive power compensation.

In conclusion, among the three MVSI structures, the cascaded is the most viable for D-STATCOM due to its modularity, simplicity and fewer component count, hence its application in this work.

2.6.2 Modular Multilevel Cascaded Converters

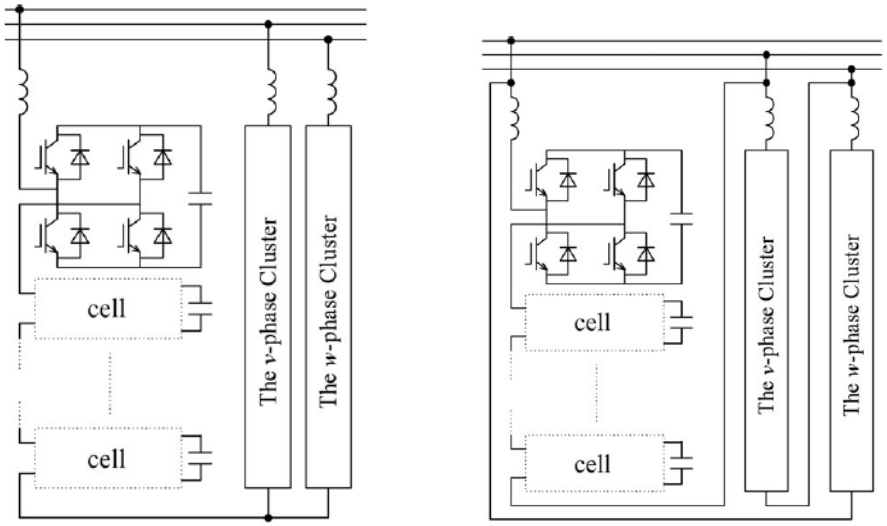
Modularity, in industrial design, refers to an engineering technique that builds large systems by combining smaller and identical subsystems. As discussed in the previous section, the modular structure of cascaded H-bridge topology allows easier maintenance and provides a very convenient way to add redundancy into the system. Due to this concept, many other modular topologies are produced which consist of many identical cells connected in series and these cells are either half or full-bridge converters.

Although modular configurations presents a fairly simple structure and increase reliability of the system, they suffers from large number of isolated capacitors in high-multilevel system which leads to complex *dc* voltage control. However, many works have been conducted to control and balance the *dc* capacitor voltage to obtain optimal performance [32, 19, 79].

2.6.2.1 Classification and Terminologies of MMCCs

The main modular multilevel cascaded configurations are consist of star, delta and double star configurations [2]. This section explain their structure and discuss the viability for STATCOM application.

Single-Star Bridge-Cells (SSBC) and Single-Delta Bridge-Cells (SDBC) configurations are shown in Fig. 2.12. Each phase consists of several H-bridge converters connected in series. Three phases can be connected in either star (Fig. 2.12a) or delta (Fig. 2.12b). A prototype of star and delta configurations as three-phase STATCOM was first demonstrated by Peng et al., in 1996 [76, 80]. After that, these topologies find their way to the industry.



(a) (b)

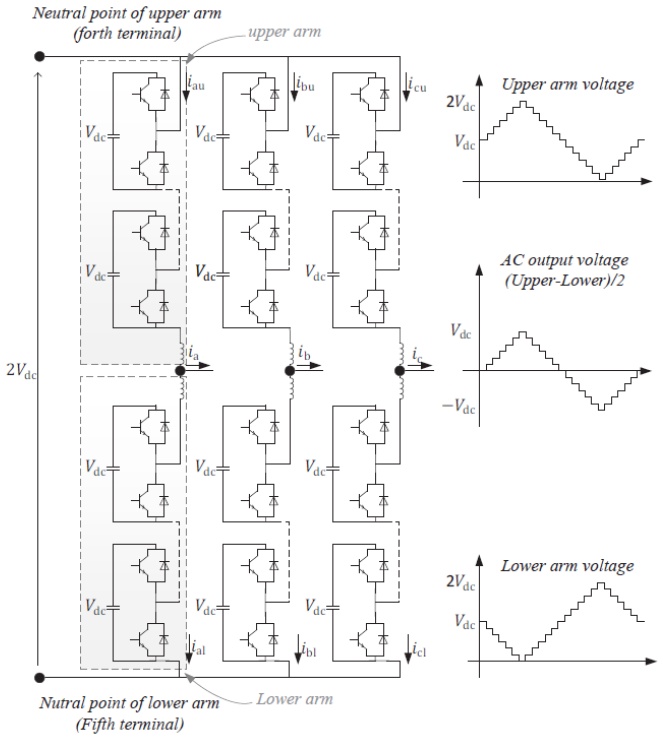
Figure 2.12: MMCC: (a) Single-Star Bridge-Cells (SSBC) (b) Single-Delta Bridge-Cells (SDBC)

Another modular configuration that is receiving great research focus is the Double-Star Chopper-Cells (DSCC) topology, which was originally proposed by Marquardt and Lesincar in 2001 [81], and has the form shown in Fig. 2.13. It is a developed multilevel converter, employing a set of submodules (cells) of identical

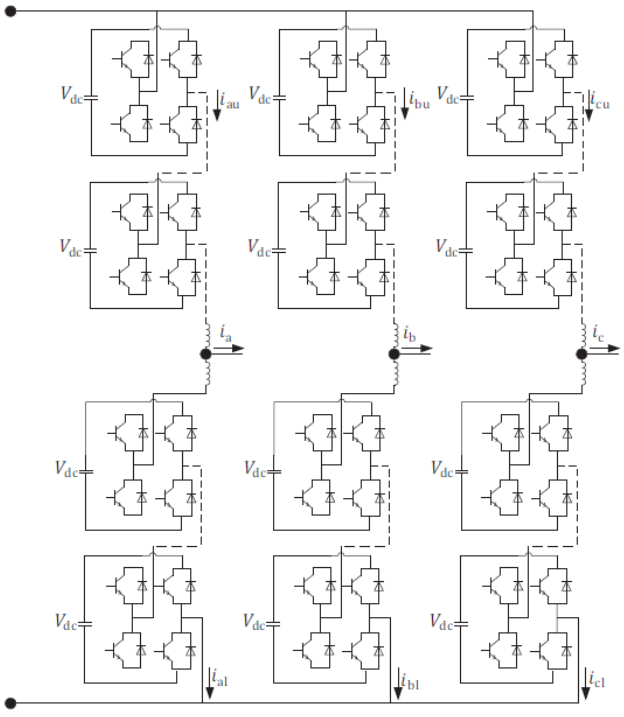
design to provide conversion/inversion process. The individual cells are coordinated by central control to synthesize ac and dc output voltages. This topology is adopted widely for HVDC/MVDC application due to several advantages compared to previously used technologies. Capacitors in each cells are used to define the voltage across the respective IGBTs. Therefore, using these capacitors, DSCC operates as voltage source to synthesize dc/ac voltages (depends on the application) [82].

Each cell contains a pair of switch that can be pulsed in complementary manner to provide the voltage level in the output side of the converter. A widely used approach is to use a single IGBT in each submodule, thus avoiding series connection of them [82]. Blocking voltage of the converters is increased by stacking high number of cells, which allows using commonly available IGBT devices. The converter consists of six legs, each of which contains series connection of cells and connected through a reactor (l) to the ac-system [83, 84]. The ac output is connected in the middle of the two arms. It is also possible to use H-bridge instead of half-bridge (Fig. 2.13a) as illustrated in Fig. 2.13b.

The design of MMCC, which includes selection of capacitors, inductors as well as the number of cells, is based on a tradeoff between the required performance and cost of the system [85]. Applied modulation technique plays very significant role in designing MMCC as it affects harmonics, losses and other performance indices of MMCC systems.



(a)



(b)

Figure 2.13: MMCC: (a) Double-Star Chopper-Cells (DSCC) (b) Double-Star Bridge-Cells (DSBC)

2.6.2.2 Comparison Between MMCC Topologies

This section introduced the main modular multilevel configurations and compare between them in terms of their applicability for STATCOM application. Table 2.2 presents comparison between the main MMCC topologies. Several alternative modular configurations can be found in literature [86, 87].

Table 2.2: Comparison among MMCC family members [1, 2]

Circuit	**Fig. 2.12a**	**Fig. 2.12b**	**Fig. 2.13a**	**Fig. 2.13b**
Given name	SSBC	SDBC	DSCC	DSBC
Effective terminal count	Three terminals	Three terminals	Five terminals	Five terminals
Prominent function	Positive-sequence current control and/or active power	Negative-sequence current control and/or active power	3-phase to 1-phase direct power conversion	Rectification and inversion
Cell count ratio	$1^{V_{ac}}/_{V_{dc}}$	$\sqrt{3}^{V_{ac}}/_{V_{dc}}$	$4^{V_{ac}}/_{V_{dc}}$	$2^{V_{ac}}/_{V_{dc}}$
Circulating current	No		Two degree of freedom	Two degree of freedom
Control complexity	Medium	Medium	High	High
Grid connection	STATCOM and BESS	STATCOM and BESS	3-phase to 1-phase frequency changers	HVDC, BTB and FTF systems
Applicability	+ + + + +	+ + +	+ + + + +	+ + + + +

2.7 Capacitor Voltage Balancing with Different Modulation Techniques

2.7.1 Comparison Between Modulation Techniques for STATCOM

For high power applications, the VSI of the D-STATCOM should operate under low switching frequency to reduce the switching losses. In addition, it should exchange

a high-quality current (i.e. THD less than 5%) with the utility grid. To meet these requirements, the indirect control strategy [88, 89, 22] is used in which the output voltage of the VSI is indirectly controlled by changing the magnitude of the dc capacitor voltage. In this scheme, the phase angle of the VSI output voltage (δ) is the control variable, while M_I is held constant at maximum value. Thus, the output voltage distortion (reflected by the THD value) is kept to a minimum due to the exploitation of maximum value of M_I. In addition, line-frequency inverter can be easily utilized; hence, low switching frequency operation is possible. However, a rapid adjustment of reactive power is unachievable since the output voltage control using δ is restricted by the time constants of charging and discharging of the VSI capacitor.

This speed limitation is addressed by the direct control approach [73, 19]. In this scheme, the capacitor voltages are fixed, while the control of reactive power is obtained by varying the amplitude of the VSI output voltage. The rapid response to the reactive power demand is achieved by changing the M_I of the pulse width modulation (PWM) switching scheme. Despite the improved performance, two problems are inherent for the direct control. First, the THD changes with the variation of M_I. At low values, the harmonics profile of the output voltage is poor. Second, the high switching frequency of the PWM scheme increases the losses of the D-STATCOM [90]. Thus, the modulation techniques play vital role on the operation of STATCOMs.

Different modulation techniques were proposed for MMCC which includes harmonics elimination PWM [20, 5, 21, 22, 23, 24, 25], space vector modulation [26], and multicarrier PWM modulations [27, 28, 29, 30, 17]. However, selection of the proper modulation techniques relies on their performance and ease of implementation.

The most popular modulation technique is the phase shifted PWM (PS-PWM) [27, 17, 91]. The concept is similar to the conventional sinusoidal PWM, whereby the switching pulses are generated by comparing a modulating and multiple carrier signals. For the MVSI topology, the PS-PWM switching operated with number of carriers that need to be phase-shifted in a correct sequence. For instance, to trigger the switches of a 3-phase 15-level MVSI, 29 carrier signals are required. In addition, the PS-PWM cannot directly eliminate the harmonics; thus it needs to be operated

with optimal design of the switching frequency according to the number of levels to maintain the THD below the IEEE-519 Standard (5%). Several works utilizes PS-PWM for STATCOM [19, 27, 91, 17, 31, 34]. For instance, the paper in [19] discusses the control and performance of 6.6-kV 1-MVA 13-level cascaded D-STATCOM using PS-PWM; Work in [27] investigates subtle practical implementation issues that deteriorate the harmonic performance of PS-PWM techniques in 11kV 19-level D-STATCOM and in [91] two PS-PWM schemes are introduced to avoid harmonics degradation; An analytical model for the phase-shifted PWM is proposed in [17] to design the current control gains for 13-level cascaded MVSI D-STATCOM.

Another modulation method that is used in the direct control of the D-STATCOM is the space vector modulation (SVM) [26, 92]. The scheme is based on vector calculation and switching states selection to achieve certain desired performance [93]. Despite the comparatively lower switching frequency that can be attained, the process of selecting switching states becomes increasingly complicated as the level of MVSI becomes higher [21].

On the other hand, the harmonic elimination PWM (HEPWM) [22, 28] is known for its superior harmonics profile and lower switching losses. Despite being an off-line technique (i.e. the angles are computed prior to execution and stored in a look-up table), it is becoming a alternative choice, particularly for high power applications. The difficulty of storing the angles in look-up table does not arise due to availability of low-cost memories. Therefore, HEPWM is a competitive alternative for the direct control scheme of the D-STATCOM especially when the MVSI topology is utilized. However, to implement HEPWM for high output voltage, a wide range of M_I is necessary which in turn, requires more switching angles to be obtained. This is where the challenge in HEPWM is noted. The problem that arises in solving for the HEPWM angles for a wide M_I range is due to the large number of non-linear transcendental equations that govern them [27]. In spite of this, several works that utilize HEPWM for direct control albeit for a lower number of angles, are reported [22, 75, 24]. For example a dc-dc converters have been used with HEPWM technique to control output voltage of single-phase five-level cascaded D-STATCOM [75]. However, in these methods [22], the M_I values are calculated for a maximum levels of 11-levels and for limited

operation range; and for [75], a dc-dc converter is used for each H-bridge to produce a controllable dc input voltage, resulting in a complex and bulky system especially for high levels MVSI. Comparison between the main PWM techniques (i.e. PS-PWM, SVM and HEPWM) for multilevel STATCOM is elaborated in Table 2.3.

Table 2.3: Comparison between modulation techniques for Multilevel STATCOM

Modulation	**Ref.**	**Remarks**
Phase shifted PWM (PS-PWM)	[19, 27, 34, 94, 17]	PS-PWM is prominent on having no restriction on the number levels. To achieve low THD, it is operated with high switching frequency for lower level converters. The operation PS-PWM for STATCOM is well documented and practically approved.
Space vector modulation (SVM)	[26, 92]	Low switching frequency. Complex for MVSI due to the difficulty of the vector calculation.
Harmonics Elimination PWM (HEPWM)	[65, 21, 24]	HEPWM superior in terms of harmonics profile and lower switching losses. The M_I values are calculated offline for high-level converters. Under unbalanced operation, the elimination of the lower order harmonic using HEPWM will not be accurate which will increase the THD of the output voltage.

2.7.2 Operation of Modulation Techniques Under Voltage Unbalance

2.7.2.1 Harmonics Elimination PWM (HEPWM)

Performance of modulation techniques deteriorate under unbalance operation of the capacitors [27, 31, 3]. For reactive power compensation using MVSI based D-STATCOM, isolated dc capacitors are used due to the advantage of reducing the cost and size of the system. However, due to the different losses of each H-bridge unit, measurement error in the voltage and current sensors and the tolerance of the passive

elements, the dc-link capacitors voltages will be unbalanced. Thus, the elimination of the lower order harmonic using HEPWM will not be accurate which will increase the THD of the output voltage hence the current. In addition, when the degree of unbalance increases, the capacitor voltage of some units become higher than others, which affects the safety of the devices or leads to serious system collapse. Thus, balancing capacitors for high-level MVSI D-STATCOM and examining the effect of the balancing techniques on the operation of HEPWM is mandatory for acceptable performance of the system.

Over the past decades, several approaches on this topic have been proposed for different MLCs under HEPWM. These strategies can be classified as [3]: 1) Self-balancing control [95, 96] 2) Charge amount regulation [97, 98]. 3) Zero-sequence harmonic adjustment [99, 100, 101]. 4) Redundant switching angle sets adjustment [102, 103]. 5) Angle modification [104, 105]. 6) Selective harmonic elimination model predictive control (SHE-MPC) [106]. 7) Space voltage vectors adjustment [107]. 8) Redundant states adjustment [104, 73]. Among the above-mentioned eight capacitor voltage balancing methods under SHE-PWM, each of them has its own merits and limitations, which is discussed thoroughly in [3, 108, 109]; these works also provide a guide of selecting the suitable capacitor voltage balancing method for the specific multilevel inverter topology considering its application. A general summary of the published voltage balancing method for the common multilevel inverter topologies under HEPWM is given in Table 2.4.

Table 2.4: Summary of capacitor voltage balancing methods of common MVSI under HEPWM [3]

Strategy	Advantages	Disadvantages	Topology
Self-balancing control	Simple concept and implementation, No voltage and current measurements, No impact on switching frequency.	Limited applicable MLCs, Poor dynamic performance.	SSBC, NPC, MMC, FC
Charge amount regulation	No voltage and current measurements, No impact on switching frequency.	Low dynamic performance, solution trajectories and harmonic performance.	SSBC, NPC, MMC, FC
Zero-sequence harmonic adjustment	No voltage and current measurements, No impact on switching frequency.	Limited applicable MLCs, Narrow effective power factor region, Poor dynamic performance. Reduced output harmonic performance, Not suitable in single-phase applications.	SSBC, NPC, MMC, FC
Redundant switching angle sets adjustment	Simple concept and implementation, No impact on switching frequency.	Limited applicable MLCs, Reduced output harmonic performance, Limited applicable ma range, Extra angle LUTs needed, Generation of interharmonics.	SSBC, NPC, MMC, FC
Angle modification	Simple concept and implementation, No impact on switching frequency.	Limited applicable MLCs, Reduced output harmonic performance, Limited balancing effects in large dynamics.	SSBC, NPC, MMC, FC
Selective harmonic elimination model predictive control	Wide application range, Fast dynamic response during transients, Multi-objective optimization for MLCs.	Potential increase on device switching frequency, High computational burden.	SSBC, NPC, MMC, FC
Space voltage vectors adjustment	Simple concept and implementation, Good dynamic performance.	Limited applicable MLCs, Potential increase on device switching frequency, Reduced phase voltage harmonic performance, Huge complexities for high levels MLCs.	NPC, MMC
Redundant states adjustment	Wide application range for most MLCs, Simple concept and implementation, Good dynamic performance.	Potential increase on device switching frequency.	SSBC, NPC, MMC, FC

2.7.2.2 Phase Shifted PWM (PS-PWM)

On the other hand, both manufacturers and researchers have paid high effort to improve the performance of mutltilevel inverters considering phase-shifted pulse width modulation (PS-PWM) [19]. The modulation is well-accepted for the SSBC based STATCOM due to its high modularity and scalability for higher level. It should be mentioned that for higher levels there is no much concerns about the harmonics as the output waveforms can be approximately sinusoidal. This results in reducing the switching frequency under PS-PWM hence a comparable performance of HEPWM can be achieved.

Phase shifted pulse width modulation (PS-PWM) is utilized for SSBC based STATCOM due to its inherited capability of equal distribution of power and semiconductor stress among H-bridge units, easy to be implemented and perfectly suitable for the commonly used control scheme. However, performance of PS-PWM technique deteriorates under unabalance operation of the capacitors [27]. Thus, capacitor voltage for each converter should be balanced under all operation for stable performance. Commonly, a hierarchical approach with different layers is considered to achieve these objectives [19]. By this approach, outer voltage control generates reference currents for the inner layer for maintaining capacitor voltages, while inner current control loop yields the required reference voltage for producing suitable driving pulses. An additional control layer has to be implemented for ensuring the well balancing of the capacitor voltages.

In [31], authors have investigated impact of switching harmonics on active power distribution and, accordingly, suggested selection of noninteger frequency modulation. Although it helps to alleviate phase-shifted angle errors between the carriers, the technique can not replace the individual balancing control [32, 33, 110, 111]. In unbalanced operation, an additional layer (i.e. cluster balancing) is required to equally share active power between the three phases. Many works were conducted to balance capacitors voltages during fault operation and several methods were proposed which can be summarized as [34]: (1) independent clustered voltage control for each phase [19], (2) zero sequence injection control [112, 113, 18] and (3) negative sequence injection control [34, 114, 115, 116].

2.8 Potential Applications of FACTs devices

2.8.1 Arc Furnace Flicker Mitigation

Heavy industries get powered directly from the transmission network, at 70 to 130 kV or higher voltage levels. Agreements with power utilities include the maximum supply of both active and reactive power. Additionally, utilities put limits on several power quality parameters such as flicker, harmonics, and unbalance. Exceeding these limits imposes penalty fees, or in severe cases, the industry might be forced to reduce or stop its operation. Therefore, heavy industries can fix a price on reactive power and power quality.

In the mining and steel industries, special loads require particularly matched reactive power compensation. Mines are often located at the end of long transmission lines, in weak networks, or island operation. This in combination with heavy mining loads creates issues with both grid stability and power quality. Electrical Arc Furnaces (EAF) require access to large amounts of reactive power. An EAF also gives rise to unsymmetrical loading and therefore has to be compensated phase by phase. The turbulent nature of the EAF also causes light flicker and other disturbances in the grid. When an induction motor starts up, it can use 6 to 8 times more current than the normal operation, causing voltage dips. Industrial networks with large induction motors are therefore frequently equipped with special shunt-connected starting capacitors. Besides, if motors are sufficiently large and started sufficiently often in a weak network, thyristor-controlled compensation employing SVC is often necessary. In process industries, there is normally a reactive baseload consisting of a very large number of AC motors. Within the steel industry, there are electric arc furnaces that consume a great deal of reactive power. An example of this is the arc furnace used to melt scrap (Fig. 2.14).

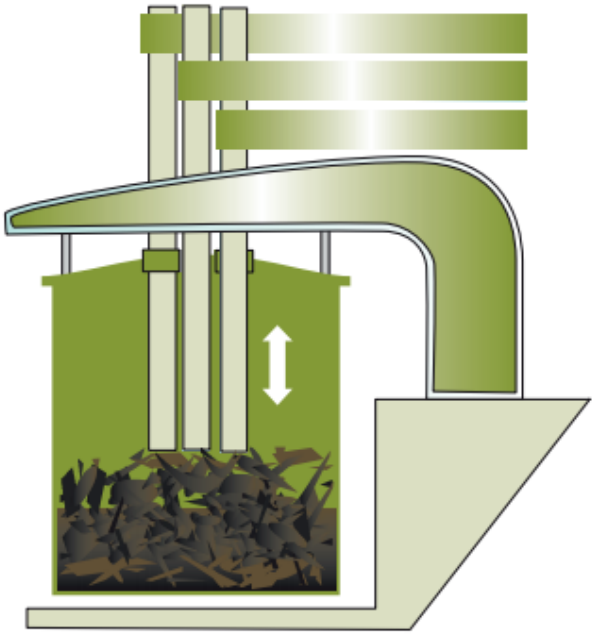


Figure 2.14: Arc furnace used for scrap melting

The basic methodology for flicker mitigation can be categorized into three types [117]: 1) The first is regulating the EAF passive components, such as source impedance. Although to some extent, the increasing series reactance can mitigate the flicker, it reduces the power supply and therefore decreases EAF productivity. Moreover, it is also expensive and laborious to control upstream transformer reactance or series reactor in the firmer deregulation power system, 2) The second is compensation through the combination of thyristor and passive components (using SVCs). They don't only improve the power quality of the nearby system but can also increase EAF productivity and bring additional economic benefits. However, it cannot catch up with the fast-varying flicker (1–20 Hz) very well with the inherent limitations of relatively low bandwidth. Hence, its dynamic performance for flicker mitigation is limited, and 3) The state-of-the-art solution is STATCOM based on a high-frequency voltage-source converter (VSC) [118, 117].

With currently available high-power semiconductor devices such as IGBTs and GCTs, STATCOM can switch at several kilohertz and achieve a closed-loop bandwidth

at several hundred hertz. Hence, the response time is less than one cycle. STATCOM can also provide real power compensation if interfaced with an energy storage unit, all of which are unattainable for SVC [119, 120]. With these benefits, the STATCOM performs significantly better than SVC, making it the best flexible ac transmission system (FACTS) device for flicker mitigation.

2.8.2 Connecting the Railway to the Grid

Many main lines electrified railway systems operate at 25 kV 50/60 Hz. There is a number of different ways to feed traction systems with electric power. The most common scheme used in many electrification systems is to directly supply it by the fundamental frequency of the main power. The transmission or sub-transmission voltages are then directly transformed by a power transformer to the traction voltage. The Auto-Transformer scheme is commonly used for high-speed lines [121].

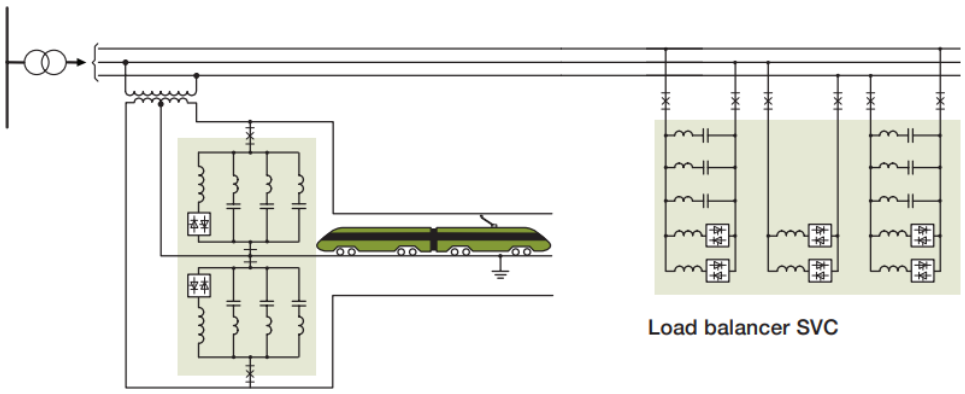


Figure 2.15: Load balancer SVC for Railway application

Although latest generation of locomotives uses ac traction motors powered through sophisticated pulse width modulation (PWM) ac drive control systems, many of the locomotives still in service today are based on dc traction motors. These older types of locomotive use thyristor-based rectifier converters for speed control and, hence, not only draw a significant amount of lagging load current at fundamental frequency but also inject significant levels of harmonic current back into the overhead feeder.

As in a public distribution system, the nonsinusoidal current waveform drawn by the dc motor locomotives degrades the power quality of the traction supply. However, traction supply systems are usually private, used exclusively for locomotive loads. Therefore, the quality of supply requirements is different from that of a public electric system. Therefore, by means of FACTS, the following important benefits can be brought about for power grids feeding railway systems (shown in Fig. 2.15), as well as for rail traction loads themselves:

- Dynamic balancing of non-symmetrical loads fed between two phases of three-phase grids;
- Dynamic mitigation of voltage fluctuations in feeding grids caused by heavy fluctuations of railway loads;
- Mitigation of harmonics injected into supply grids from traction devices;
- Power factor correction at the point of common coupling, with a high and stable power factor at all times, regardless of load changes and fluctuations;
- Dynamic voltage support of catenaries feeding high power locomotives, thereby maintaining traction capability despite weak feeding, without harmful voltage drops along the catenary;
- Dynamic voltage support of catenaries during outages of feeding points, thereby enabling adequate power infeed into locomotives, or, alternatively, with fewer infeed points required in the system;
- Dynamic voltage control and harmonic mitigation of AC supply systems for DC converter fed traction (typically underground and suburban trains).

In all these cases, time and money can be saved by avoiding reinforcement of the railway feeding infrastructure such as building new transmission or sub-transmission lines and new substations and infeed points.

2.8.3 Grid Integration of Wind Farms

When a fault occurs in a feeder to which the wind farm is connected it will be disconnected with the faulty part. But, if the wind farm is connected to the non-faulted part of the system, it is desirable that the wind farm stays connected during the fault.

As soon as the faulty feeder has been disconnected, the wind turbine generators should return to operation to avoid causing consequential loss of generation which may lead to a system collapse. Therefore the wind farm connection must be designed to be capable of continuous uninterrupted operation to support fault ride-through.

For a weak electrical network, the behavior of the wind farm at network faults will be strongly improved by reactive power support. An SVC/STATCOM can be installed as a reactive power source located close to the farm as shown in Fig. 2.16. It can bring several advantages:

- Full compensation of wind farm and cable in one system
- Fulfilling the national Grid Code
- Control of reactive power, even without the wind farm in operation
- Lower wind farm complexity
- High wind farm availability
- Improvement of dynamic voltage stability in the grid
- Wind farm, cable, and SVC act together to offer MW and MVAr in the grid, similar to any other major generation source.

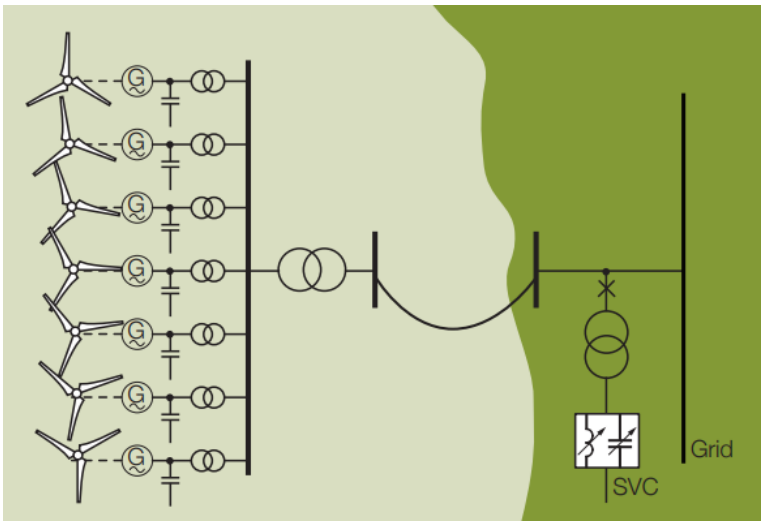


Figure 2.16: Grid Integration of Wind Farms with SVC

2.9 Summary

A detailed overview of multilevel inverters for STATCOM is presented in this chapter, which includes the inverter topologies, control strategies, and modulation techniques. In terms of topologies, modular multilevel cascaded converters (MMCCs) are widely used to overcome the drawbacks of the conventional two-level VSI. Among the common MMCC topologies, Single-Star Bridge-Cell (SSBC) topology is shown to be the best choice for STATCOM due to its reliability and layout flexibility. Additionally, in terms of modulation techniques, phase-shifted PWM is preferred due to inherited equal distribution of power and semiconductor stress among H-bridge units, easy to be implemented and perfectly suitable for the commonly used control scheme for STATCOM. Thus, in this work, it is considered for the implementation of the SSBC based STATCOM system. The next chapter elaborates the detailed methodology of its operation and implementation along with overall control of the system.

CHAPTER 3

HARDWARE DESIGN AND ANALYSIS OF SSBC-STATCOM

3.1 Introduction

With more installation of electronic loads and of distributed renewable energy sources, static compensators gain more interest to encounter the resulting power quality issues in low and medium voltage grids. Traditionally, two-level inverter topology is utilized for this application, eventually with transformer at medium voltage. However, due to the low harmonics performance and the requirement for bulky filtering, the multilevel converters topologies become more attractive. Different topologies have been introduced during the last few decades and among the others, the Single-Star bridge cell is well applied to this application for its satisfactory performance and superior component count. Generally, the feasibility of adoption of static compensators for low and medium voltage systems relies strictly on their performance and cost-effectiveness. Theoretically, the harmonics performance improves with increasing the number of levels. However, this has a direct effect on their design and hence on their overall complexity and cost. There is no work that has extensively discussed the impact of the number of levels on the cost of static compensators. Thus, in this chapter, some key factors in STATCOM design will be investigated with emphasis on their impact on the overall cost in low and medium voltage applications.

3.2 Literature Background

Traditionally, two-level voltage source inverter (VSI) with a series coupling inductor, is used as the main building block of the Static Compensator (STATCOM). However, the output voltage of the VSI is characterized by high harmonics that require bulky and costly filters. Furthermore, for high and medium voltage interconnections, it is mandatory to use the line frequency (50 or 60 Hz) step-up transformer to match the output voltage of the VSI with the utility grid. This increases the cost, size, weight and power losses of the overall STATCOM as well as affects the system dynamics. Thus, the multilevel VSI (MVSI) is being exploited to replace the two-level VSI [2].

The salient features of this topology include: 1) modularity and scalability, to fulfill high-voltage level requirements, 2) feasibility of the direct connection to high-voltage networks without using transformers, therefore, reducing system size, cost, losses and footprint, 3) superior harmonics performance due to the high level of the output voltage waveform in which a large number of submodules with low rating switches are used, thereby allowing a significant reduction in the filtering requirement, and 4) low expense for fault-tolerant operation due to utilization of standard, low voltage components, such as 600 V - 1200 V IGBT.

Assuming cascaded H-bridge as the reference basic module topology, for multilevel STATCOM, the controlling factor is the number of bridges (N) [19]. The selection of N accounts for the blocking voltage of the switches and consequently the input capacitor size. Therefore, with higher multilevel, lower-cost switches and smaller capacitance can be utilized. Besides, this allows system operation with low switching frequency. Thus, filtering and thermal requirements can be reduced due to low losses. However, the number of components (switches, gate drivers, and voltage sensors) rises; consequently complexity of the system increases.

As STATCOM can be effectively used in both medium and low voltage systems, the aforementioned design aspects might change disparately. For instance, design of 20 kV STATCOM necessitates distinct requirements in terms of isolation and layout as well as components ratings (switches and capacitors). Many works on utilization of multilevel converters for STATCOM are presented which can be classified into topologies, control and modulation techniques [80, 122, 94, 79]. Some papers have compared these topologies in terms of component count, performance and capacitance requirements. However, the cost aspect is not included. In [123, 115], losses and cost estimation for two modular multilevel topologies are performed. However, the comparison is made with one design case and there is no detailed investigation about the effect of the number of levels on the system cost. In [109], five cascaded bridges are used for 12 kV SSBC STATCOM using 3.3 kV IGBT. Although authors have considered different levels, the design is only based on harmonics performance. Work in [30] used 1.7 kV IGBT to construct the SSBC STATCOM in which twelve cascaded bridges are used in each phase. However, cost justification for this design is not presented.

There is no publication that comprehensively discusses and investigates the effect of increasing the number of levels of SSBC STATCOM for medium and low voltage systems on the overall cost. Therefore, this study is dedicated to investigating the implementation cost of SSBC STATCOM with different cascade number design. The work tries to disclose the relationship between the STATCOM implementation cost and the number of levels in both low and medium voltage systems. Two case studies are considered for this purpose (i.e. 400 V and 11 kV). The outcomes of this analysis can be extended to other multilevel topologies.

3.3 Single-Star Bridge-Cell STATCOM

The single-star bridge-cell (SSBC) topology is considered to be among the most attractive due to its modularity and fewer component count [1]. It is built by stacking a number of H-bridge (each with its own isolated dc source) to form a stepped output waveform. By increasing the number of H-bridges, more output steps are synthesized, resulting in higher output voltage. If N denotes the number of H-bridge inverter units, the line and phase voltages are $4N + 1$ and $2N + 1$, respectively. The structure of a three-phase SSBC STATCOM is shown in Fig. 3.1.

In conventional two-level STATCOM, a single capacitor bank is used to maintain the dc-input voltage of the VSI. In SSBC, the number of capacitors is proportional to the number of the synthesized levels, however, due to the different losses of the H-bridges, adopted modulation technique, measurement error in sensors and tolerance of passive elements, $dc-$link capacitors voltages could be unbalanced. In addition, under fault operation, the unbalanced problem is more severe. With different number of levels, balancing requirements will be different in terms of complexity and associated number of sensors. Thus, balancing is fundamental in cost analysis. In this work, the control method presented in [19] is considered in which it is accomplished by two layers. The inner current control loop yields the required reference voltage for producing suitable driving pulses, while the outer voltage control generates reference currents for the inner layer for maintaining capacitor voltages. Different modulations are presented for generating gate driving pulses. Phase shifted pulse width modulation (PS-PWM) is commonly used for SSBC STATCOM due to equal distribution of power and semiconductor stress among the H-bridge units [124]. Therefore, it is considered

throughout the design in this study. The overall control is shown in Fig. 3.2 and the component count for SSBC with different levels are listed in Table 3.1.

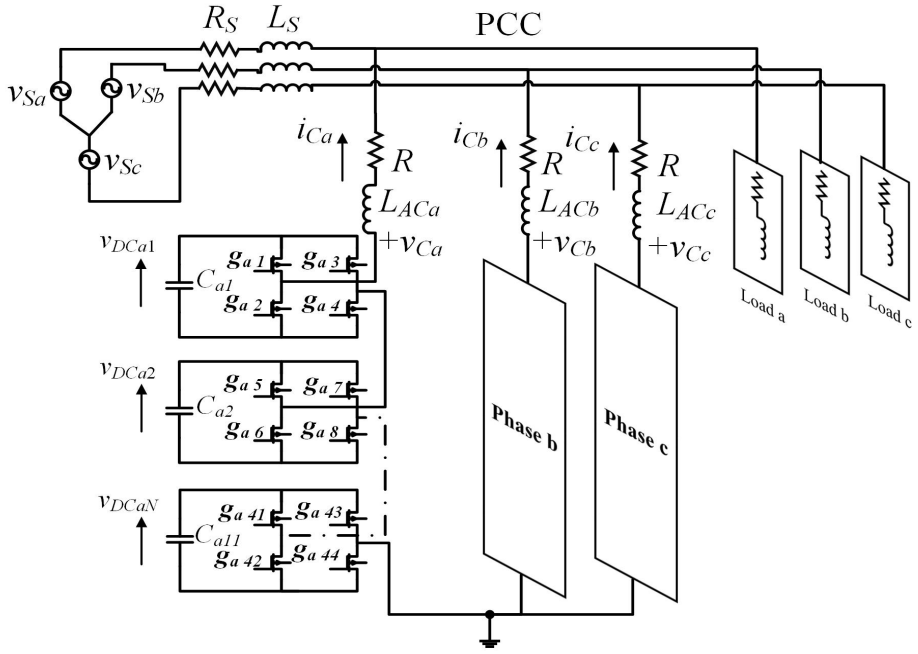


Figure 3.1: Three-phase SSBC based STATCOM [5]

Table 3.1: Components count for Single-Star Bridge Cell

Levels	Switches	Drivers	Heatsink	Voltage sensors	Capacitors
7-levels	36	18	36	9	9
13-levels	72	36	72	18	18
23-levels	132	66	132	33	33
33-levels	192	96	192	48	48

3.4 Multilevel SSBC-STATCOM Design

The design study should consider the effect of the harmonic of connecting the STATCOM system to the point of common coupling (PCC), hence, after determining the voltage and current rating of the system, maximum stresses on all STATCOM's components can be determined. Accordingly, considering the worst cases, the passive and active components can be selected.

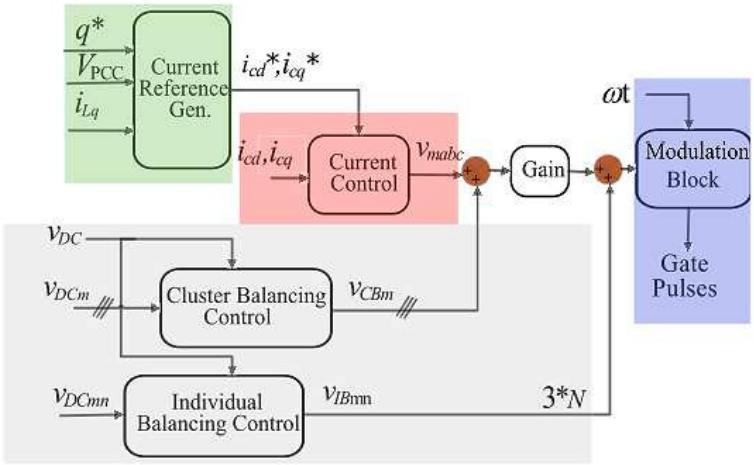


Figure 3.2: SSBC based STATCOM control

3.4.1 STATCOM System Rating

The basic function of STATCOM is to rapidly control the reactive power (i.e. generation or absorption) according to the control purpose. In most cases, it is used to control the busbar voltage, while sometimes it is utilized for optimal control of reactive power at a particular point of the grid network. Transmission STATCOM (T-STATCOM) is mostly used for voltage regulation employing changing the flow of reactive power in the network. Therefore, the rating of STATCOM is determined by the effective reactive current that can bring the voltage at a specific node to a stable condition. In contrast, STATCOMs applied in distribution systems (D-STATCOMs) are typically less complex than T-STATCOMs in their design, manufacture, operation, and maintenance. D-STATCOMs are typically applied at or near a load center to mitigate voltage fluctuations, flicker, phase unbalance, or other load-related disturbances. Thus, the determination of a STATCOM rating is based on knowledge of the behavior of the connected load.

Generally, STATCOM is used to achieve one of the following control objectives functions:

1. voltage control: To restore busbar voltage to normal after a system disturbance, e.g., due to a fault or load rejection.
2. reactive power control:

(a) Coordination of VAr contributions from other equipment: to control the switching of externally connected shunt capacitors and reactors.

(b) Fast correction of impact of variable loads: the generation or absorption of VAr to counteract the effect on voltage of the variation of power and VAr demand of loads that are balanced between phases but variable in time (e.g., convertor fed drives for rolling mills).

(c) Fast correction of power factor: the generation and absorption of VAr to meet a particular demand of a load or group of loads, or to counteract a flicker-generating load.

(d) The correction of unbalance: the generation or absorption of VAr asymmetrically between the phases to counteract the negative phase sequence components of loads or system components. The action can balance phase voltages by adding reactive loads in two phases to offset an active load in the other phase.

3. control of non-power frequency effects:

(a) Harmonic filtering: to reduce the harmonic voltage distortion caused by the harmonic currents generated by the STATCOM itself.

(b) Subharmonic filtering: the STATCOM system cannot be expected to contribute to the removal of all subsynchronous currents or resonances. However, it may, by suitable control responses in the appropriate frequency range, either avoid worsening them or provide a counteracting effect.

(c) Managing of background harmonics: the STATCOM system may be required to be designed to maintain background harmonics within an acceptable level. However, it may, by suitable control responses in the appropriate frequency range, either avoid worsening them or provide a counteracting effect. The STATCOM system is not expected to reduce all background harmonics. Controlling background harmonics may require additional active filtering control loops on the STATCOM or additional passive or active filters. This may result in additional losses in the added components and/or an increase in the rating of the STATCOM system.

The improvement of one of the aforementioned aspects will sometimes degrade another, thus, for multi-objective operation, it is important to prioritize the STATCOM operation to respond to these preset control objectives and/or limit the control action and their effects. The reactive power rating of D-STATCOM is governed by

$$Q = \pm \frac{V_g}{X_{ac}} \left(V_g - V_r \right) \tag{3.1}$$

where V_g is the magnitude of the grid voltage at the point of common coupling, V_r is the magnitude of the STATCOM voltage and X_{ac} is the inductive impedance between STATCOM and the grid.

3.4.2 Power Switches

In designing the SSBC-STATCOM, selection of cascade number of H-bridge (N) is an important parameter because it accounts for the blocking voltages of the switches used in constructing the system. According to [19], assuming the effective (RMS) AC voltage of each H-bridge V_{AC}, the mean DC values V_{DC} and defining a design parameter κ, follows that

$$V_{AC} = \frac{V_{DC}}{\kappa} \tag{3.2}$$

Then, the cascade number N can be calculated as follows

$$N = \frac{kV}{\sqrt{3} V_{AC}} \tag{3.3}$$

It should be mentioned that in (3.2), κ gives flexible operation range. If 1.2 kV IGBTs are used for building the STATCOM, V_{DC} = 600 V is generally considered the maximum value ensuring safe operations. By selecting κ = 1.6, the cascade number N = 16 is fitting to connect the STATCOM to 11 kV system for instance.

3.4.3 Capacitor Sizing

Capacitor selection is a crucial aspect in designing power converter. It should be carefully chosen to reduce the voltage ripple that deteriorates waveforms and could bring to semiconductors failure. High capacitance values result in ripple reduction and in overall performance improvement, but at the same time system size and cost increase. Therefore, a trade-off must be considered. In typical applications, voltage variations should be limited to around 10% of the nominal voltage. In addition, the choice of capacitor type (i.e. electrolytic, polypropylene etc.) has a serious impact on overall cost. Assuming an equal capacitance for all H-bridge units, required capacitor C is calculated by [94]

$$C = \frac{M_I \times I_{RMS}}{4\pi f \epsilon V_{DC}} \tag{3.4}$$

where:M_I is the modulation index which is assumed to be at maximum value, I_{RMS} is the maximum current rating, f is the fundamental switching frequency, ϵ is the voltage ripple magnitude and V_{DC} is the capacitor voltage rating. To show the effects of capacitor value and switching frequency on voltage ripple, simulation of 7-level SSBC based STATCOM is conducted with different cases and the results are demonstrated in Fig. 3.3 and Fig. 3.4. It is clearly shown that switching frequency has negligible effect on voltage ripple magnitude. Ripple harmonics deteriorate with low switching frequency which might affect injected current harmonics, however, the magnitude of the second harmonics, which determines capacitor voltage ripple, is significantly affected by current rating and the capacitance. Therefore, the design in this paper considers these two aspects in calculating the capacitor value.

3.4.4 Heat Sink Design

One of the important factors that affect the cost of the STATCOM is its thermal behavior. The output power and overall performance are affected by several factors including passive and active components losses. The conduction and switching losses increase the temperature across the power devices, and if not properly anticipated, might heat up switches over their junction temperature, hence, causing operation failure, and

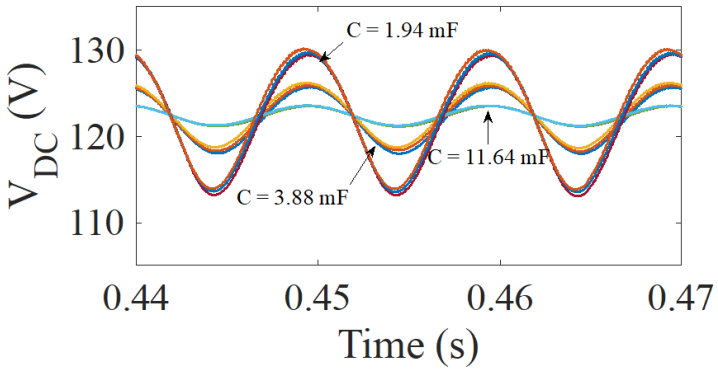


Figure 3.3: Effect of capacitor values on the ripple magnitude

in a worse case, fire. To avoid such condition, the thermal limit of selected switches should be properly determined by calculating the dissipated power losses

$$\theta_{thsa} = \frac{(T_j - T_a)}{P_D} - (\theta_{thjc} + \theta_{thcs}) \tag{3.5}$$

where θ_{thsa}, θ_{thjc} and θ_{thcs} are the thermal resistance of sink to ambient, junction to case and case to sink respectively; T_j, T_a are the junction and ambient temperatures and P_D refers to the power loss. To study the effects of heatsink design on overall cost of SSBC STATCOM, the effective switching frequencies for different multilevel STATCOMs are initially determined in such a way that current harmonics remain unchanged. Therefore, the coupling inductor L_{AC} between the STATCOM and the grid is fixed for all cases. Using Phase Shifted PWM modulation (PS-PWM), which is commonly used in STATCOM application, the switching frequencies are calculated

$$f_{sw} = 2 \times N \times f_{cr} \tag{3.6}$$

where: $f_{cr} = k_{cr} \times f_F$, is the carrier frequency, N is number of H-bridge per phase and f_F is the fundamental frequency.

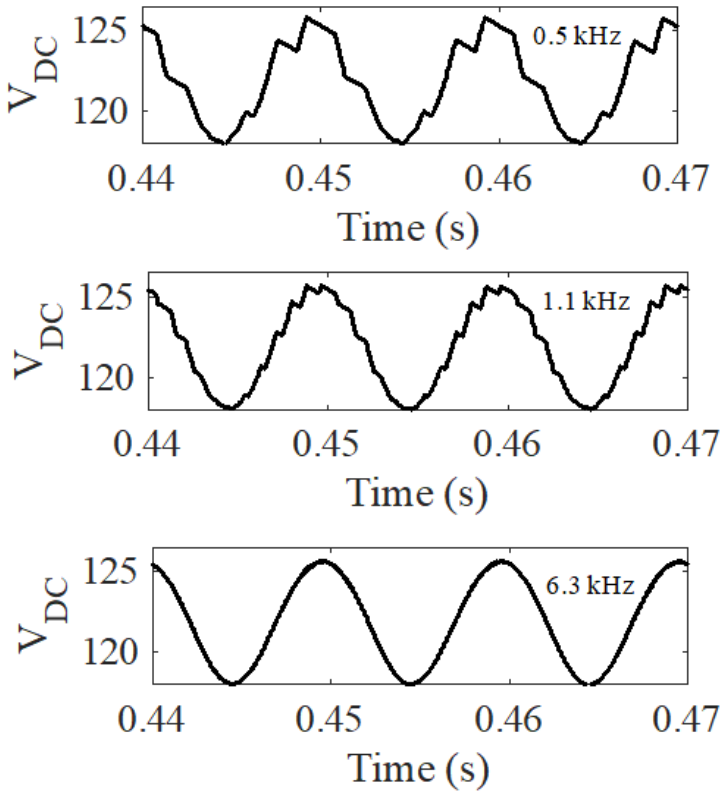


Figure 3.4: Effect of switching frequency on the ripple voltage

3.4.5 Gate Driver Requirements

Another important part in designing SSBC STATCOM is the gate driver which has direct effect on optimal switching of power devices hence affecting the performance of the whole system. In a medium-voltage STATCOM application, IGBTs up to 6.5 kV might be used. Therefore, galvanic isolation and overvoltage protection are central elements in designing the required gate drivers. From these points, gate driver design differs for different voltage level applications and, therefore, the estimation of the cost will also be different.

3.4.6 Filtering Requirements

Generally, L and LCL line-filters are mainly used to connect STATCOM to the utility system. The L-filter is a first-order filter that uses series inductor in each phase to connect STATCOM to the grid. Using conventional two-level VSC topology, with L-filter, the switching frequency has to be high to fulfill harmonics attenuation standards which results in a reasonable size of the line filter. Increasing switching frequency results in higher losses and hence higher cost of the heat sink design. Alternatively,

two methods are commonly used to reduce switching frequency of the converter which are: 1) adoption of modular multilevel topologies and 2) using higher-order LCL-filter.

MMCC topologies prove to be attractive for reducing the filtering requirements and consequently footprint and losses. Modularity concept of these topologies enables high prefabrication and in-factory testing, bringing to an overall reduction of project lead-time and enhancement of product quality. Besides, with a high number of levels, positive impacts on the overall cost of the system can be obtained, although it requires optimal and careful design, considering other factors which include voltage and current ratings, production quantity, component count, PCB design and other related mechanical and installation and communicational costs. As discussed in [125], assuming single-star bridge-cell (SSBC) as the reference basic module topology, the selection of number of levels (N) is an important design factor for the cost analysis of multilevel STATCOM system which accounts for the blocking voltage of the switches and consequently the input capacitor size. With higher number of levels, lower cost switches and smaller capacitor can be utilized. Another main advantage of increasing number of levels is reducing the switching frequency. Thus, filtering and thermal requirements can be reduced due to the low losses. Thus, theoretically, the L-filter design is sufficient for multilevel STATCOM with the proper design of the number of levels.

Alternatively, LCL-filter can be used for the attenuation of the harmonics caused by the PWM converter which its performance increases at a rate of 60 dB per decade above the resonance frequency in comparison with the increase of 20 dB per decade for the L-filter [126]. This feature makes it possible to obtain good harmonics performance of the currents at low and moderate switching frequencies. Besides, considering the performance of the harmonic, LCL filter structure results in low inductance values compared to L-filter under the same switching frequency. However, selecting the parameters of an LCL-filter is a complicated task [127, 128]. Besides, more complex current control strategies are required for LCL based systems to maintain their stability, and due to the resonance, they are more susceptible to harmonics interference [127], which means that the design of LCL-filter is highly interconnected to the grid impedance.

3.4.6.1 L-filter Design

The ripple current and the voltage drop are the main design consideration of the filter. Using the simple first-order filter (L-type) with small value results in high current ripple and consequently the controlled current will be sensitive to the variation of the output voltage. Additionally, the current harmonics might be increased higher than the allowed IEEE 519-1992 Standard. In contrast, if the designed inductance is too large, higher voltage drop is produced, hence a larger output voltage of the STATCOM is required to generate the same current. In addition, larger value, theoretically increases the cost, size and losses**.** Thus, proper design of the filter is required considering these factors for specific power and switching frequency applications. A tradeoff between current ripple and voltage drop is usually considered in designing L_{AC},

$$\frac{\epsilon V_{PCC}}{\omega I_{RMS}} \geq L_{AC} \geq \frac{U_{DC}}{8\eta f_{sw} I_{RMS}} \tag{3.7}$$

where: I_{RMS} is the STATCOM output current, ϵ is the voltage drop coefficient ($\epsilon \leq 10\%$), U_{DC} is the overall DC voltage in the input side of STATCOM, η is the ripple current coefficient ($\eta \leq 25\%$) and f_{sw} is the switching frequency.

3.4.6.2 LCL-Filter Design

To obtain sufficient attenuation of the harmonics caused by the PWM converter, LCL filter is used. The main advantages of this filter are

1. attenuation of 60 dB/decade for harmonics over the resonance frequency.
2. possibility of using lower switching frequencies and inductance values compared to L-filter.

The design procedures start by selecting the converter-side inductor (L_1) using

$$L_1 = \frac{U_{DC}}{8\eta f_{sw} I_{RMS}} \tag{3.8}$$

which is the lower limit defined for the range of selecting the L-filter value. Then, based on the rating of the system, the capacitance of the filter can be chosen to limit the reactive power production (e.g. 5%)

$$Z_{base} = \frac{1}{\omega C_b}, \qquad C_f = 0.05 C_b \tag{3.9}$$

The LCL filter should reduce the expected current ripple to 20%, resulting in a ripple value of 2% of the output current. Thus, the inductance at the grid-side can be calculated according to

$$L_2 = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f \omega_{sw}^2} \tag{3.10}$$

where ω_{sw} refers to the switching frequency and k_a is the attenuation factor. For stable operation of STATCOM, resonance frequency needs to be designed according to

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{3.11}$$

and it is limited by the following condition

$$0.5 f_{sw} > f_{res} > 10 f_F \tag{3.12}$$

This information helps in designing the series resistor R_{res} with the capacitor to attenuates part of the ripple on the switching frequency in order to avoid the resonance which can be calculated using:

$$R_{res} = \frac{1}{6\pi f_{res} C_f} \tag{3.13}$$

3.4.6.3 Case Study

For 9-level STATCOM with V_{dc}= 40 V and considering V_{L-L}= 142 V and I_{rms} = 8 A, total switching frequency f_{sw} = 4 kHz, the two filters values can be defined as follows:

- L-filter inductance should be selected between the range of

$$\frac{\epsilon V_{PCC}}{\omega I_{RMS}} \geq L_{AC} \geq \frac{U_{DC}}{8\eta f_{sw} I_{RMS}} \tag{3.14}$$

$$5.6\,\text{mH} > L_{AC} > 2.5\,\text{mH} \tag{3.15}$$

Usually, high inductance on this range is selected to achieve the required attenuation, or alternatively higher switching frequency is used in combination to reach to the desired harmonics performance.

- For LCL filter,the lower range limit in the L-type filter design is chosen for the converter-side inductance , L_1 = 2.5 mH. The capacitor value is designed to limit the reactive production of the capacitor to 5% , thus C = 8.97 mF is selected. Then grid-side inductance , L_2 = 1.06 mH is selected. The required resonance damping can be achieved using f_{res} = 1948 Hz, capacitor's series resistor $R_{res} = 10\,\Omega$.

In both cases, the values need to be selected according to the price and standard components used in the market.

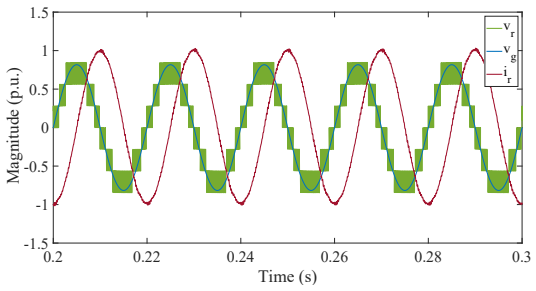


Figure 3.5: 9-level SSBC STATCOM with LCL filter

THD comparison between the two filters is demonstrated in Table 3.2:

Table 3.2: THD comparison between L and LCL filter

Parameter	L-filter using L = 3.57 mH	L-filter using L = 5 mH	LCL-filter
i_r THD	2.93%	1.6%	1.86%

3.4.6.4 Coupling Inductance vs. Converter Output Current Harmonics

The effect of the coupling inductor on the line current harmonic is examined by applying different inductance values. The STATCOM was simulated in both modes (± 2 kVAr) of operation with a switching frequency of 4 kHz. The harmonics spectra of the line currents in the capacitive and inductive modes are plotted in Fig. 3.6 and the THD values are reported in Table. 3.3, for values of 6 mH and 2 mH. By comparing both, it is shown that a larger inductor can attenuate more harmonic components in both operation modes resulting in lower THD values.

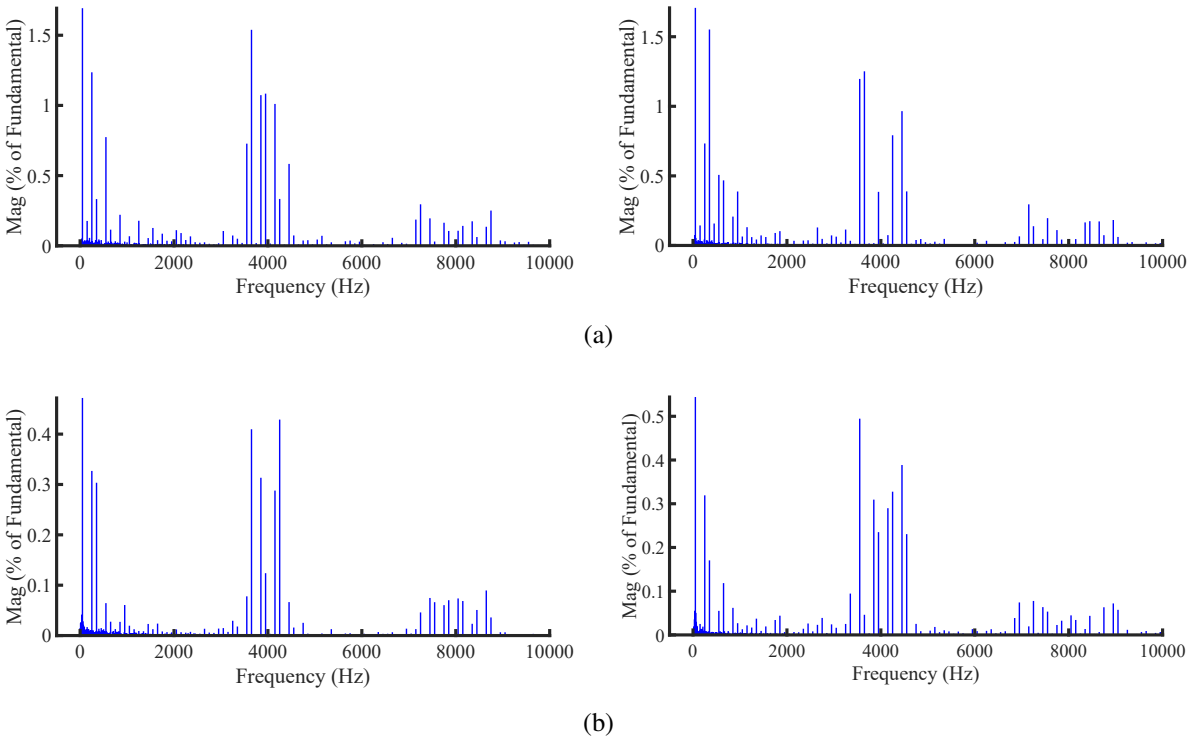


Figure 3.6: FFT analysis of line current with (a) L_{ac} = 2 mH (b) L_{ac} = 6 mH (inductive modes left side, and capacitive mode right side)

Table 3.3: Effects of the inductance on the current harmonics

Parameter	L_{ac} = 2 mH	L_{ac} = 6 mH
Inductive	3.09%	0.91%
Capacitive	3.0%	1.01%

3.4.6.5 Coupling Inductance Design and Converter Operation Range

The amount of reactive current exchanged between the STATCOM and the point of common coupling (PCC) is controlled by the voltage drop across the coupling inductor. In other words, the output voltage of the converter is controlled to provide a suitable voltage drop across the coupling inductor. According to modulation techniques, the duty cycle determines the operating window range for the converter. In general, the duty cycle is limited to 1 p.u. by the switching behavior of power converters. The operating range of the converter, therefore, limits the size of the coupling inductor.

Fig. 3.7 demonstrates how the coupling inductor affects the operating window of the converter. The same system with the same control parameters is operated with

two different coupling inductors, i.e., one at 6 mH and one at 2 mH. The results show the transition of the modulation-index responses to the command from full inductive to full capacitive mode to fulfill the operation of ±2 kVAr. The system with 6 mH requires the change of M_I from 0.58 p.u. to 0.87 p.u. while for 2 mH, the reported values are 0.67 p.u. and 0.80 p.u. for the inductive and capacitive modes respectively. Thus, for lower inductance values, the reactive power compensation capability can be increased.

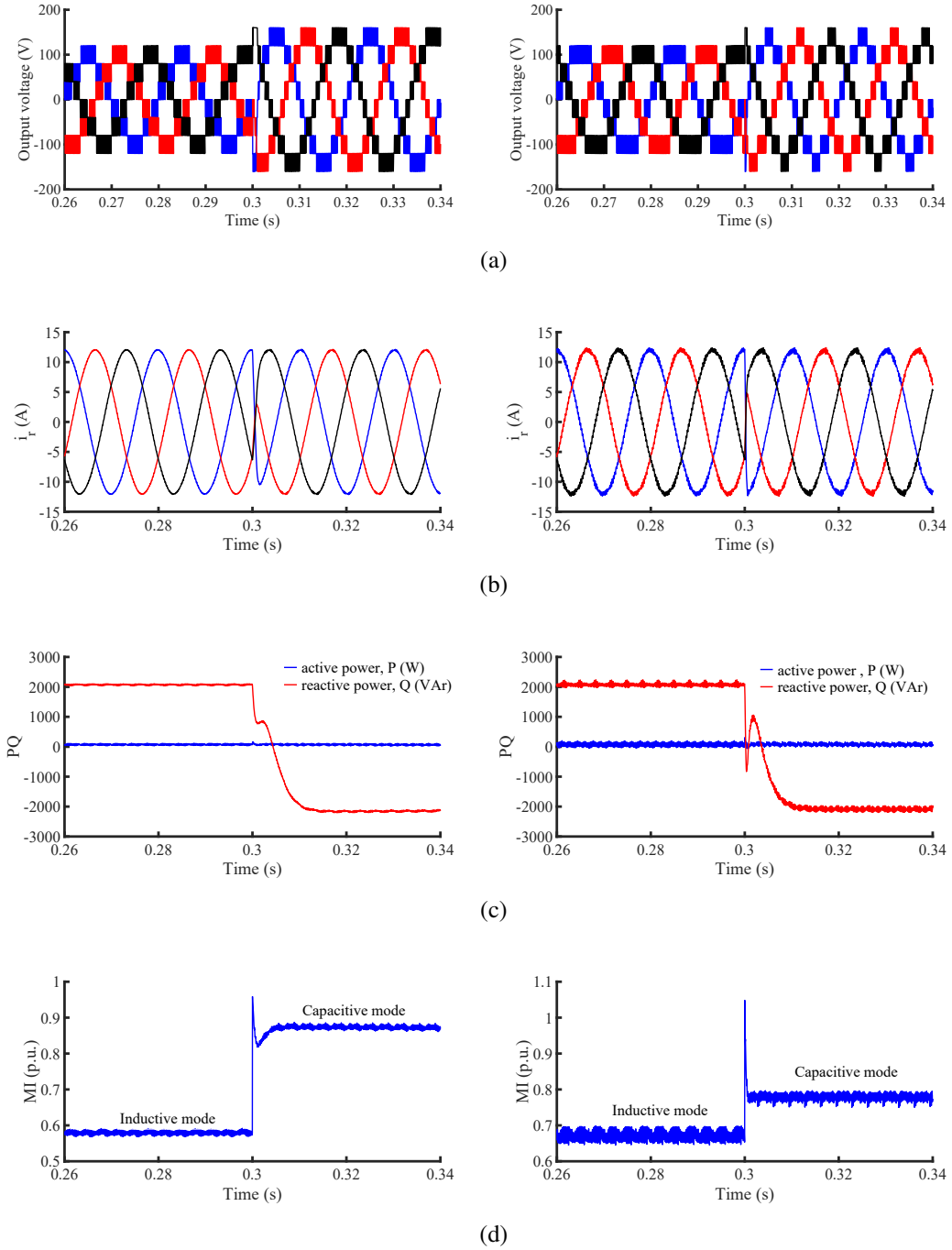


Figure 3.7: Effects of the inductance on the range of operation of STATCOM (a) output voltage (b) phase current (c) active and reactive powers (d) M_I

3.5 Number of Levels and Harmonics Performance

The ultimate goal in the design of STATCOMs is to generate a fully controllable sinusoidal current that allows the reactive power exchange with the grid. Furthermore, the harmonics should comply with IEEE 519-1992 standards, which normally requires the harmonics of the line current to be less than 5%. This can be achieved by proper utilization of PWM method and a careful design of input filter. In addition, to operate D-STATCOM with direct control scheme (based on control of M_I value), PWM methods become indispensable. The main PWM techniques (i.e. PS-PWM and HEPWM) are elaborated in the followed sections. Among PWM modulation techniques, SPWM is the most popular method applied to control the power inverters. To generate the gate signals for the switches, a sinusoidal reference waveform is compared with a triangular carrier waveform and the intersection between them produces the required pulses. In high power applications, power dissipation is crucial issue. Thus, fundamental frequency SPWM was proposed to minimize the switching losses. For multilevel inverters, the multi-carrier SPWM methods have been implemented to increase their performance; and they have been classified according to the vertical and the horizontal arrangements of the carrier signals. Among the vertical carrier distribution techniques, the Phase Dissipation (PD), Phase Opposition Dissipation (POD), and Alternative Phase Opposition Dissipation (APOD) are popular, while, for the horizontal arrangement, the phase shifted (PS) technique is well-defined. In fact, PS-PWM is only useful for cascaded H-bridges and flying capacitors, while PD-PWM is more useful for NPC. PS-PWM method has been extensively utilized for cascaded H-bridge MVSI based D-STATCOM. It is an extension of the traditional SPWM methods. The switching pattern of each H-bridge is determined from two comparisons of low-frequency reference waveform (i.e. modulation) and high-frequency triangular signal (i.e. carrier). The intersection between the two signals generates the required driving pulses for the switches. For MVSI based D-STATCOM, N triangular-carrier signals are required with a phase shift of $(180/N)$ for each cell where N is the number of H-bridge units in each phase.

For PS-PWM based D-STATCOM, the lower order harmonics of the output voltage are shifted to a higher frequency by increasing the MVSI switching frequency. By increasing the number of levels in the inverter, the output voltages have more steps in generating a staircase waveform, which has a reduced harmonic distortion. However,

a larger number of levels increase the number of devices that must be controlled and the control complexity. At present, there are no commercial digital signal processors (DSPs) having appropriate built-in pulse width modulation (PWM) units that are enough to control the large number of switches used by multilevel converters. A software implementation of these PWM units is very time-consuming. Therefore, a fast and expensive DSP is needed to carry out the modulation and the control processes. An architecture where one field programmable gate array (FPGA) carries out the modulation task and one DSP implements the control strategy is better suited for multilevel converters. Thus, cheap DSP and FPGA are needed.

The generation of the switching pulses using PS-PWM is depicted in Fig. 3.8. To generate the switching pulses, first, the suitable M_I value is determined. The M_I value is used to determine the amplitude of the modulation signal. Then, the triggering pulse for each H-bridge is determined by comparing the modulation with carrier signals. For instance, for 23-level MVSI, eleven triangular carriers are phase shifted by (180° / 11) for each cell.

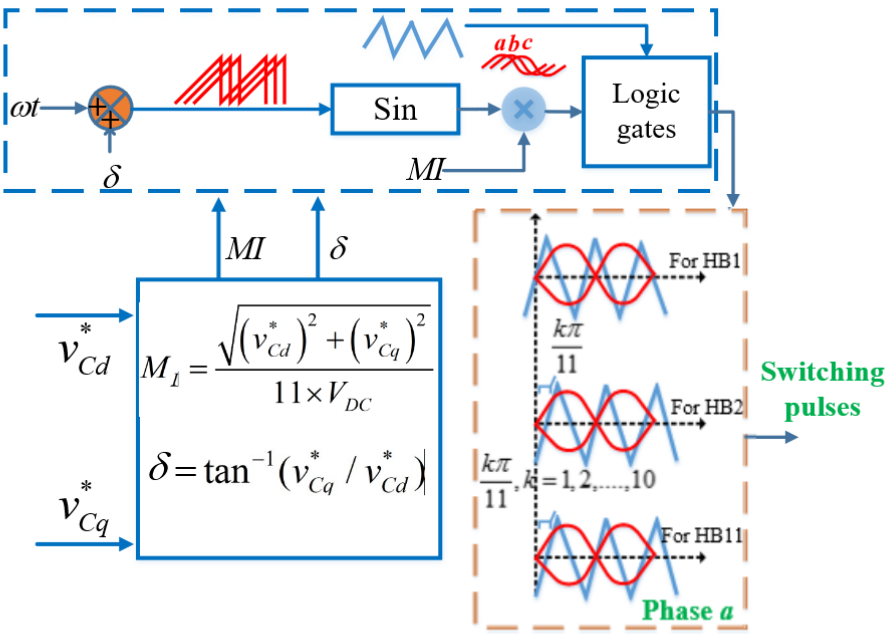
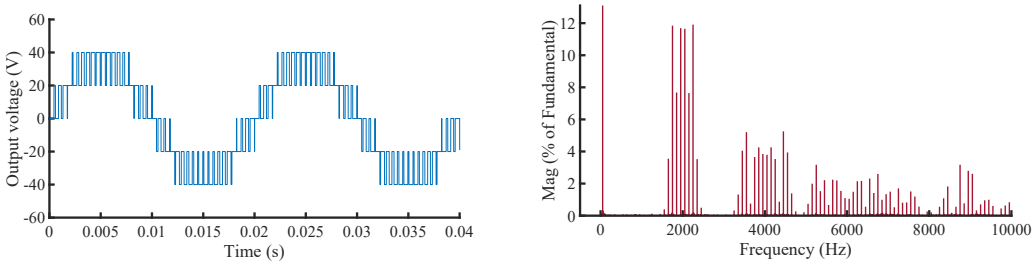


Figure 3.8: Generation of the switching pulses using PS-PWM

To evaluate the harmonics performance, the simulated output voltage waveforms are captured. Fig. 3.9, Fig. 3.10 and Fig. 3.11 show the harmonic spectra of the line-to-neutral voltage for 5-level, 7-level and 9-level SSBC with 500 Hz and 1 kHz switching frequencies. As shown, as the switching frequency increases, the harmonic clusters are shifted to a higher level. Thus, For higher number of levels, harmonics standard (i.e. THD < 5%) can be accomplished with low switching frequency. This is advantages specially in high power application as increasing the switching frequency is not desirable due to the high switching losses that result.



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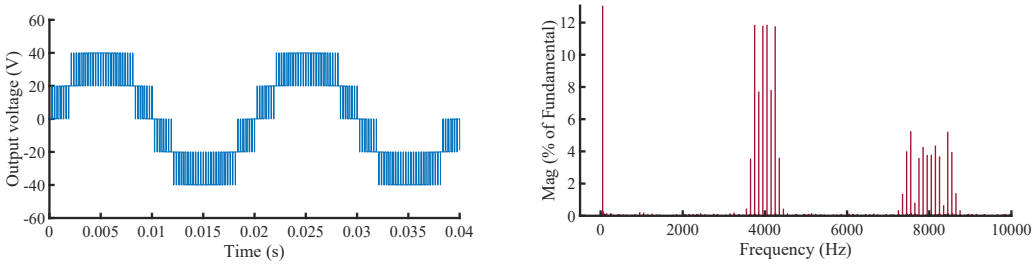
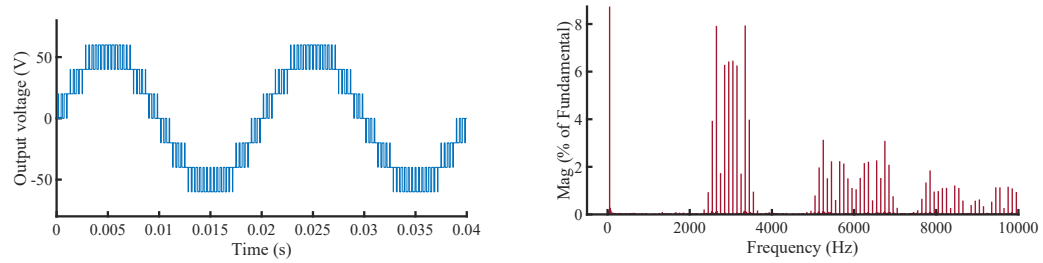


(b)

Figure 3.9: The simulation results: output voltage waveforms and frequency spectra for 5-level SSBC with switching frequency of (a) 500 Hz (b) 1 kHz



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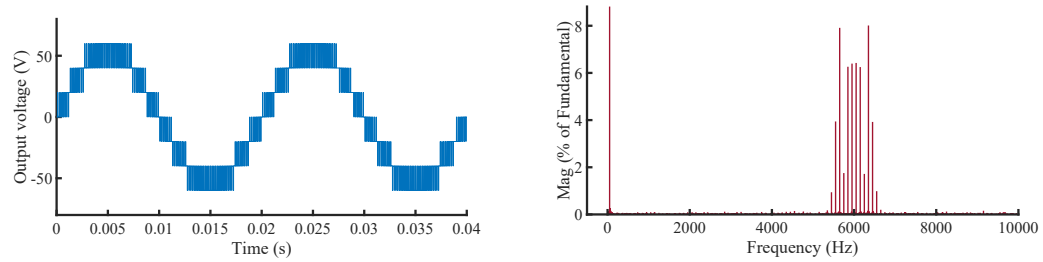
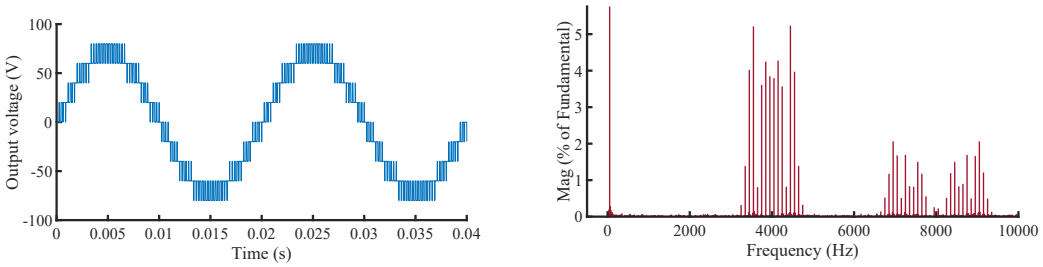


(b)

Figure 3.10: The simulation results: output voltage waveforms and frequency spectra for 7-level SSBC with switching frequency of (a) 500 Hz (b) 1 kHz



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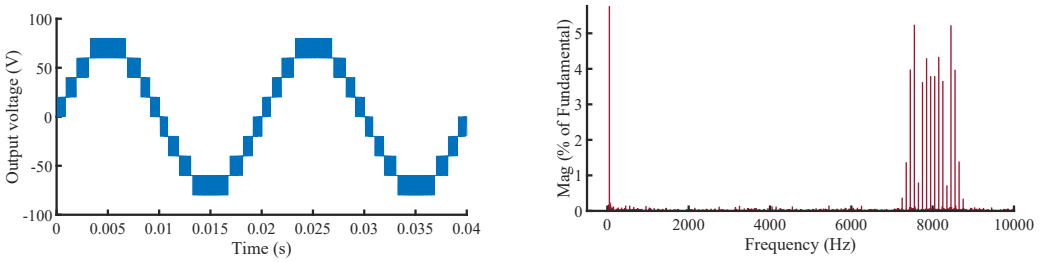
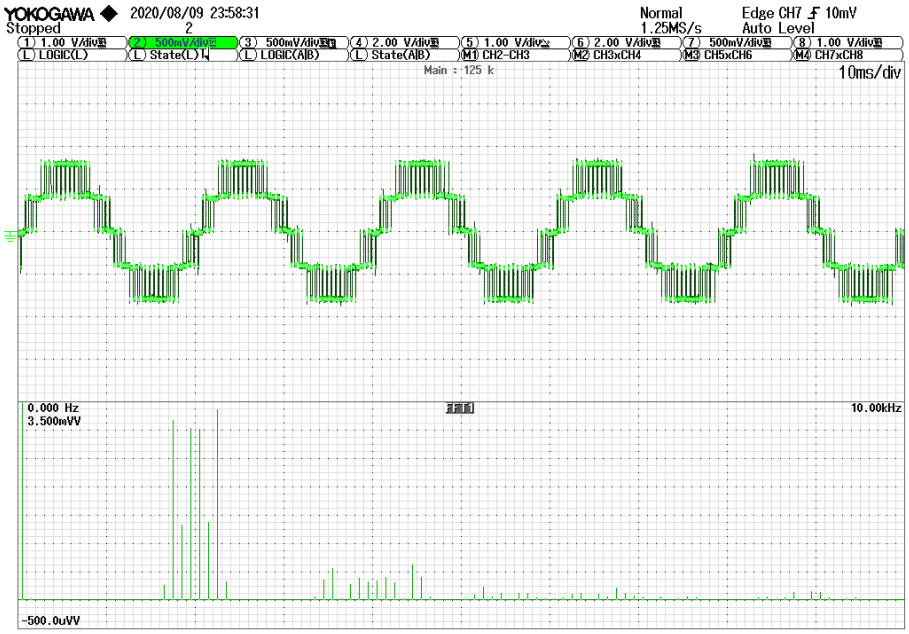


(b)

Figure 3.11: The simulation results: output voltage waveforms and frequency spectra for 9-level SSBC with switching frequency of (a) 500 Hz (b) 1 kHz

A three-phase 9-level MVSI test rig is also developed to practically validate the simulation results. The hardware prototype, design concept and strucutre are explained in detailed in Section 3.7. The fundamental frequency is 50 Hz and the input dc voltage source for each H-bridge is set to 40 V. In addition, the timing of the pulses is created using the QUARTUS II software, which is programmed in VHDL, while the ALTERA Cyclone® V FPGA is utilized to generate the gate drive signals. The output voltages and their frequency spectra are analyzed using Yokogawa DLM4058 oscilloscope.

The oscilloscope-waveforms of the phase voltages and their harmonics spectra for the same M_I values (0.9 p.u.) with 500 Hz and 1 kHz switching frequencies are presented in Fig. 3.12, Fig. 3.13 and Fig 3.14. It is observed that the low order harmonics are eliminated from the phase voltage harmonics spectra with the first cluster appears as $(2N \times f_{sw})$. This is consistent with the simulation results.



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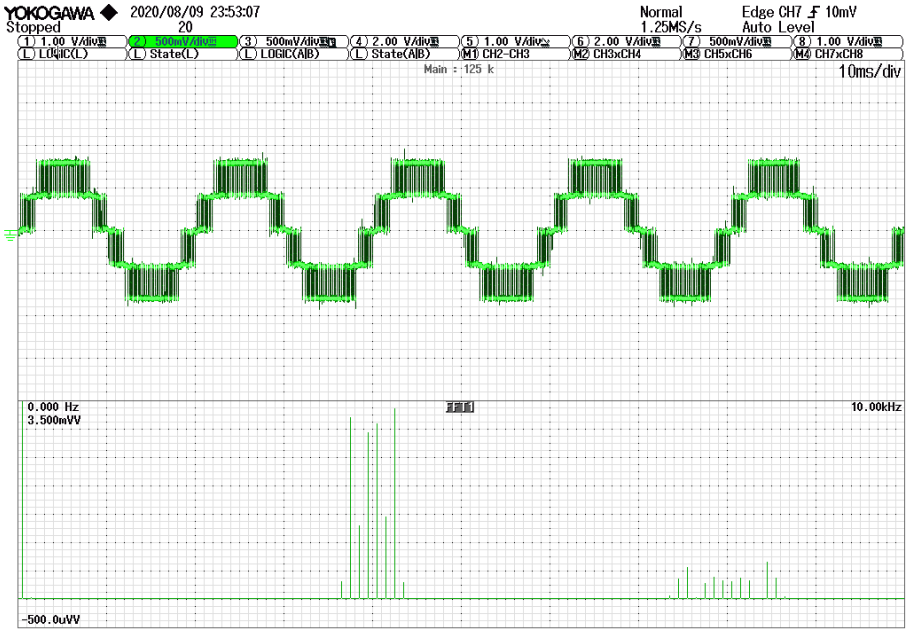
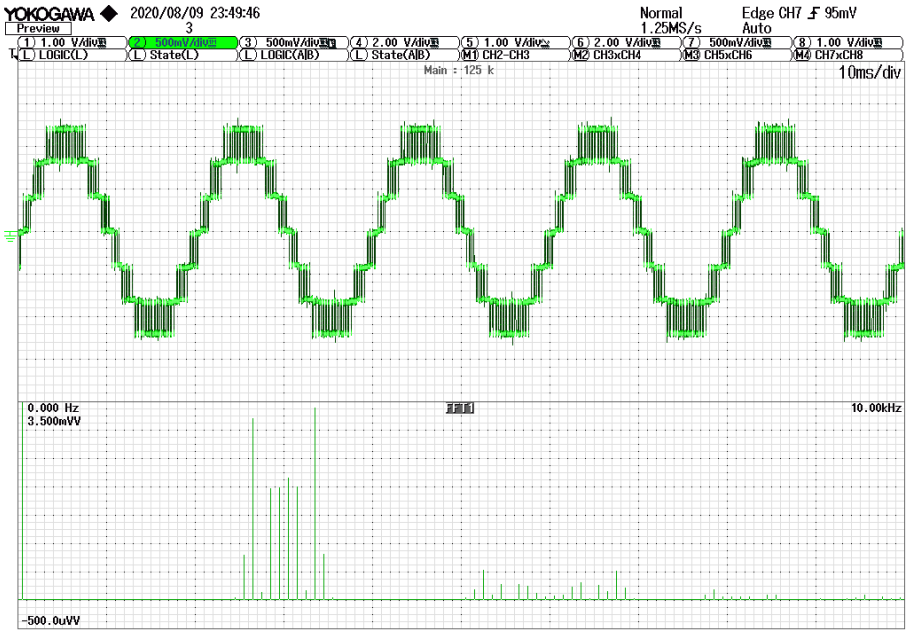
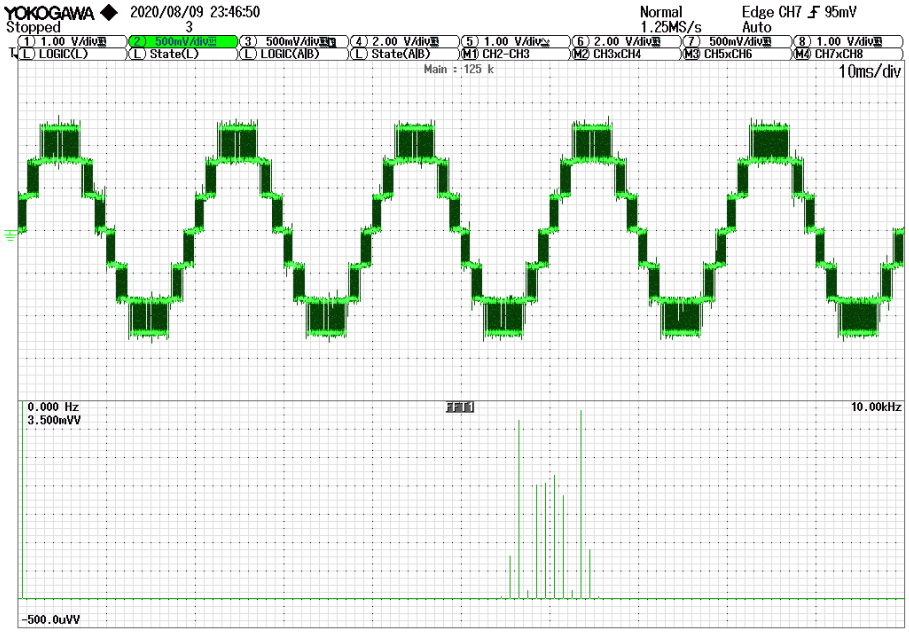


(b)

Figure 3.12: The experimental results: output voltage waveforms and frequency spectra for 5-level SSBC with switching frequency of (a) 500 Hz (b) 1 kHz

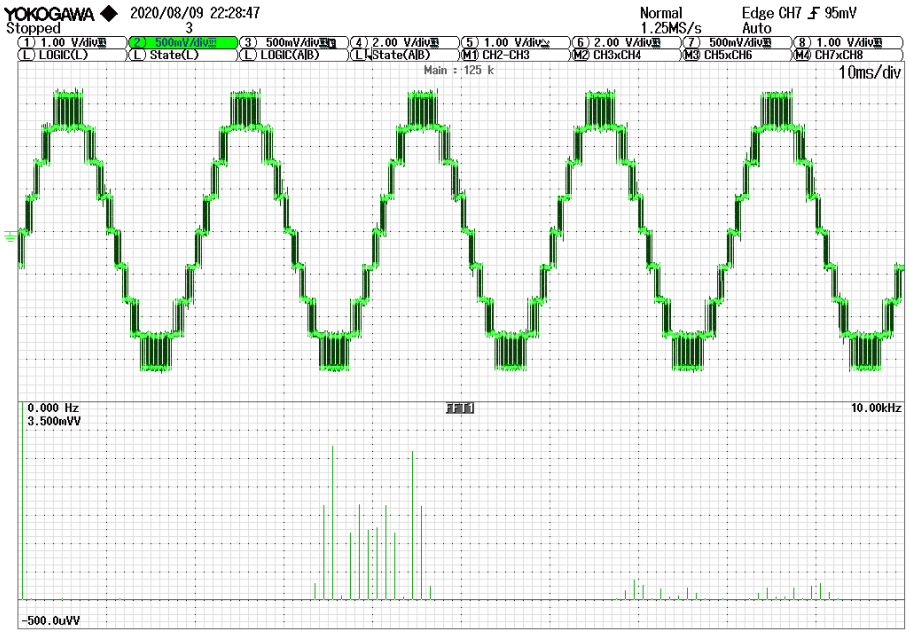


(a)

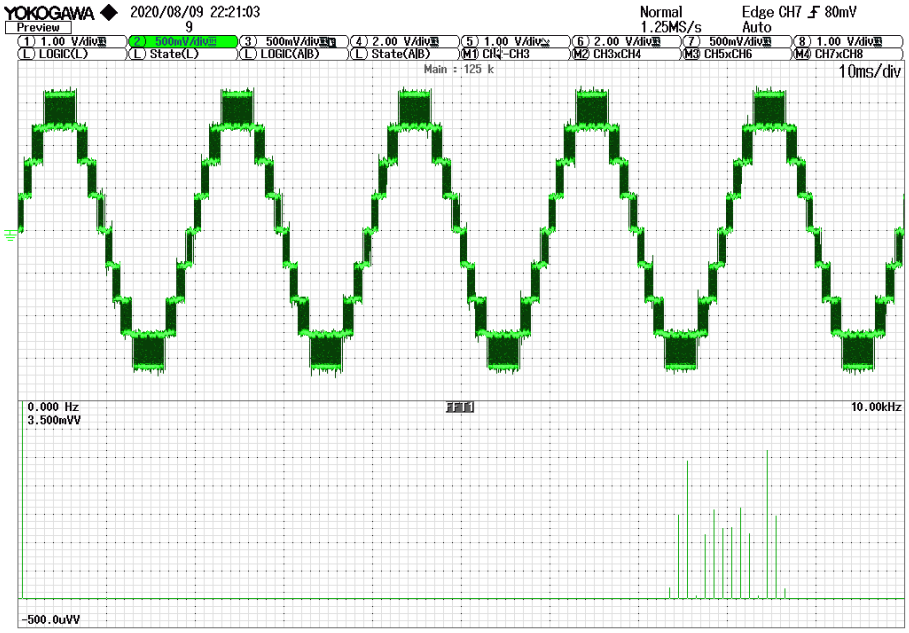


(b)

Figure 3.13: The experimental results: output voltage waveforms and frequency spectra for 7-level SSBC with switching frequency of (a) 500 Hz (b) 1 kHz



(a)



(b)

Figure 3.14: The experimental results: output voltage waveforms and frequency spectra for 9-level SSBC with switching frequency of (a) 500 Hz (b) 1 kHz

3.6 Cost Analysis

Overall cost of STATCOM is divided into installation and operation and maintenance costs. In this work, the impact of number of levels on the implementation cost of SSBC STATCOM is analyzed by highlighting the most effective factors in both low and medium voltage applications. Two case studies (i.e. 400 V and 11 kV systems) were considered. The components' costs for each case are obtained based on the best available electronic components distributors' prices with optimal consideration of the available quantities for per-unit cost.

Table 3.4: Voltage and capacitance design for 400 V and 11 kV systems

Number of levels (N)	**400 V**		**11 kV**	
	Input voltage (V_{DC})	**Required capacitance**(C)**, 30 A**	**Input voltage** (V_{DC})	**Required capacitance** (C)**, 100 A**
7-level	123.1 V	3.88 mF	3.4 kV	0.45 mF
13-level	61.58 V	7.75 mF	1.7 kV	0.94 mF
23-level	33.6 V	14.21 mF	0.9 kV	1.73 mF
33-level	23.1 V	20.67 mF	0.635 kV	2.51 mF

Table 3.5: Cost for AVX and TDK Capacitors from Mouser Electronics Company

AVX Capacitors	**TDK Capacitors**
FFLI6B1907KJE (800 V, 1.9 mF), € 292,85	B25620B0158K883 (900 V, 1.5 mF), € 159,24
FFLI6U1607K (1.2 kV, 1.6 mF), € 247,16	B25620B1297K982, (1.98 kV, 0.295 mF), €102
FFLI6B3007KJE (800 V, 3mF), € 398,26	B25620B1427A101, (1.1 kV, 4.2 mF), € 53,85
FFLI6U1307KJE (1.2 kV, 1.3mF), € 217,22	B25620B0158K883 (1.5mF, 900V), € 150,49
FFLI6B1907KJE (800 V, 1.9 mF), € 292,85	

Different SSBC levels were considered in this design, namely 7, 13, 23 and 33. For each system, the corresponding switches and capacitors were selected (Table 3.4). Infineon Technologies switches with the same characteristics (package, temperature, mounting style) were considered. Their models were simulated in PSPICE to calculate power losses and hence design required heatsinks. They were operated under same overall switching frequency (18.9 kHz) using PS-PWM. Therefore, switching frequency of each component is different as well as corresponding losses. Based on calculated thermal resistances, aluminum heatsinks from Aavid were selected [129]. ALS30 Aluminum Electrolytic capacitors from KEMET with 20% tolerance were selected in which their ESR values were assured to be small to reduce their impacts on the lifespan

of the capacitors. Isolated gate drivers were considered in this analysis in which the high-CMTI ISO5852S Texas Instruments driver (2.5-A source and 5-A sink current) was used. A € 20 is estimated for dual isolated gate driver board.

Similarly, based on the input voltages and capacitance values (Table 3.4), IGBTS modules and capacitors for 11 kV STATCOM were selected. Infineon IGBT modules supplied by Arrow Electronics Company and capacitors supplied by Mouser Electronics Table 3.5 were considered. For reliable cost estimation of the capacitors, two designs were conducted based on AVX and TDK components. It is worth mentioning that film capacitors are preferable to electrolytic capacitors for DC input applications due to their high reliability and lifetime [130]. For high voltage application, film capacitors are available with high voltage and capacitance values which allows using lower number of components for each H-bridge units, while much higher number of parallel and series components are required in case of electrolytic capacitors which, in turn, severely affects system performance and reliability. Therefore, in this analysis, film capacitors were considered. Gate driver design is another key factor that affects system performance. Main requirements for gate drivers in medium voltage applications are high current capability, overvoltage protection and galvanic isolation between IGBT modules and control electronics circuits. Considering these aspects, SCALE Power Integrations gate drivers were selected for different modules [131]. The selected devices and their prices are listed in Table 3.6 and Table 3.7 for 400 V and 11 kV respectively.

3.6.1 Results and Discussion

Fig. 3.15 and Fig. 3.16 compare components' cost for different multilevel STATCOM in 400 V and 11 kV system. The overall cost of the system reduces with higher number of levels in 11 kV STATCOM, while it increases in low voltage due to higher number of gate drivers and sensors.

As demonstrated in Fig. 3.15, a higher number of levels results in a reduction of heatsink cost due to the low-frequency operation. In addition, the cost of the switches is reduced to some level limits. The high increase in cost for higher levels is due to the driving and sensing requirements. Therefore, reducing their cost will encourage the utilization of higher-level STATCOM for low voltage applications. In

Table 3.6: Component selection for different levels of 400 V SSBC STATCOM

Level	MOSFET	P_D (W)	θ_{thjc} (°C/W)	θ_{thsa} (°C/W)	Heatsink	Capacitor
33-level	IPP80N04S4-03 40 V, 80 A (€ 0,763 for 100 units , € 0,533 over 1000)	1.5	1.6	61.23	Not strictly required	ALS30A223DE022 mF, 40 V (€ 9,54 per 50 units)
23-level	IPP037N06L3 G 60 V, 90 A (€ 0,886 for 100 units, € 0,64 over 1000)	2.5	0.9	36.6	577002B04000G 32°C/W, (€ 0,43390 for 100 units)	ALS30A153KE015 mF, 63 V (€ 13,40 per 50 units)
13-level	IPP076N12N3 G 120 V, 100 A (€1,53 for 100 units, € 1,11 over 1000)	10	0.8	8.2	531202B02500G 7.50°C/W, (€ 0,88500 for 100 units)	ALS30A103KE100, 10 mF, 100 V (€ 19,93 price per 20 units)
7-level	IPP220N25NFDAKSA1 250 V, 61 A (€3,90 for 100 units , € 2,80 over 1000)	1.75	0.3	3.56	6400BG 2.70°C/W, (€ 1,90860 for 50 units)	ALS30A472MF250, 4.7 mF, 250 V (€ 29,45 price per 10 units)

this analysis, however, the high-cost isolated gate drivers are considered. In [132, 133], successful implementation of low-cost bootstrap charge pump drivers for three-level NPC inverters is demonstrated. Therefore, if such drivers are successfully used in high multilevel systems, a significant reduction of the overall cost will be achieved.

In medium voltage applications, with increasing the number of levels, IGBT modules and capacitors costs exhibit decremental effect on the total cost. Although driver cost has no significant effect on overall STATCOM cost of STATCOM compared to others (switches and capacitors cost), it also exhibits lower cost with 33-level (i.e. € 1,468.80). Therefore, this analysis emphasizes the advantages of increasing the number of levels in medium voltage applications.

It is worth noting that snubber circuit and electrical and mechanical layout might have serious impact on overall cost of the systems. In addition, a compromise between filtering requirement and operating switching frequency is another interesting factor that should be investigated to come up with comprehensive cost estimation of

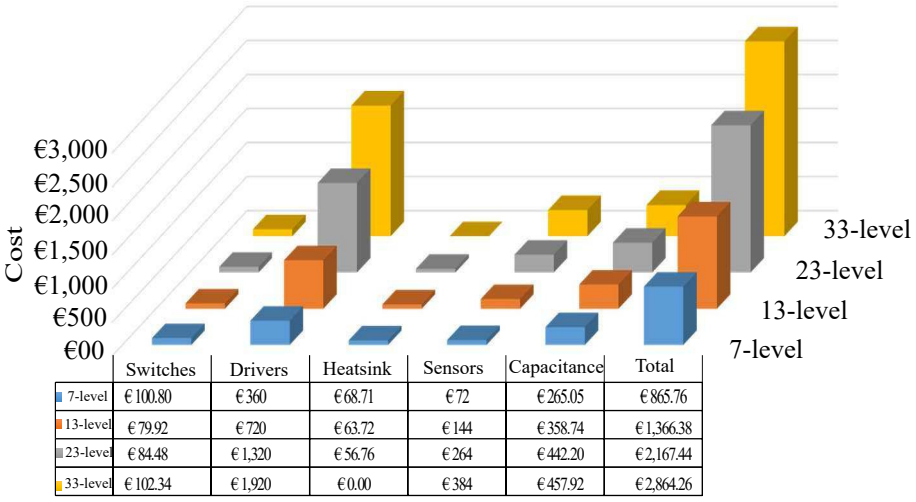
Table 3.7: Cost comparison with different levels for 11 kV SSBC STATCOM

Level	Module	Gate drivers	Capacitors (based on FFLI/AVX capacitors)	Capacitors (based on EPCOS/TDK capacitors)
7-levels (V_{DC} = 3.4 kV)	FZ600R65KE3, 6.5 kV, 600 A, Single switch configuration (€ 1.724,83 per 1 unit)	1SC0450E2A0-65 (€ 115,92 per 48 units)	FFLI6B1907KJE (8 units ×2 units) (16 ×€ 267,71)	B25620B0158K883 (7 units ×3 units) (21 ×€ 151.32)
13-levels (V_{DC} = 1.7 kV)	FF400R33KF2CNOSA1, 3.4 kV, 660 A, dual configuration (€ 954.25 per 60 units)	2SC0535T2A1-33 (2 in one board) (€ 125,58 per 40 units)	FFLI6U1607K (3 units ×3 units) (9 ×€ 222,93)	B25620B1297K982 (7 units) (7 ×€ 102,66)
23-levels (V_{DC} = 0.9 kV)	FF450R17ME4BOSA1, 1.7 kV, 600 A,dual configuration (€ 158.7389 per 10 units)	2SC0108T2H0-17 (2 in one board) (€ 28,59 per 100)	FFLI6B3007KJE (2 units) (2 units ×€ 317,24)	B25620B1297K982 (6 units) (6 ×€ 102,66)
33-levels (V_{DC} = 0.635 V)	FF450R12KT4HOSA1, 1.2 kV, 580 A,dual configuration, €106.06 per 10 units	2SC0106T2A1-12 (2 in one board) (€ 15,30 per 100 units)	FFLI6U1307KJE (2 units) (2 units×€ 195,92)	B25620B1427A101 (6 units) (6 ×€ 51,87)

different multilevel design. Furthermore, the modular design of the converter is an advantage in term of reliability and, in some aspects, in cost reduction. However, reliability and hence operation and maintenance costs of different multilevel design might give different indicators. These aspects are not considered in this work. The analysis is restricted to component cost investigation in which it highlights important factors design and their effects on selection of number of level in medium and low voltage applications.

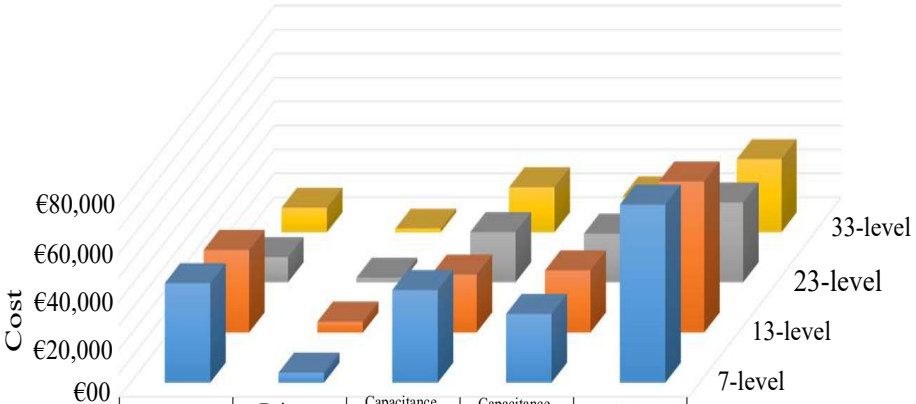
3.7 Hardware Design for 142 V SSBC-STATCOM

A three-phase 9-level SSBC STATCOM test rig was designed which is a subset from a three-phase 33-level MMCC system constructed in DigiPower. The whole project has been developed to realize a system with a very high level of modularity and flexibility.



	Switches	Drivers	Heatsink	Sensors	Capacitance	Total
7-level	€ 100.80	€ 360	€ 68.71	€ 72	€ 265.05	€ 865.76
13-level	€ 79.92	€ 720	€ 63.72	€ 144	€ 358.74	€ 1,366.38
23-level	€ 84.48	€ 1,320	€ 56.76	€ 264	€ 442.20	€ 2,167.44
33-level	€ 102.34	€ 1,920	€ 0.00	€ 384	€ 457.92	€ 2,864.26

Figure 3.15: Cost comparison with different levels for 400V SSBC STATCOM

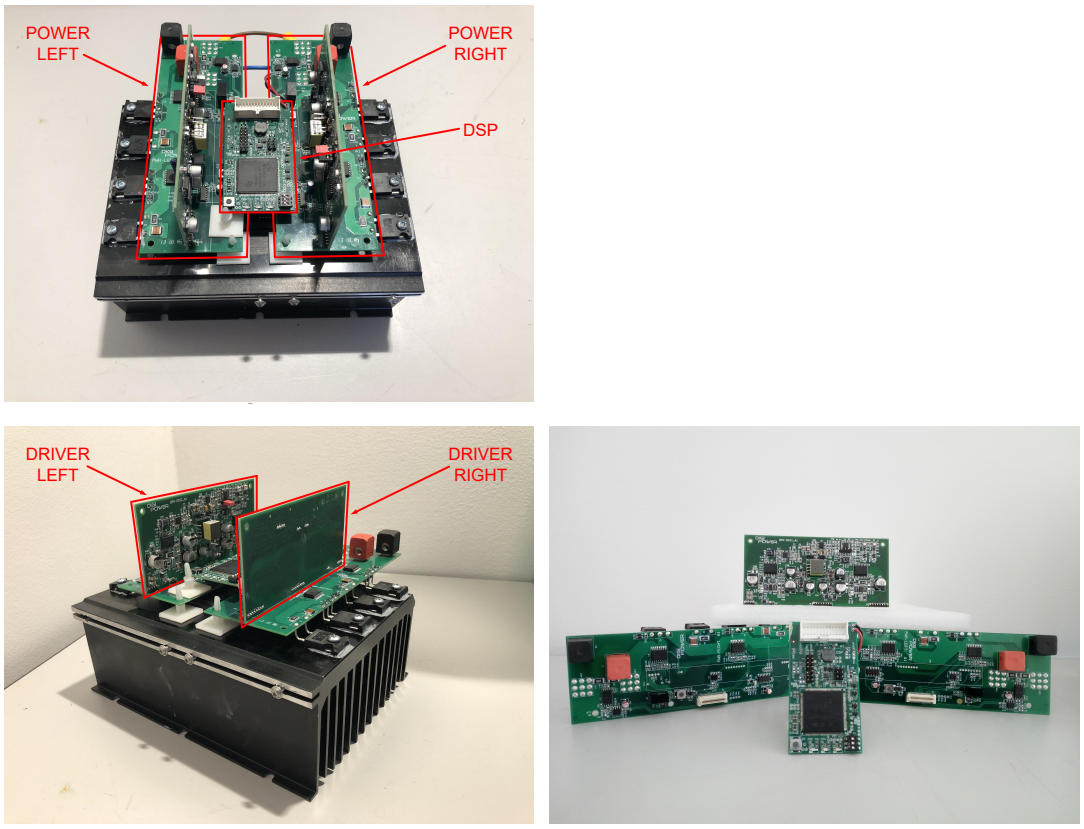


	Switches	Drivers	Capacitance (AVX)	Capacitance (TDK)	Total (AVX)
7-level	€ 41,395.92	€ 4,173.12	€ 38,550.20	€ 28,599.50	€ 74,168.54
13-level	€ 34,353.00	€ 4,520.88	€ 24,076.40	€ 25,870.30	€ 62,950.28
23-level	€ 10,476.76	€ 1,886.94	€ 20,937.80	€ 20,326.68	€ 33,301.50
33-level	€ 10,233.60	€ 1,468.80	€ 18,808.30	€ 14,938.56	€ 30,510.70

Figure 3.16: Cost comparison with different levels for 11 kV SSBC STATCOM

3.7.1 H-Bridge Converter

The H-bridge module is the perfect candidate to implement this idea. Each H-bridge converter can be used separately or as part of the multilevel system. It has all the features of a standard power converter module. Each unit consists of four power switches, associated snubber circuits, overcurrent and overvoltage protection, and input voltage and output current measurements. The designed H-bridge module is shown in Fig. 3.17a while its parts are shown in Fig. 3.17b. The nominal operating conditions of the H-bridge module are listed in Table 3.9.



(a) (b)

Figure 3.17: (a) H-bridge converter (b) parts of the converter module (i.e. power boards, gate driver, DSP)

Using an H-bridge module for a multilevel system allows easy connection to the other modules using plug-in input and output power connectors. In this configuration, the DSP board becomes a slave for the master control board (combined with FPGA and DSP). The two logic units are connected through the I/O pin connector, located at the top of the DSP board. The exchanged signals between the mainboard and the local slave DSP when the multilevel configuration is used are the gate signals, voltage and current measurement, synchronization signal, and fault and reset signals.

Table 3.9: nominal operating conditions H-bridge module

Parameter	Value
V_{DCnorm}	600 V
I_{norm}	35 A
f_{sw}	10 kHz
T_{max}	100°C
η_{norm}	99 %

SSBC is built by stacking a number of H-bridge (each with its own isolated *dc* source) to form a stepped output waveform. By increasing the number of H-bridges, more output steps are synthesized, resulting in higher output voltage. The design and selected of the components should consider the effect of the harmonic of connecting the STATCOM system to the PCC, hence, after determining the voltage and current rating of the system, maximum stresses on all STATCOM's components can be determined. Accordingly, considering the worst cases, the passive and active components can be selected.

3.7.2 Control Board

The huge complexity of the system requires more computational capability and A general-purpose input/output (GPIO) availability than any commercial FPGA device. For this reason, the main control board is equipped with an FPGA, a A complex programmable logic device (CPLD) and a DSP device that cooperates to satisfy the system requirements. A block diagram of the proposed solution is shown in Fig. 3.18 and a summary of the main tasks of each module are listed below:

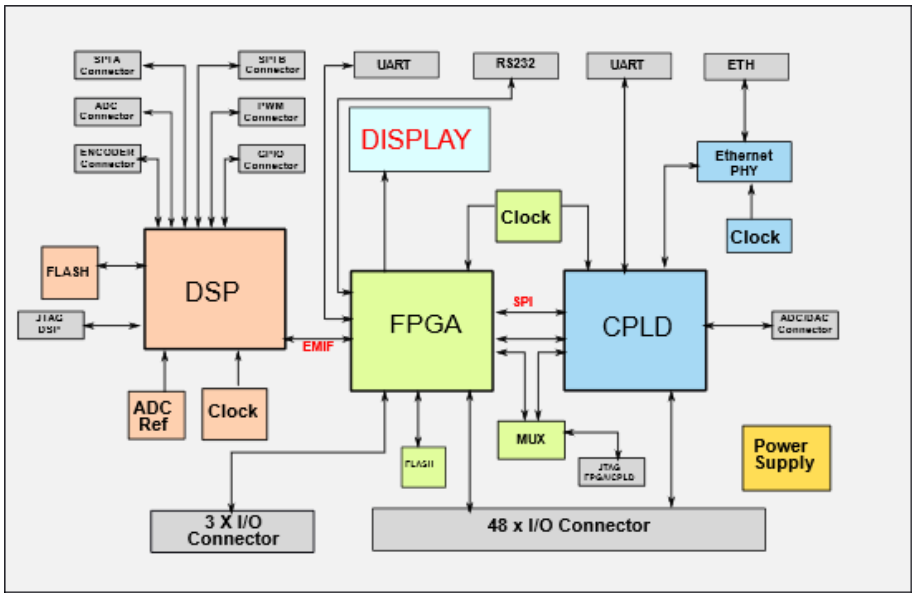


Figure 3.18: Block diagram of the main control board

1. The FPGA is in charge to collect all the measurement and status information that comes from the system and to compute the control algorithm for the required application. In the specific case of proposed prototype, the FPGA is computing a STATCOM control algorithm. The tasks of the FPGA device are listed in detail below:

   (a) It receives through SPI interface the current and voltage measurements of the power grid. This informations are then used to compute the control algorithm of the system.

   (b) It receives through SPI interface the measurements of the *dc*-bus voltages of each H-bridge in the three phases. These values are then used together with the information received from the phase A and B to compute a DC voltage balancing control algorithm. It is necessary to avoid any kind of voltage unbalancing in the DC links of the H-bridge modules.

   (c) It generates a synchronization signal called “time tick” with is sent to the CPLD. This signal is forwarded to all H-bridge units which is necessary to keep the right synchronism in the whole system.

(d) It manages the alarm of the system. Each H-bridge can send an alarm signal when a fault occurs and the FPGA can identify the problem and can decide to disconnected the damaged H-bridge module or turn-off the whole system.

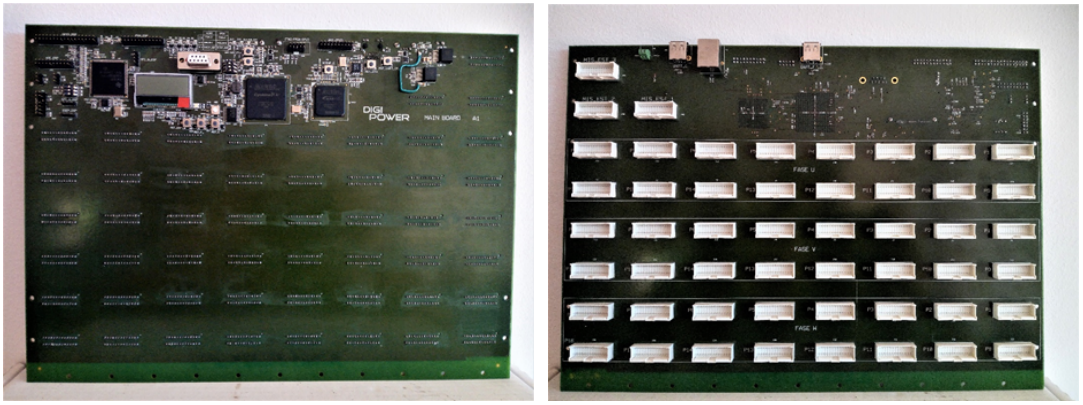
(e) When a problem related to a fault signal results in a false alarm or in a temporary problem (e.g. a lose of synchronization). The FPGA can send a reset command to the involved H-bridge module.

(f) It manages a memory interface with the DSP, which provide to the FPGA the information required for the synchronization of the output voltage of the system with the power grid.

2. The CPLD has the role of GPIO expander for the FPGA device. FPGA pinout is not able to satisfy alone the huge number of required output signals (switching command patterns, synchronization signals, reset signals etc.).

3. The DSP architecture, which is optimized for the operational needs of digital signal processing, is exploited to compute PLL algorithm in order to synchronize the output of the SSBC converter with the power grid voltage waveform. The information extracted from the power grid measurements by the DSP is sent to the FPGA, which uses it as an input parameter for the control algorithm.

The prototype of the main control board is shown in Fig. 3.19a and in Fig. 3.19b, respectively in the top and bottom view. On the top view it is possible to observe the three logical devices: the FPGA, the CPLD and the DSP. On the bottom are mounted the 48 connectors where each H-bridge module is connected through its own cable, allowing the exchange of all the data and the modulation patterns.



(a) (b)

Figure 3.19: Main control board (a) top view (b) bottom view

3.8 Summary

Multilevel inverters successfully replaced traditional VSI in many applications. However, it is still ambiguous the optimal choice of number of levels for each application. As cost and reliability are the main detrimental factors, this study highlights component cost-effectiveness of different levels for 400 V and 11 kV STATCOMs. It is shown that higher number of levels increases the cost in 400 V due to the cost of gate drives and sensors. In contrast, for medium voltage applications, it is recommended to go for high levels as the cost is dramatically decreased. It should be mention that it is also important to study the snubber circuit, mechanical and electrical layout, and filter designs to comprehensively investigate the optimal design of levels from cost point of view. In addition, reliability and hence operation and maintenance costs are essential factors that should be considered too. These will be directions for further investigation.

CHAPTER 4

CONTROL DESIGN AND IMPLEMENTATION OF SSBC STATCOM

4.1 Introduction

Modular multilevel converters prove to be well-suitable for high and medium voltage systems due to their lower cost and high-redundance design. For STATCOM, Single-Star Bridge-Cell (SSBC) topology is well applied for its satisfactory performance and superior component count. Multilevel SSBC-STATCOM control is composed of three layers which are output voltage control, internal current control, and capacitor voltage balancing. Although PI regulators are commonly used for its simplicity and ease in implementation, STATCOM system is an essentially nonlinear system, therefore, a nonlinear controller can effectively improve performance and robustness. In this work, a backstepping nonlinear control based on Lyapunov function design is proposed to regulate the overall capacitor voltage. Besides, detailed control design and implementation of the proposed control of SSBC-STATCOM using FPGA is discussed. Experimental set-up was designed to verify the results practically which confirmed the robustness and stability of the proposed control approach. In addition, the performance of the proposed method under V_{dc} step change and variation of system impedance has been analyzed and results were compared with the traditional PI controller.

4.2 SSBC STATCOM System

4.2.1 System Dynamics

The system under study is shown in Fig. 4.1 and consists of a SSBC connected in parallel with the grid through a coupling inductor L_{ac} and converts dc input voltages $(v_{x1}, v_{x2}...v_{xn}, where\ x = a, b, c)$ to balanced three phase voltages (v_{ra}, v_{rb}, v_{rc}) with controllable magnitude (M_I) and phase angle (δ). The voltage difference across L_{ac} creates the reactive power (Q) exchange between the STATCOM and the grid. In the inductive mode operation, STATCOM absorbs Q by making magnitude of $v_{rx} < v_{gx}$, during the capacitive mode the magnitude of $v_r > v_g$ a Q is injected in the grid.

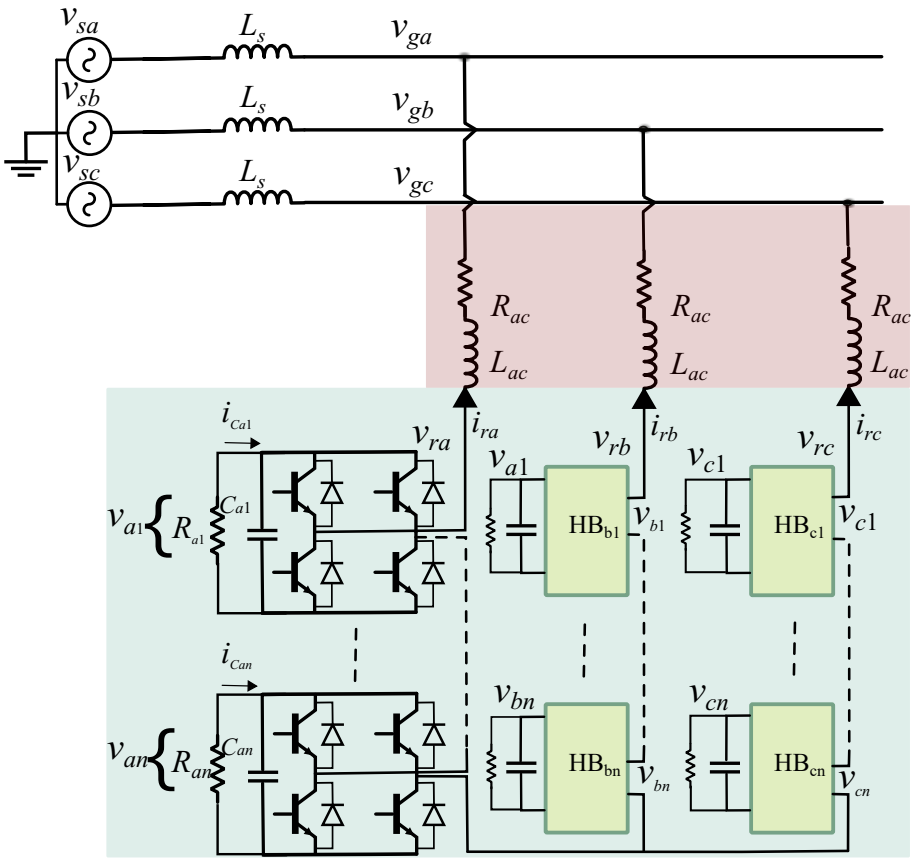


Figure 4.1: Three-phase SSBC based STATCOM

4.2.2 STATCOM Model

To develop model of SSBC based STATCOM, the process starts by extracting switching model of the converter in abc coordinates then, due to complexity to analyse system based on its switching form, a simplified model is obtained using $dq-$frame transformation. This allows for easier design and implementation of the controller. By assuming capacitor voltages are well−balanced through sub−layers controllers, SSBC STATCOM model can be represented by 4.2.

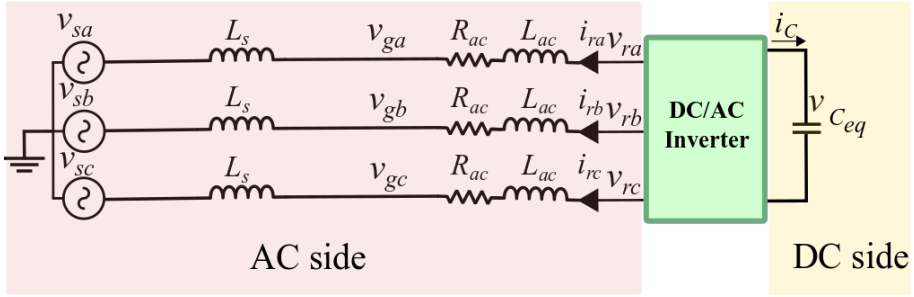


Figure 4.2: Three-phase average model of STATCOM

The $ac-$side dynamic of the STATCOM can be derived using first-order differential equations in the $abc-$frame, i.e. [89].

$$L_{ac}\frac{di_{r,abc}\,(t)}{dt} + R_{ac}i_{r,abc}\,(t) = v_{g,abc}\,(t) - v_{r,abc}\,(t) \tag{4.1}$$

Applying abc/dq transformation,

$$v_{rd} = v_{gd} - L_{ac}\frac{di_{rd}}{dt} + L_{ac}\omega i_{rq} - R_{ac}i_{rd} \tag{4.2}$$

$$v_{rq} = v_{gq} - L_{ac}\frac{di_{rq}}{dt} - L_{ac}\omega i_{rd} - R_{ac}i_{rq} \tag{4.3}$$

where ω is the system frequency (rad/s). According to the instantaneous power theory, the injected active and reactive powers can be calculated as

$$P = v_{gd}i_{rd} + v_{gq}i_{rq}, \qquad Q = -v_{gd}i_{rq} + v_{gq}i_{rd} \tag{4.4}$$

where $\left(v_{rd}, v_{rq}, v_{gd}, v_{gq}\right)$ and $\left(i_{rd}, i_{rq}\right)$ are the projection values of the voltage and current vectors in dq reference frame. Choosing d-axis in phase with v_g, leads to v_{gq} is equal to zero . Hence, the active and reactive power at the ac-side of the system can be written as

$$P = v_{gd}i_{rd}, \qquad Q = -v_{gd}i_{rq} \tag{4.5}$$

According to active power balance, the instantaneous power at the $ac-$and $dc-$terminals of the inverter are equal. Considering small value of R_{ac}, the dc-side model can be written as

$$v_{gd} i_{gd} = v i_{dc} \tag{4.6}$$

$$\Rightarrow \frac{dv^2}{dt} = \frac{v_{gd} i_{rd}}{C_{eq}} \tag{4.7}$$

The system model is assumed to be lossless as capacitor voltages are assumed to be balanced by means of balancing control. From (4.2), (4.3) and (4.7), the dynamic model of STATCOM can be arranged as

$$\begin{aligned} \frac{di_{rd}}{dt} &= -\frac{R_{ac}}{L_{ac}} i_{rd} + \omega i_{rq} - \frac{1}{L_{ac}} \left(v_{rd} - v_{gd} \right) \\ \frac{di_{rq}}{dt} &= -\omega i_{rd} - \frac{R_{ac}}{L_{ac}} i_{rq} - \frac{1}{L_{ac}} \left(v_{rq} - v_{gq} \right) \\ \frac{dv^2}{dt} &= \frac{2 v_{gd} i_{rd}}{C_{eq}} \end{aligned} \tag{4.8}$$

4.3 Overall Control Design

To regulate reactive power according to a preset requirement, STATCOM should be able to draw active current for stabilizing the system by keeping capacitor voltages charged and balanced and to rapidly inject the required reactive current. In this work, backstepping control design (BSC) is applied to achieve the first objective. The idea is to recursively select appropriate functions of the state variables as virtual control to systematically decompose nonlinear systems to simpler and smaller ones. Each step results in a new virtual control corresponding to the decomposed subsystem which is used as a reference to the next design step. Ultimately, original control can be formed by summing up individual Lyapunov functions associated with each stage.

4.3.1 Phase Locked Loop

For grid connected systems, grid variables (i.e. voltage, phase and frequency) should be continuously monitored to guarantee correct operation between the STATCOM and the grid. Numerous synchronization methods are proposed in the

literature; among them, phase locked loop (PLL) is usually preferred due to its simplicity and robustness [134]. PLL is a nonlinear device used to synchronize phase and frequency of output signal with that of the input. A basic structure comprises three main blocks, namely the phase detector (PD), loop filter (LF) and a voltage-controlled oscillator (VCO). The PD is used to compare the two input signals, afterward; the error signal is filtered by LF. Then the filtered signal is used to drive VCO to generate the output phase. This process continues until the phase error between output and reference phase reduces to minimum value. Once the error is zero, phase will be locked. Synchronous reference frame PLL (SRF-PLL) is widely used for grid-connected converters for its simple implementation and accurate estimation. However, conventional SRF-PLL allows precise estimation in ideal condition and its performance during unbalanced grid voltage, presence of harmonics, and frequency deviation is highly degraded. Therefore, several methods are proposed in literature to cope with these needs, such as decoupled double SRF-PLL (DDSRF-PLL) and double second-order generalized integrator FLL (DSOGI-FLL) [135, 136]. In this work, for fast implementation, 3-phase SRF-PLL is used for synchronization.

4.3.2 BSC Design for dc-Bus Voltage

The overall capacitor voltage error is defined as $e_C = v^{*2} - v^2$, and its dynamic is computed by taking the derivative of e_C and substituting (4.8) into the derivative as

$$\frac{de_C}{dt} = \frac{dv^{*2}}{dt} - \frac{2v_{gd}i_{rd}}{C_{eq}} \tag{4.9}$$

The control objective is to make e_C converge asymptotically to zero. The active current term i_{rd} can be viewed as a virtual control variable in (4.9). Define Lyapunov energy function candidate as

$$W_C = \frac{1}{2}e_C^2 + \frac{1}{2}\lambda_C\gamma_C^2 \tag{4.10}$$

to satisfy control Lyapunov function (clf) inequality such that to guarantee the solution is globally asymptotically stable, the derivative of W_C is given [137]

$$\frac{dW_C}{dt} \leq 0 = -k_C e_C^2 \tag{4.11}$$

Thus, the condition can be enforced by

$$\frac{de_C}{dt} = -k_C e_C - \lambda_C \gamma_C \tag{4.12}$$

where k_C and λ_C are positive constants, and γ_C is the integral of e_C. Recalling (4.9), the derivative becomes

$$\frac{dv^{*2}}{dt} - \frac{2v_{gd} i_{rd}}{C_{eq}} = -k_C e_C - \lambda_C \gamma_C \tag{4.13}$$

By considering the state variable i_{rd} as a virtual control input of the subsystem in (4.8), a virtual control stabilizing function α can be obtained as

$$\alpha = \frac{1}{2v_{gd}} \left(K_C e_C + \lambda_C \gamma_C \right) \tag{4.14}$$

where $K_C = k_C C_{eq}$ and λ_C are positive constants. Since active current i_{rd} is selected as a virtual control, a dynamic behavior exists with its reference which can be examined by taking the derivative of the active tracking error $e_d = \alpha - i_{rd}$ such as

$$\frac{de_d}{dt} = -\frac{R_{ac}}{L_{ac}} i_{rd} + \omega i_{rq} + \frac{1}{L_{ac}} \left(v_{rd} - v_{gd} \right) - \frac{d\alpha}{dt} \tag{4.15}$$

In equation (4.15), active output voltage of STATCOM (v_{rd}) appears as a control input. Assuming the active grid voltage v_{gd} is constant, derivative of α can be calculated as

$$\frac{d\alpha}{dt} = \left(-\frac{i_{rd}}{C'_{eq}} K_C + \frac{1}{2v_{gd}} \lambda_C e_C \right) \tag{4.16}$$

v_{rd} can be chosen to cancel some undesirable dynamics by selecting a Lyapunov energy function candidate as

$$W_d = \frac{1}{2} e_d^2 + \frac{1}{2} \lambda_d \gamma_d^2 \tag{4.17}$$

where λ_d is a positive constant and γ_d is the integral of e_d, which is introduced to enforce steady-state error to zero despite the presence of disturbance and model uncertainty [138]. To satisfy clf inequality such that

$$dW_d/dt \leq 0 = -k_d e_d^2 \tag{4.18}$$

According to (4.18) and recalling (4.15), the final control law can be designed as

$$v_{rd} = v_{gd} - (K_d e_d + \lambda_d \gamma_d) - L_{ac} \frac{d\alpha}{dt} - R_{ac} i_{rd} + \omega L_{ac} i_{rq} \tag{4.19}$$

4.3.3 BSC Design for Reactive Current

The objective of BSC design of the reactive current is to force the reactive current state variable $\left(i_{rq}\right)$ to track the preset reference $\left(i_{rq}^*\right)$. The reactive current error i.e. $\left(e_q\right)$ is defined as

$$e_q = i^*_{rq} - i_{rq} \tag{4.20}$$

By selecting Lyapunov energy function

$$W_q = \frac{1}{2}e_q^2 + \frac{1}{2}\lambda_q \gamma_q^2 \tag{4.21}$$

dW_q/dt is written as an explicit function of v_{rq} to satisfy clf inequality such that

$$dW_q/dt \leq 0$$

This can be simply achieved by

$$dW_q/dt = -k_q e_q^2$$

The final control law can be designed as

$$v_{rq} = v_{gq} - \left(K_q e_q + \lambda_q \gamma_q\right) - L_{ac}\frac{di^*_{rq}}{dt} - L_{ac}\omega i_{rd} - R_{ac} i_{rq} \tag{4.22}$$

where K_q, λ_q are positive constants at our disposal, and γ_q is the integral of e_q. For voltage regulation, i^*_{rq} is derived by an external PI regulator, i.e.

$$i^*_{rq} = -K_v e_v - \lambda_v \gamma_v \tag{4.23}$$

where $e_v = v_g^* - v_{gd}$; K_v and λ_v are positive constants, and γ_v is the integral of e_v.

The control laws generated from the control design, v_{rd} and v_{rq} in (4.19) and (4.22), are synthesized to generate suitable modulation index (M_I) and phase angle (δ) such as

$$M_I = \sqrt{v_{rd}^2 + v_{rq}^2}, \delta = \arctan\left(\frac{v_{rq}}{v_{rd}}\right) \tag{4.24}$$

Accordingly, M_I and δ are used to generate suitable modulation signals $\left(i.e.\ v_{m,ref} = \sin(\omega t_m + \delta)\right)$.

4.3.4 Capacitor Voltage Balancing

Capacitor voltage balancing is achieved by maintaining energy inflow and outflow of the converters. Since current is the same for all units in the phase, to handle the imbalance, the output voltage of each unit needs to be modulated separately. Therefore, through proportional controller, individual balancing is implemented to extract reference voltages by getting errors between average cluster voltage $(\overline{v}_m)$ and individual voltages [19]. Then, the outputs are multiplied by sinusoid so that resulting reference voltages are in−phase or opposite−phase of the corresponding current. The relative adjustments are implemented as

$$v_{IBmn} = \begin{cases} K_{IB} \times (\overline{v}_m - v_{mn}) \times \cos(\omega t) & , q > 0 \\ \\ -K_{IB} \times (\overline{v}_m - v_{mn}) \times \cos(\omega t) & , q < 0 \end{cases} \tag{4.25}$$

Where v_{mn} refers to individual capacitor voltages in each phase $m = a, b, c$. As in (4.25), errors $(\overline{v}_m - v_{mn})$ and K_{IB} constant are used as indexes to determine adjustment amount of PWM references. For STATCOM, the reactive current is dominant, thus, the component $\cos(\omega t)$ ensures adjustments are synchronized with relative phase current. As long as reference voltages $\left(v_{m,ref}\right)$ are obtained from inner

current control, they are updated with corresponding individual control outputs (v_{IBmn}) to generate suitable overall references as

$$v_{mn,ref} = \frac{\left(v_{m,ref}\right)}{NV_{DC}} + v_{IBmn} \tag{4.26}$$

The voltage references in (4.26) are processed in the modulation stage for generating suitable driving pulses which determined by comparing (on−line) low-frequency reference $\left(v_{mn,ref}\right)$ with high−frequency triangular signal (i.e. carrier). For multilevel, N triangular-carriers are required with a phase shift of (π/N) for each cell. To produce triggering pulses for three-phase multilevel SSBC STATCOM, carrier and modulating signals are shifted by $\pm\frac{2\pi}{3}$ for phase b and phase c accordingly.

4.3.5 Fault-Tolerant Operation

Fig. 4.3 shows the flowchart of the post-fault operation of SSBC based STATCOM. When a fault is detected in one H-bridge, the required commanding pulses should be sent to the IGBT to bypass related converter units. Besides, dc-voltage reference and switching frequency should be updated to enable the fault-tolerant operation and enhance the performance under this condition. The proposed backstepping control allows a stable transition of the control action without losing its stability.

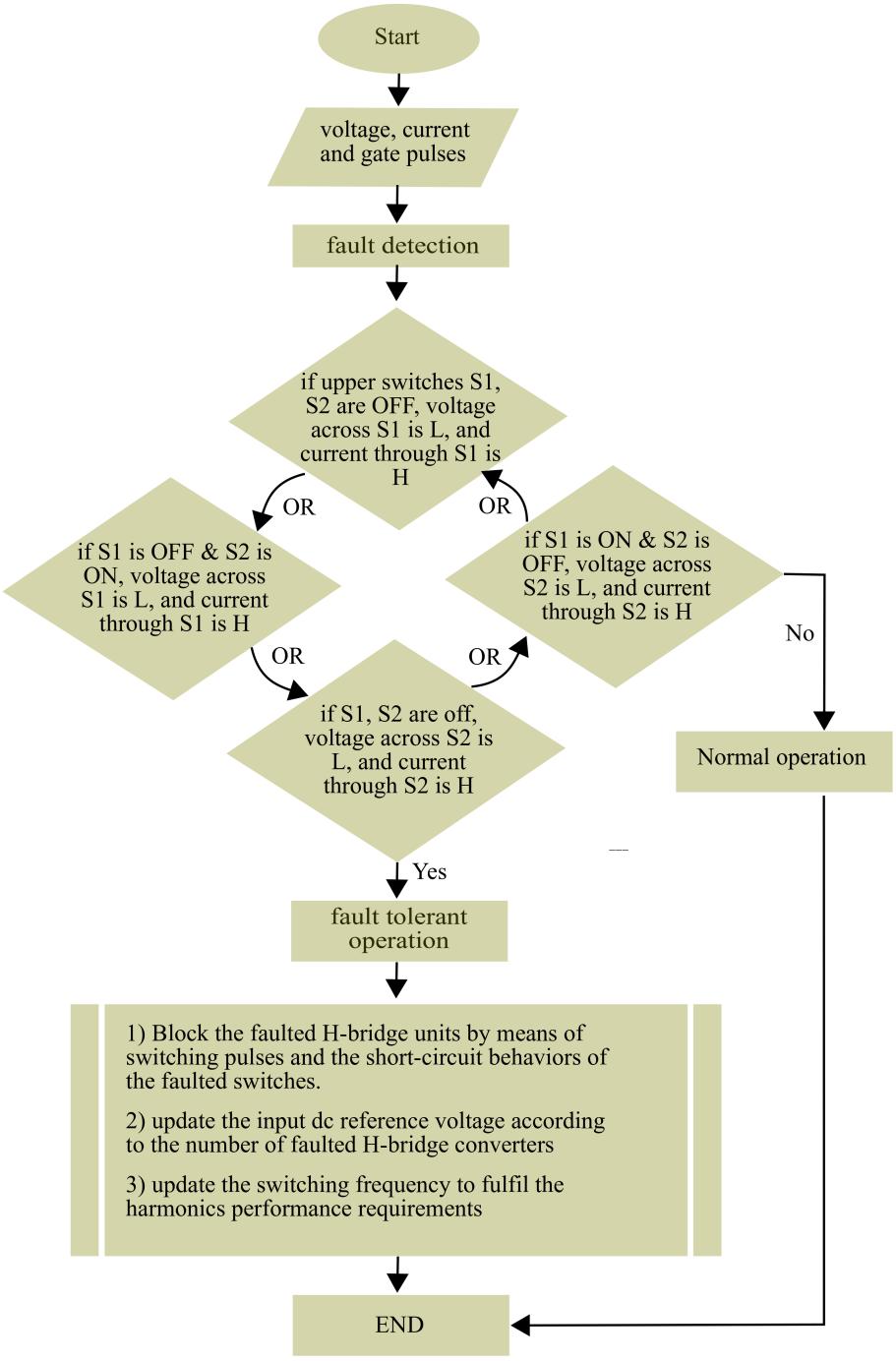


Figure 4.3: Flowchart of fault-tolerant operation.

Fig. 4.4 shows the schematic diagram of the overall direct control scheme using backstepping approach. The overall control consists of three parts, namely, the generation of the reference dq-currents, the inner current control and the PWM pulse generator. In the first part, the α (4.14), $d\alpha/dt$ (4.16) and i_{rq}^{*} are generated to inject the precise reactive power amount by the STATCOM. The inner current loop compares the

measured i_{rd} and i_{rq} with α and i_{rq}^{*}, to produce the corresponding values for v_{rd} and v_{rq} using (4.19) and (4.22) respectively.

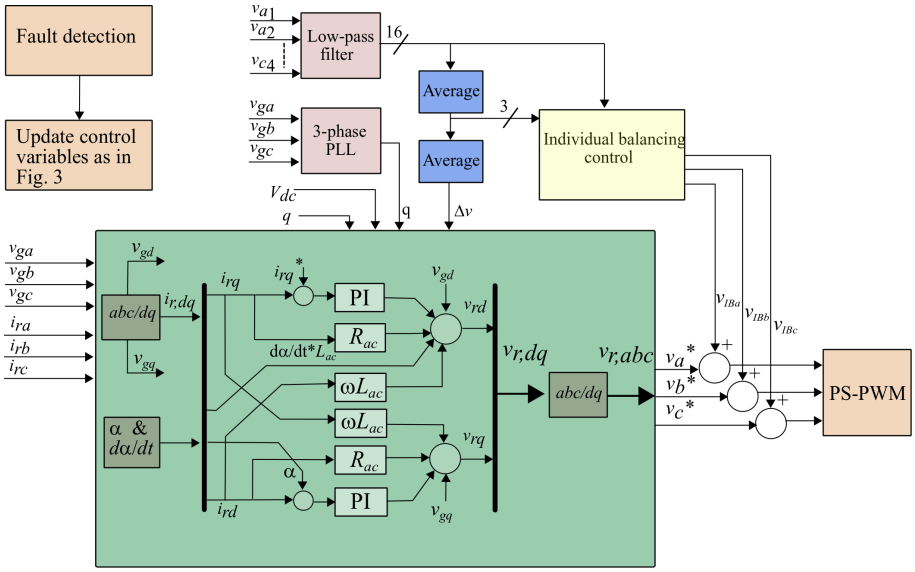


Figure 4.4: Overall control of STATCOM.

4.3.6 Phase Shifted PWM

The switching angles of each H-bridge are determined by comparing (on-line) low-frequency reference (i.e. modulation; $v_{mn,ref}$) with high frequency triangular signal (i.e. carrier) as shown in Fig. 4.5. For multilevel, N triangular-carriers are required with a phase shift of $(180/N)$ for each cell. The modulation signals are generated in a closed loop. To produce triggering pulses for 3-phase multilevel SSBC STATCOM, the carrier and modulating signals are shifted by $\pm \frac{2\pi}{3}$ for phase-b and phase-c accordingly.

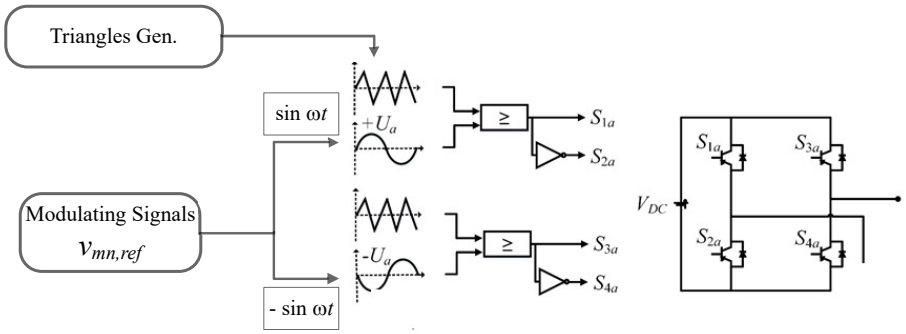


Figure 4.5: PS-PWM switching for one H-bridge

4.3.7 Third Harmonics Injection

4.3.7.1 Background−Mathematical Model

This section presents comprehensive analysis of the capacitor voltage ripple generation. Based on this analysis, proposed zero−sequence injection method is introduced in the following section its elimination.

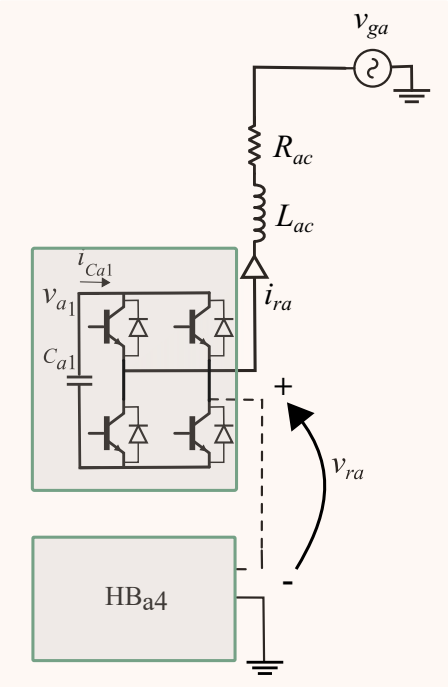


Figure 4.6: Single−phase SSBC STATCOM

For analysis purposes, a single phase multilevel SSBC circuit as depicted in Fig. 4.6 is considered here. The instantaneous power at both sides of each unit in the phase a can be written as [139]

$$p_a = \bar{p}_a + \tilde{p}_a \tag{4.27}$$

where $\bar{p}_a$ is the average active power, and $\tilde{p}_a$ refers to the generated oscillating power. With the assumption that the capacitor voltages are equal in each phase, given that the positive−sequence voltage and currents [140]

$$\begin{cases} v_{ran} = \frac{V_{ra}}{N}\ \mathrm{e}^{j\vartheta} \\ \\ i_{ra} = I_{ra}\ \mathrm{e}^{j\delta} \end{cases} \tag{4.28}$$

the instantaneous power $(i.e.\ p_{an})$ for each individual capacitor can be written as follows

$$p_{an} = -v_{an} \cdot C_{an} \frac{dv_{an}}{dt}$$

$$= \overbrace{\frac{1}{2}\frac{V_{ra}}{N} I_{ra} \cos(\vartheta - \delta)}^{\bar{p}_{an}} - \overbrace{\frac{1}{2}\frac{V_{ra}}{N} I_{ra} \cos(2\omega t + \vartheta + \delta)}^{\tilde{p}_{an}} \tag{4.29}$$

where $n = 1, 2, .., N$ and N refers to the number of cells in each phase. Assuming the flow of the energy is from the $ac-$side to the $dc-$side, neglecting the losses, the ripple voltage across the capacitor can be calculated as

$$\tilde{v}_{an} = \frac{1}{2}\frac{V_{ra}}{N} I_{ra} \int \cos(2\omega t + \vartheta + \delta)\, dt \tag{4.30}$$

For STATCOM operation, the phase of current is given by $\delta = \vartheta \pm \frac{\pi}{2}$. Accordingly, the capacitor ripple voltage during both modes is written as

$$\tilde{v}_{an} = \mp \frac{1}{2} \frac{V_m}{NCV_{an}} I_m \left[\frac{\cos 2\omega t}{2\omega} \right] \tag{4.31}$$

In (4.31) the amplitude of the ripple can be written as

$$\tilde{v}_{an} = \mp \frac{M_I I_m}{4\omega C} \tag{4.32}$$

where the modulation index $M_I = \frac{V_{ra}}{NV_{an}}$, and I_m refers to the phase current. The previous formula defines the main factors (i.e. M_I, I_m, and C) that affect the ripple voltage magnitude. Ripple harmonics are deteriorated with low switching frequency which might affect injected current harmonics. However, the magnitude of the second harmonics, which determines capacitor voltage ripple, is significantly affected by current rating, modulation index and the capacitance. Thus, commonly, capacitance is designed to limit the ripple voltage to 10%. To design STATCOM with higher compactness and lower cost, capacitor value should be reduced. However, lowering the designed capacitance, higher harmonics distortion is induced on the output voltage of STATCOM. To address this problem the instantaneous power at the output of the converter can be controlled by injecting the zero-sequence voltage (ZSV) component.

4.3.7.2 Suppression of dc Voltage Fluctuation Using Zero-Sequence Voltage

Generally, for three-phase system without neutral, ZSV does not affect the injected current but it influences the reference point of connection. Thus, it affects overall active power flow in each phase. If the output voltage of the inverter is defined by

$$v_{ran} = \frac{V_{ra}}{N} \sin(\omega t + \vartheta) + \frac{V_0}{N} \sin(3\omega t + \vartheta_0) \tag{4.33}$$

the corresponding active power generated due to zero sequence injection can be calculated as

$$\begin{aligned} p_{an} &= -v_{an} \cdot C_{an} \frac{dv_{an}}{dt} \\ &= \left[\frac{V_{ra}}{N} \sin(\omega t + \vartheta) + \frac{V_0}{N} \sin(3\omega t + \vartheta_0) \right] i_{ra} \sin(\omega t + \delta) \end{aligned} \tag{4.34}$$

where $n = 1, 2, .., N$. Considering only the power generated due to the zero−sequence term, it can be expressed as

$$p_{03} = \frac{1}{2}\frac{V_0}{N} I_{ra} \left[\cos\left(2\omega t + \vartheta_0 - \delta\right) - \cos\left(4\omega t + \vartheta_0 + \delta\right)\right] \tag{4.35}$$

By grouping (4.29) and (4.35), the instantaneous power at the output side of the converter is equal to

$$p_{an} + p_{03} = \overbrace{\frac{1}{2}\frac{V_{ra}}{N} I_{ra} \cos\left(\vartheta - \delta\right)}^{\overline{p}_{an}} - \overbrace{\frac{1}{2}\frac{V_{ra}}{N} I_{ra} \cos\left(2\omega t + \delta\right)}^{\widetilde{p}_{an}} +$$

$$\overbrace{\frac{1}{2}\frac{V_0}{N} I_{ra} \left[\cos\left(2\omega t + \vartheta_0 - \delta\right) - \cos\left(4\omega t + \vartheta_0 + \delta\right)\right]}^{p_{03}} \tag{4.36}$$

To calculate the ripple voltage, oscillating term in (4.36) is assigned to the power at the $dc-$side

$$-v_{an} \cdot C_{an} \frac{dv_{an}}{dt} = -\overbrace{\frac{1}{2}\frac{V_{ra}}{N} I_{ra} \cos\left(2\omega t + \delta\right)}^{\widetilde{p}_{an}} +$$

$$\overbrace{\frac{1}{2}\frac{V_0}{N} I_{ra} \left[\cos\left(2\omega t + \vartheta_0 - \delta\right) - \cos\left(4\omega t + \vartheta_0 + \delta\right)\right]}^{p_{03}} \tag{4.37}$$

If $\vartheta_0 = \pi$ and $\delta = \pm\frac{\pi}{2}$ for capacitive and inductive operation, the voltage ripple across the capacitor is given by

$$\widetilde{v}_{an} = \pm \left[\frac{1}{2}\frac{V_{ra}}{NC_{an}V_{an}} I_{ra} - \frac{1}{2}\frac{V_0}{NC_{an}V_{an}} I_{ra}\right] \frac{\cos\left(2\omega t\right)}{2\omega} \pm$$

$$\frac{1}{2}\frac{V_0}{NC_{an}V_{an}}I_{ra}\frac{\cos(4\omega t)}{4\omega} \tag{4.38}$$

In (4.38), the $\cos(2\omega t)$ can be reduced by controlling the V_0.

4.4 Simulation Results

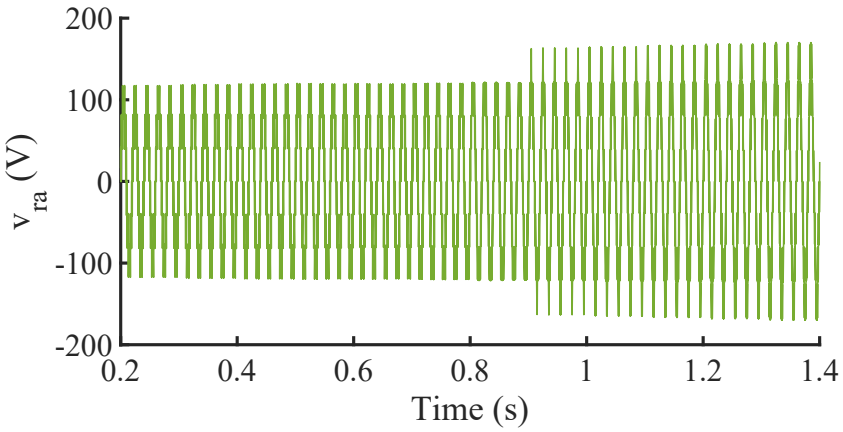
To evaluate the performance of the proposed control system, a STATCOM model is developed using MATLAB/Simulink. The model uses a three-phase, star-connected 9-level SSBC. Each phase consists of four H-bridge units connected in series. In addition, by considering the harmonic performance of the line current, L_{AC} has been chosen to be 6 mH. Detailed specifications of the SSBC based STATCOM model are given in Table 4.1

Table 4.1: System and control parameters for 9−level SSBC STATCOM

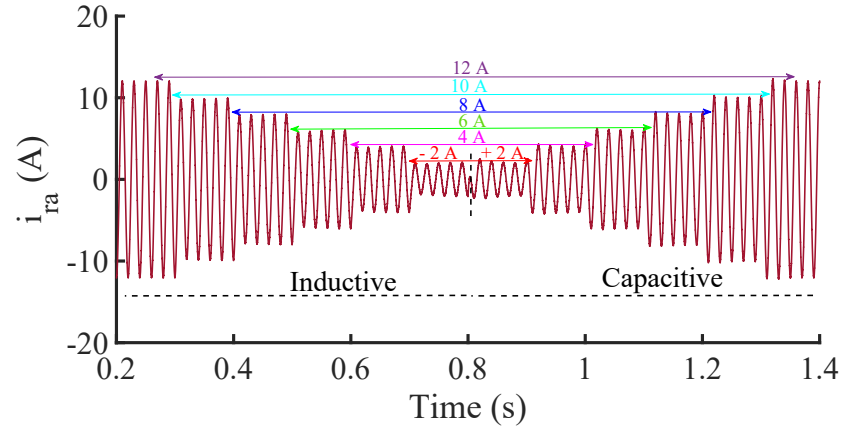
Parameter	Symbol	Value
Line to line rms grid voltage	V_{gL-L}	142 V
Reactive power capacity	Q	± 2 kVAr
series coupling inductance	L_{AC}	6 mH
Resistance of L_{AC}	R	0.2 Ω
Cascaded H-bridge number per phase	N	4
Input DC capacitor voltage for each H-bridge unit	V_{DC}	40 V
Input capacitance for each H-bridge unit	C_{DC}	0.9 mF
Fundamental frequency	f_F	50 Hz
Switching frequency	f_{SW}	1 kHz
Maximum and mi-minimum modulation index	$MI_{IMax} - MI_{Min}$	0.59 p.u. − 0.85 p.u.
Inner control gains	K_P, K_I	1.8, 75
Outer control gains	$K_{P_{Vdc}}$, $K_{I_{Vdc}}$	0.01, 0.5
Individual balancing control gain	K_{IB}	0.3

4.4.1 Reactive Current Step Response

The exchange of the reactive power in the capacitive and inductive modes of the proposed PS-PWM based STATCOM is tested by varying the reactive current $\left(i_{rq}^{*}\right)$ in step. The result in Fig. 4.7 illustrates the operation principle of the STATCOM with the proposed control. In the standby mode, i_{rq}^{*} is set at 0 A. To test the transition to inductive and capacitive modes, a six step change in i_{rq}^{*} with 2 A difference from -12 A to -2 A is imposed at 0.2 s to 0.8 s, respectively. Then, similiarly, a step change in i_{rq}^{*} for +2 A to +12 A is imposed for 0.6 s. As a response to a -12 to +12 step change in both inductive and capacitive modes, the M_I is varied to set to be 0.59 p.u. for the -12 A inductive case then increasing up to 0.85 p.u. for the +12 A capacitive case. As can be seen, for both methods, a rapid adjustment of reactive power is achieved. This is superior to the indirect control scheme, which requires changing of the capacitor voltage level to cope with the reactive power requirements. The slower response of the indirect control is attributed to the capacitor's charging and discharging mechanism which demands more time for the capacitor to change its voltage to a new required level. On the other hand, for the direct control (based on the variation of M_I using PS-PWM method), this problem is eliminated by controlling the M_I instead. Thus, fast and efficient tracking is achieved.



(a)



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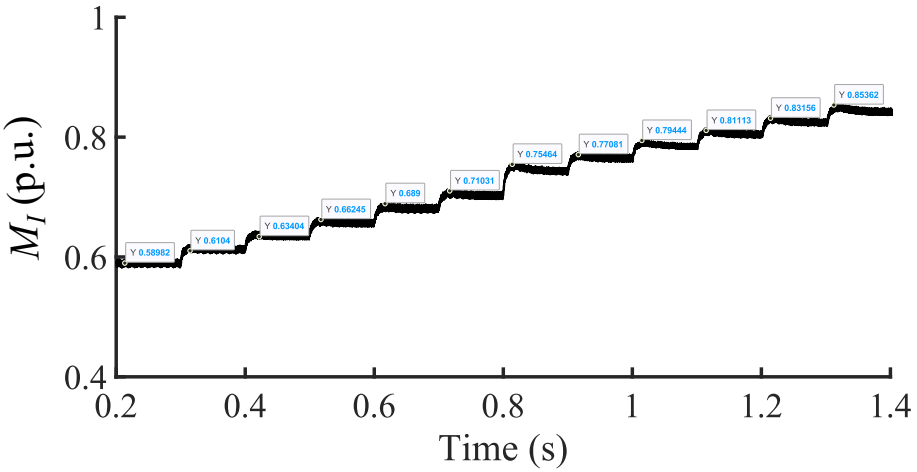


(c)

Figure 4.7: Reactive power compensation using STATCOM for 6 different step response in the capacitive and inductive operation modes (a) output voltage waeform(b) line current waveform (c) M_I response

The harmonics of the voltage and current waveforms are analyzed under the same operation with similar switching frequency (i.e. 1 kHz) and the results are given in Table 4.2. The calculation of the THD are restricted to the 100 harmonics component (5 kHz) which means, with the operation of overall switching frequency (8 kHz), the effect of capacitor voltage ripple is the main factor of harmonics degradation. As seen in Table 4.2, the design of STATCOM with 9-level SSBC (operating with 1 kHz switching frequency) is capable of reducing the THD to less than 5% over the entire operating range. As discussed in Chapter 3 of this thesis, the voltage ripple is mainly affected by the M_I and the current value. Hence, with higher rms current, the THD% is increased compared to lower rms current case under the same mode of operation.

For the current harmonics performance, it is clear its distortion is directly affected by the output voltage difference between grid voltage (v_g) and that of the SSBC (v_r). By having the L_{ac} in series, it acts as a filter for the high-frequency harmonic component resulting in less THD of the i_r. Thus, the harmonics content of v_r plays an important role in determining the quality of current waveform.

Table 4.2: THD harmonics analysis for multiple cases in both capacitive and inductive operation modes

Reference current (A)	**-12**	**-10**	**-8**	**-6**	**-4**	**-2**	**0**	**2**	**4**	**6**	**8**	**10**	**12**
THD% of output voltage	2.36	2.29	2.06	1.72	1.52	1.13	0.93	1.15	1.40	1.77	2.17	2.83	3.19
THD% of line current	0.58	0.78	0.83	1.10	1.65	3.40	–	3.92	1.56	0.97	0.83	0.67	0.49

4.4.2 Dynamic Response Analysis

The dynamic performance of STATCOM is depicted in Fig. 4.8. The worst case i.e. a transition from full inductive to full capacitive (-12 to +12 A) scenario is

considered. As shown in Figure 4.10 (a), it takes one a cycle to reach steady state. This fast response is attributed to the direct control of SSBC output voltage using the M_I. Fig. 4.8 demonstrate the responses of i_{rq}, M_I, v_{ra} and i_{ra}.

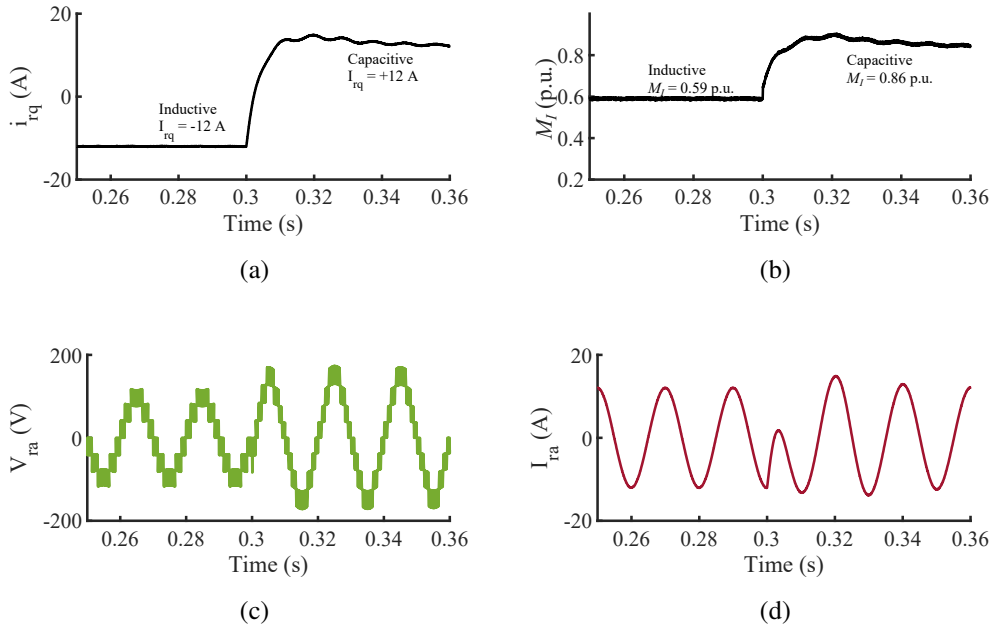
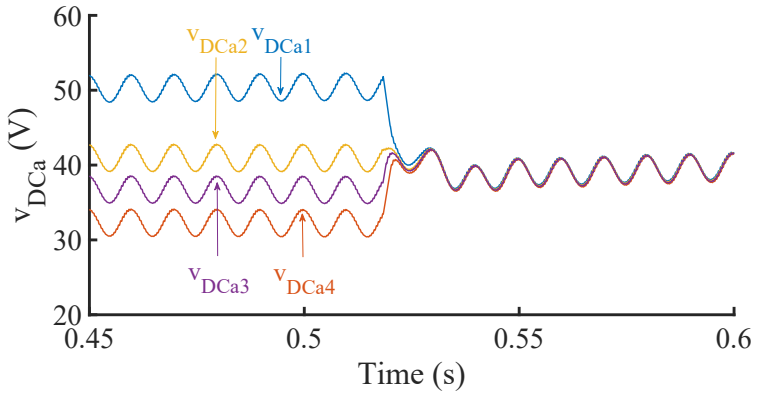


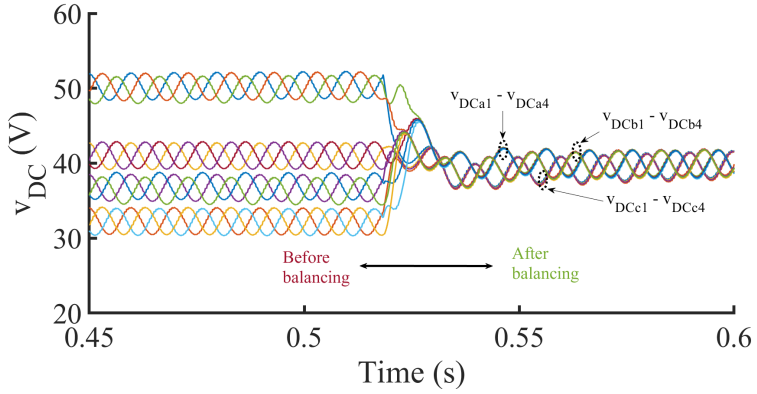
Figure 4.8: Reactive current step response test for ±12 A (a) i_{rq} response (b) M_I response (c) voltage waveform (d) current waveform

4.4.3 Capacitor Voltage Balancing

Fig. 4.9 shows simulated waveforms of the phase-a ac voltage v_{ra} and the dc capacitor voltages for phase-a and all phases, which confirms the effectiveness of the individual balancing control. During inductive operation at 2 kVAr with $v_{dc} = 40$ V, the individual balancing control was intentionally enabled at 0.52 s. To create an unbalance case, resistors are connected at the input side of the H-bridge converters with different values $(55\,\Omega, 35\,\Omega, 45\,\Omega, 40\,\Omega)$. The THD of the output voltage before and after balancing is calculated and the results demonstrated 2.5% harmonics THD improvement after the individual balancing is activated. This is due to the fact that the phase-shifted PWM method is heavily affected during the unbalanced case.



(a)



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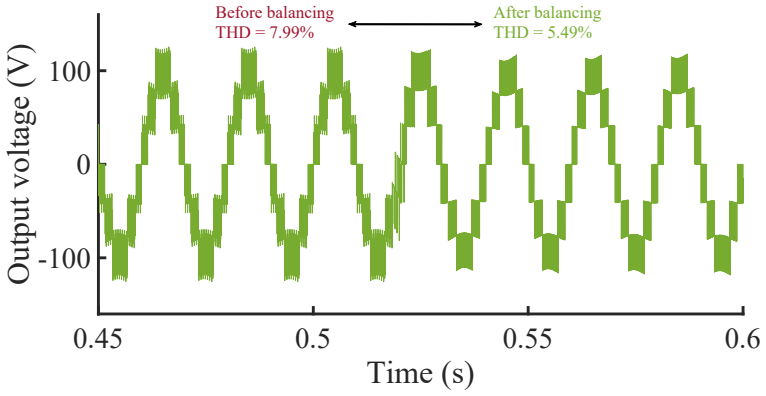


(c)

Figure 4.9: Individual capacitor voltage balancing (a) capacitor voltages of phase a (b) capacitor voltages for all phases (c) output voltage of phase a

4.4.4 Robustness Analysis

Before experiments, in order to verify robustness of the proposed control, system was simulated under two cases. First, stability boundary of the proposed control was

evaluated by imposing a step change on V_{dc} [141]. Then, operation with variable system impedance was conducted to confirm robustness and reliability of the control under weak grid condition. A comparison was made with a conventional PI control.

In the first case, a 60 V step in V_{dc} was applied at $t = 0.4$ s, giving the responses shown in Fig. 4.10. The system was simulated with different gains and compared with PI control. The integral gain for all cases was fixed at $K_I = 100$ to alleviate steady-state error. It is shown that, with the backstepping control, the conversion is assured with variation of the controller gain while growing oscillation is observed in the case of PI controller. This confirms the high bandwidth and stability margin of the proposed control.

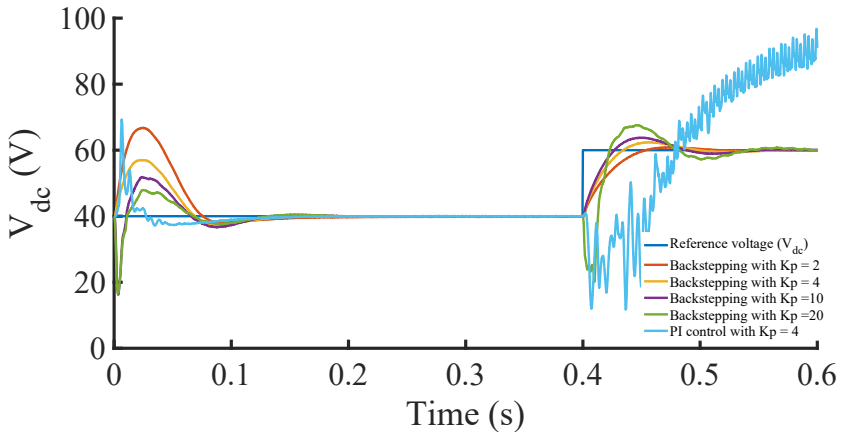


Figure 4.10: V_{dc} step response for backstepping and PI controllers

Besides, DVC's stability is greatly affected under weak grid operation [142, 143]. This is because variation of system impedance influences active power regulation ability and increases interactions between control loops which harmfully affect DVC dynamics. Therefore, proposed controller was tested under different system impedance values to verify its robustness.

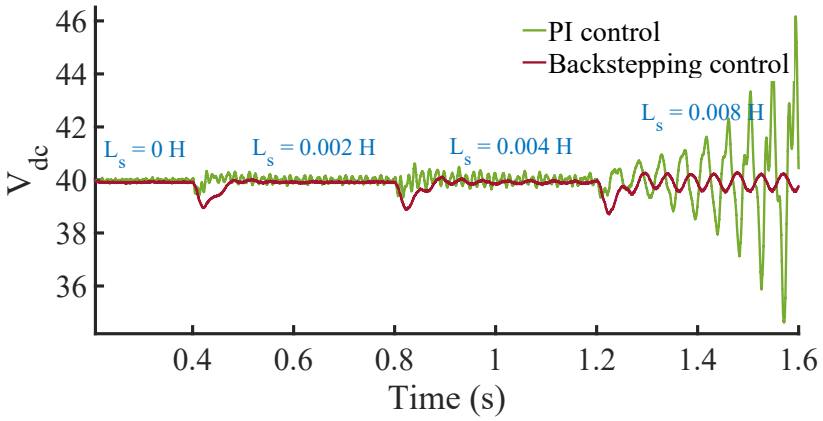


Figure 4.11: V_{dc} average control with variable impedance

Four cases were considered with L_s = 0.008 H as the worst case. As shown in Fig. 4.11, proposed control maintains dc-bus voltage control under all cases although with small oscillation for the worst-case condition, while with increasing impedance values, growing oscillations are observed in the case of PI control.

Fig. 4.12 shows the results of dynamics and steady-state performance of post-fault operation of 9-level SSBC STATCOM under capacitive mode. This case is presented to assure the suitability of proposed control not only during normal operation but also if fault-tolerant operation is necessary. However, it should be mentioned that the fault detection, insulation, and system recovery are not the primary scope of this paper. As observed, theoretically when the fault is detected in one H-bridge of one phase, the corresponding H-bridge units in the three phases are bypassed. The capacitor voltage reference is changed to allow the conversion to a 7-level system to cope with the grid voltage while continuing the injection of the same amount of reactive current. In order to convert in seven level operation, the switches have to be selected capable to sustain the higher voltage. To maintain the performance of the harmonic, the switching frequency is increased to guarantee the shifting of the harmonics spectrum to a higher frequency that can be easily attenuated by the series inductor. Latest observation demonstrates an additional capability of the proposed system, which will be fully exploited with the support of experimental results in a future work.

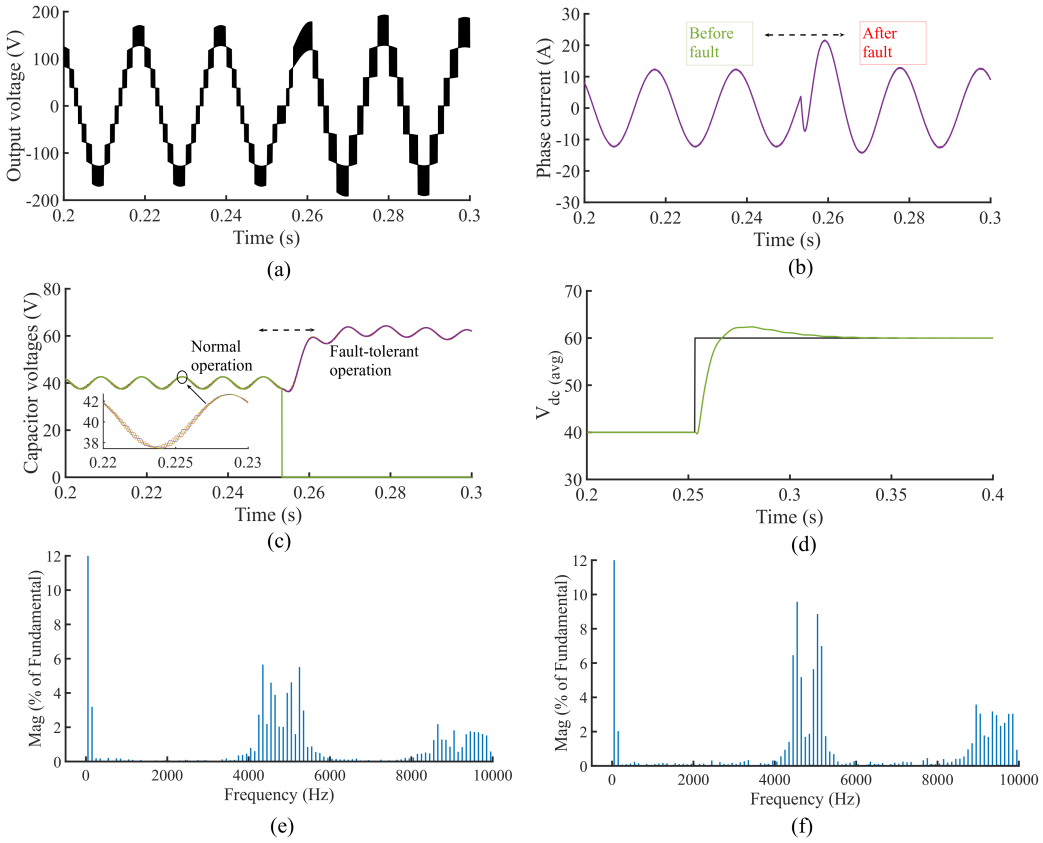


Figure 4.12: Simulation results for fault-tolerant control of 9-level SSBC STATCOM (a) output voltage (b) phase current (c) capacitor voltages (d) average input dc voltage (e) FFT analysis of phase voltage before fault (f) FFT analysis of phase voltage after fault

4.5 Hardware Implementation

4.5.1 Hardware Set-up

To practically validate the proposed control, a three−phase 9−level SSBC STATCOM test rig was used, which is a subset from a three−phase 33−level MMCC system developed by DigiPower [53]. The rig (shown in Fig. 4.13) is connected to the grid using three step−down transformers (to be conneccted to 142 V) and series inductor, L = 6 mH. The fundamental frequency is 50 Hz and input dc voltage for each HB is set to 40 V. Each H-bridge consists of two separate half-bridges, DSP board, input and output voltage and current sensors. The purpose of the DSP is to provide data acquisition and bidirectional communication with the main control board. The ON Semiconductor IGBTs 30N120L (1200 V, 35 A @ 100 °C, with anti−parallel diodes) were available in power circuits. The control was coded in VHDL except for PLL and Nios II software which $C++$ is used. The results are analyzed using Yokogawa DLM4058 oscilloscope.

An FPGA control board designed by DigiPower [53], which incorporates one FPGA, one CPLD, and a DSP that cooperates to satisfy the system requirements, and is capable to control up to 48 distinct H-bridges (i.e. 96 half-bridges), was used to implement the control. The board hosts a 5CEBA7F31C7 Cyclone® V FPGA from Intel, which has 56,480 adaptive logic modules (ALMs) that use an 8-input LUT with four dedicated registers for getting improved timing closure and higher design packing capability. Besides, it has 156 variable-precision DSPs blocks for processing arithmetic operations. Control operations are done with 50 MHz clock, which is enough to implement the algorithms. An additional ADC board developed by DigiPower provides line voltages and currents to FPGA through SPI. These values are processed by Nios II and sent as inputs to the other VHDL blocks. The adopted control board has 480 output pins which add flexibility to extend the SSBC to a high number of levels. The CPLD device is the ALTERA MAX 10 10M16DAF484 which represents the ideal solution for problems of system management, I/O expander, control algorithm implementation, and communication management. Texas Instruments 320F28377S 32-Bit DSP is used in this work for the PLL implementation.

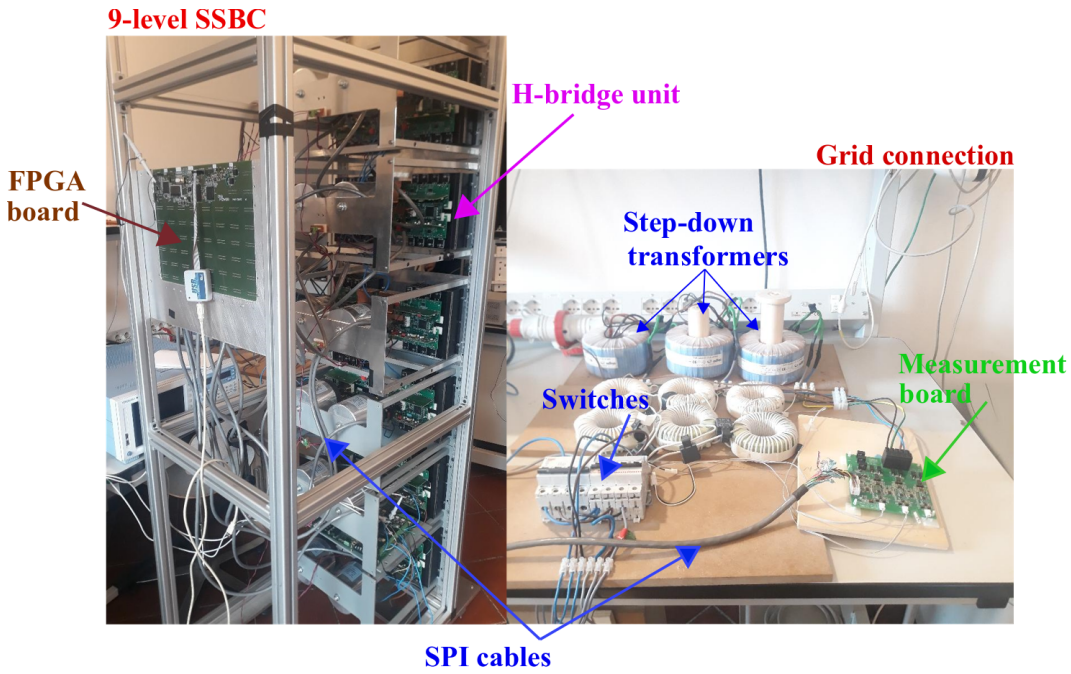


Figure 4.13: Hardware set-up of 9-level SSBC STATCOM

4.5.2 Control Implementation

Fig. 4.14 illustrates the designed code structure. The *ref_current_gen* generates active and reactive current references for the inner *current control* in which reference voltages represented by (4.19) and (4.22) are generated. For the proposed control, active current reference is generated as depicted by (4.14). Besides, a compensating term (4.16) produced from the backstepping approach is added to the inner current control for better stabilizing the internal control. M_I and δ are calculated based on (4.24).

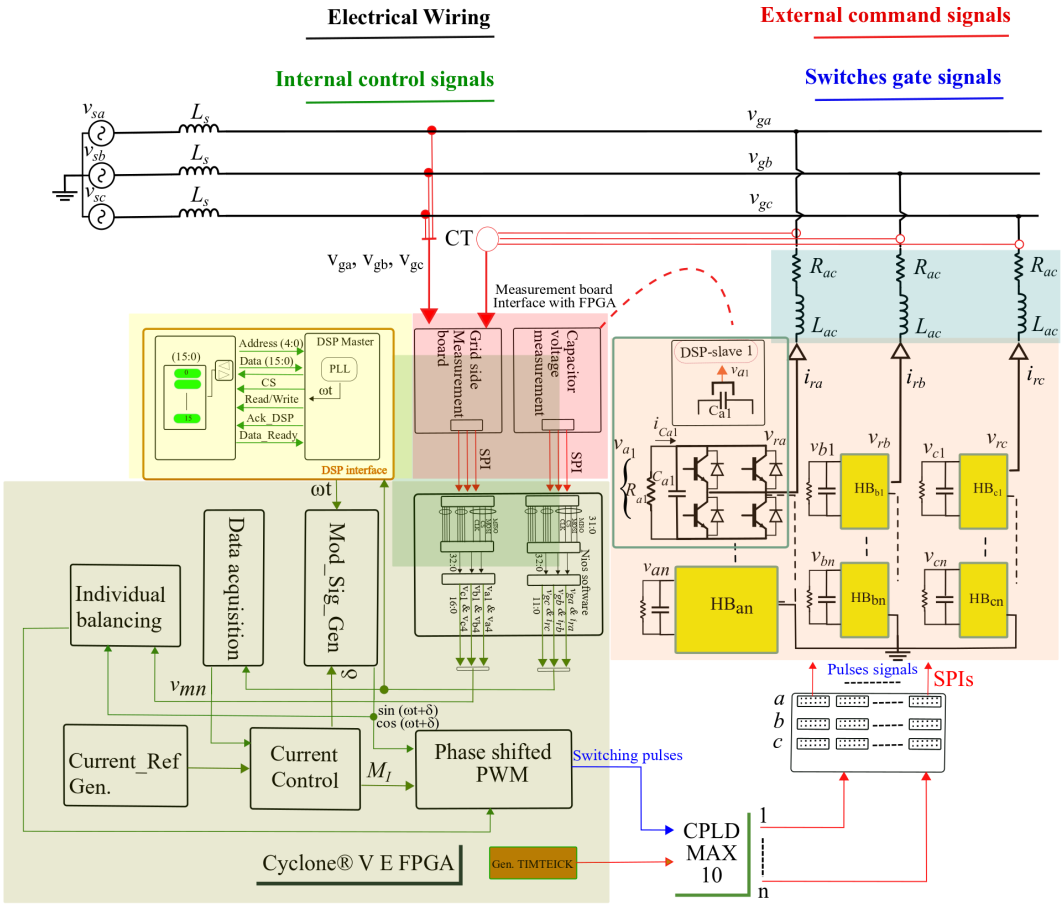


Figure 4.14: FPGA-hardware-implementation

The angle (δ) is sent to *Mod_Sig_Gen* block to generate the required synchronizing $\sin-$ and $\cos-$ signals used in the individual balancing and switching blocks. The square and trigonometric functions ($i.e.$ $\sin, \cos, \arctan$) are calculated using *ALTERA* arithmetic functions *(ALTFP_ATAN, ALTFP_SQRT and ALTERA_Cordic)*. In *Individual balancing control* block, the required voltage

adjustments for capacitor voltage balancing are generated and used to update reference signals as described by (4.26). Synchronizing signal (ωt) is sent to FPGA using *DSP interface* block. The switching pulses of each H-bridge are then determined by comparing generated modulating signals $v_{mn,ref}$ with high−frequency triangular signals (generated using counters in VHDL). SPIs cables are used to deliver pulses to the corresponding modules.

4.5.2.1 PS-PWM Implementation

The switching pulses of each H-bridge are then determined by comparing generated modulating signals $v_{mn,ref}$ with high−frequency triangular signals (generated using counters in VHDL). SPIs cables are used to deliver pulses to the corresponding modules. Table 4.3 and 4.4 illustrate the details implementations and resource utilization of the FPGA.

Table 4.3: FPGA hardware resources use of STATCOM control

Resource utilization by entity	Combinational ALUT	Dedicated Logic Registers	Block Memory bits	DSP blocks
Top level	53748	21168	3315998	119
Gen. TIMETICK	24	15	0	0
DSP Interface	93	49	0	0
Mod_sig_gen	1186	763	0	2
V_{DC} average	13062	0	0	0
Top control	28124	5307	7454	48
Individual balancing control	1592	126	0	54
NIOS	5893	5427	338944	0
PS-PWM	2598	408	0	15

Table 4.4: Total blocks utilization

Logic utilization (in ALMs)	Total registers	Total block memory bits	Total DSP Blocks	Total PLLs
29,579 /56,480 (52 %)	20513 /225920	3,315,998 / 7,024,640 (47 %)	119/156 (76 %)	2/7 (29 %)

4.5.3 Results and Discussion

4.5.3.1 PLL Synchronization

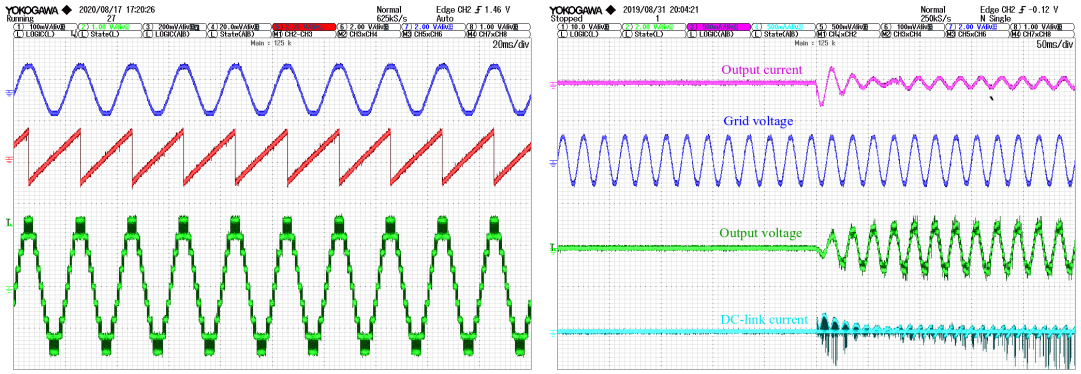
The following procedures are to be followed to test the system after the successful generation of the required netlist; these procedures are supported by the hierarchical design of the control and its implementation in FPGA: $Step\ 1$: testing the grid voltage and current measurements, $Step\ 2$: testing all H-bridge individually and assuring the correct SPI communication, $Step\ 3$: testing the output phase voltages of the 9-level SSBC system and ensuring the correct operation of the PS-PWM method. Once all the aforementioned steps are performed, it is essential to assure the correct synchronization between the SSBC output voltage and the voltage of the grid. This step is very important for the safe operation of the inverter and proceeding correctly with the control implementation. For instance, if SSBC output voltage terminals are connected in opposite phase with the grid voltage, the capacitor voltage will not charge correctly and accordingly control will not work properly. Further, if the system is connected while the capacitor voltages are not charged to the required level, high current will flow and hence resulting in system faults and damage. Fig. 4.15a verifies the correct synchronization of the SSBC system with the grid.

4.5.3.2 Start-up Test

STATCOM operation relies on the flow of reactive current due to the voltage difference between STATCOM and and the grid. However, dc-input capacitor voltages of STATCOM are zero at start-up. Therefore, they need to be pre-charged to nominal value to avoid flow of instant large inrush current that endangers safety of both the system and humans. So, task of start-up operation is to charge capacitors to their reference values in a short time. This process can be achieved by means of auxiliary power supplies. However, with high number of levels, it is not practical due to its high cost.

On the other hand, the use of series resistors at the ac side is proved to be easy for implementation and robust, with balancing during start-up, for closed-loop control. Therefore, three resistors are inserted in series with ac side of STATCOM and all triggering pulses are suppressed, so that charging of dc capacitors is obtained through the corresponding diodes. Thus, initial inrush current is minimized, and capacitors

are charged with RC circuit. Once voltages across capacitors reach certain value, resistors are bypassed and gate pulses are enabled allowing STATCOM to operate in its normal operation. At this stage, a small angle shift between STATCOM and grid voltages is maintained for losses compensation. Results in Fig. 4.15b confirms validity and effectiveness of the applied method by experiment based on a three-phase 9-level prototype.

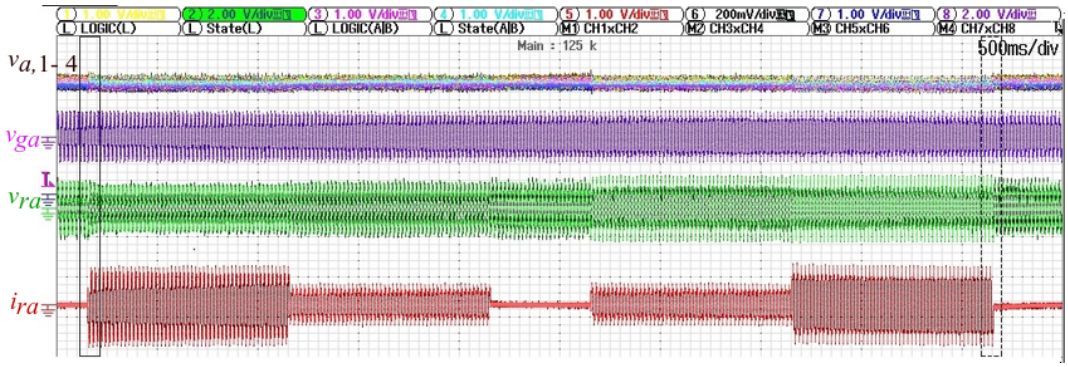


(a) (b)

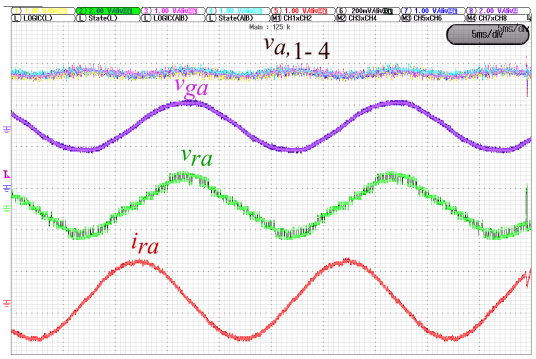
Figure 4.15: SSBC STATCOM implementation (a) PLL synchronization test (b) Start-up test

4.5.3.3 Steady State Response Analysis

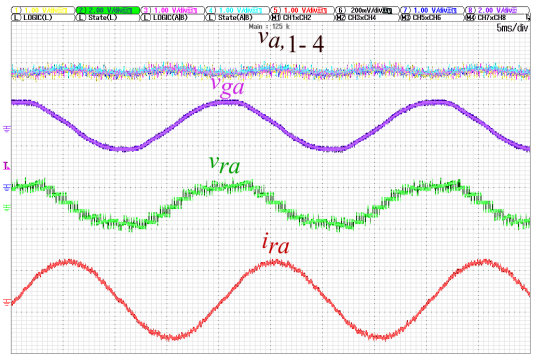
To validate the performance of the proposed control, STATCOM was operated under two tests. The first one was performed with varying reactive current (i_{Cq}) in steps. Two modes of operation (i.e. capacitive and inductive) were considered in which $\pm$ 0.4 and $\pm$ 0.8 p.u. step changes are imposed each for 50 cycles and results are reported in Fig. 4.16 (a). In addition, results of $\pm$ 0.8 p.u. for two cycles are shown in Fig. 4.16 (b) and Fig. 4.16 (c) respectively. In capacitive mode, STATCOM reacts by increasing M_I, thus increasing the voltage at STATCOM side which allows injection of reactive current to the point of common coupling. In inductive mode, control force the system to decrease the M_I value, therefore, reactive current is absorbed by STATCOM due to the opposite voltage difference across L_{ac}. The results also verify the performance of the individual balancing control in which capacitor voltages are well−balanced against internal losses of the system in this case.



(a) response for ± 0.4 p.u. and ± 0.8 p.u.



(b) 0.8 p.u. capacitive mode



(c) 0.8 $p.u$ inductive mode

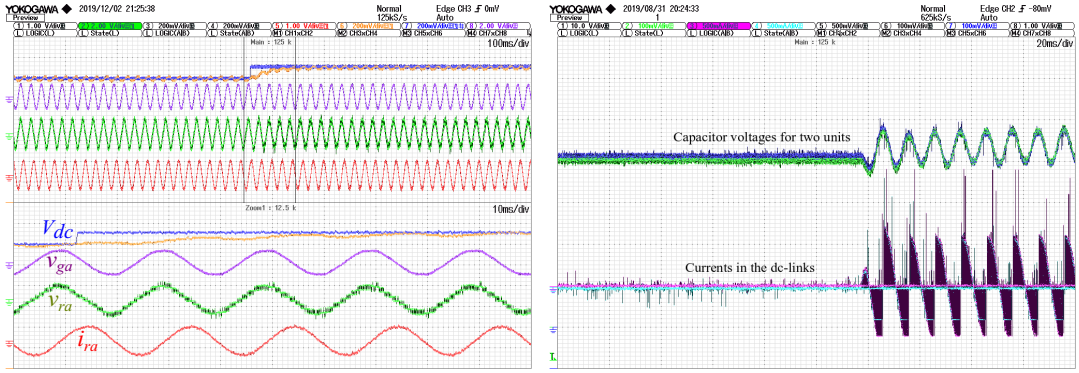
Figure 4.16: A i_{Cq} step response for 9-level SSBC STATCOM

4.5.3.4 Dynamic Response Analysis

To examine the dynamic performance of the proposed control, a step change from 0.282 p.u. to 0.352 p.u. of capacitor reference voltage is imposed and the results are captured in Fig. 4.17a. System reacts by increasing the voltage across the capacitors and accordingly reducing the M_I. Therefore, the synthesized output voltage of SSBC is reduced to seven levels. As shown in Fig. 4.17a, its takes three cycles for the average capacitor voltage to reach a steady state.

4.5.3.5 Individual Capacitor Voltage Balancing

The individual balancing control is tested for 9-level and the results for two units are shown in Fig. 4.17b. The results confirm the viablity of the individual balancing control.

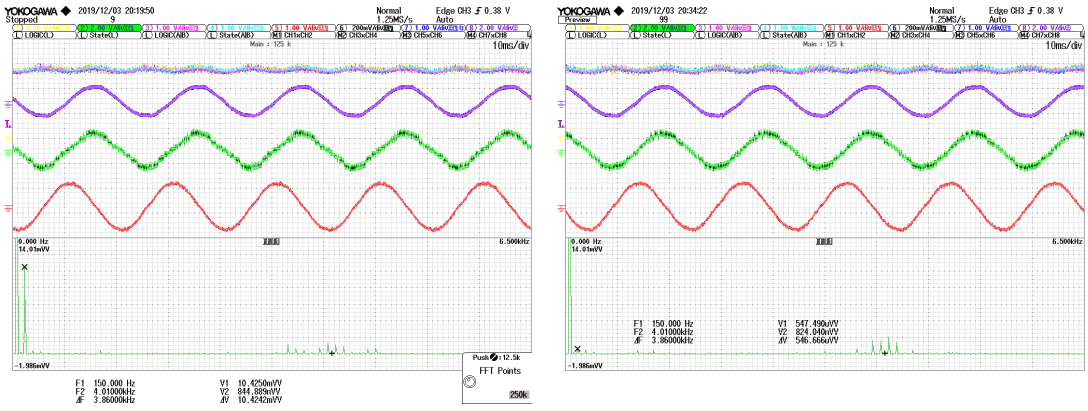


(a) (b)

Figure 4.17: (a) Response of SSBC STATCOM under capacitor voltage step test (b) Capacitor voltage balancing for two units

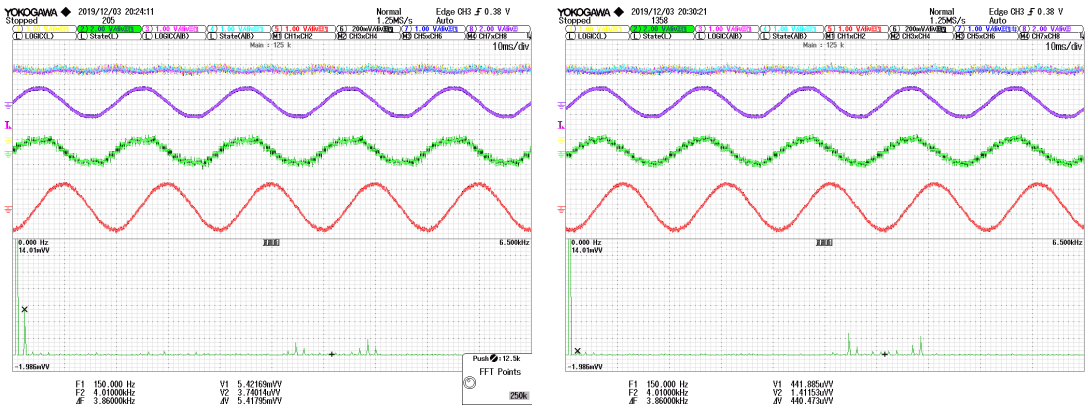
4.5.3.6 Third Harmonics Injection

To practically validate harmonics performance of STATCOM with ZSV injection, a three−phase 9−level SSBC test rig was setup using modular multilevel converter modules produced by DigiPower [53]. The rig (shown in Fig. 4.13) is connected to the grid using three step−down transformers and series inductors, $L_{ac} = 6$ mH. The results are reported in Fig. 4.18 and 4.19 for both STATCOM operation. As shown, with ZSV injection method, the third harmonic component is successfully eliminated.



(a) (b) 0.8 p.u. capacitive with ZSV injection

Figure 4.18: Hardware verification of ZSV Injection of 9−level SSBC STATCOM for 0.8 $p.u$ capacitive (a) without ZSV injection (b) with ZSV injection



(a) (b)

Figure 4.19: Hardware verification of ZSV Injection of 9−level SSBC STATCOM for 0.8 $p.u$ inductive (a) without ZSV injection (b) with ZSV injection

4.6 Summary

Modular multilevel SSBC-STATCOM control is composed of three layers which are output voltage control, internal current control and capacitor voltage balancing layers. Because of nonlinear behavior of SSBC−STATCOM system, PI regulators are not sufficient for robust and good performance. For this reason, this work is dedicated to the application of backstepping control for regulating $dc-$bus voltage of SSBC-STATCOM. The approach guarantees Lyapunov energy function, hence, enhances stability and robustness of the system. The performance of the method was tested under V_{dc} step change and variation of system impedance and verified practically. Results confirm the robustness of the proposed method compared with the conventional PI controller. In addition, detailed control design and hardware testing and implementation was discussed in this Chapter.

CHAPTER 5

OPERATION OF SSBC-STATCOM UNDER UNBALANCED CONDITIONS

5.1 Introduction

Due to sudden load changes, different losses of each converter unit, measurement errors in voltage and current sensors, and tolerance of passive elements, the voltages of dc-link capacitors are unbalanced in SSBC-STATCOM. In addition, under fault operation, the unbalanced real power within the converter phases results in more divergence of capacitor voltages and failure of the control system which affects the safety of the devices or leads to serious system collapse. Thus, ensuring the capacitor voltages balancing for SSBC-STATCOM is a fundamental and critical issue. This chapter is devoted to analysis of zero-sequence voltage (v_z) for SSBC-STATCOM using SRF and DSRF. All related issues are deeply investigated and simulation results are presented to support the analysis.

5.2 Impact of Unbalanced Conditions on Power Distribution

Fig. 5.1 shows the line-diagram of SSBC-STATCOM. Considering an unbalanced conditions, with reference to Fig. 5.1, the converter voltage and current for each phase can be written as

$$\begin{cases} v_{ra} = V^{+}e^{j\theta_v^{+}} + V^{-}e^{j\theta_v^{-}} \\ v_{rb} = V^{+}e^{j\left(\theta_v^{+}-\frac{2\pi}{3}\right)} + V^{-}e^{j\left(\theta_v^{-}+\frac{2\pi}{3}\right)} \\ v_{rc} = V^{+}e^{j\left(\theta_v^{+}+\frac{2\pi}{3}\right)} + V^{-}e^{j\left(\theta_v^{-}-\frac{2\pi}{3}\right)} \end{cases} \tag{5.1}$$

$$\begin{cases} i_{ra} = I^{+}e^{j\delta_i^{+}} + I^{-}e^{j\delta_i^{-}} \\ i_{rb} = I^{+}e^{j\left(\delta_i^{+}-\frac{2\pi}{3}\right)} + I^{-}e^{j\left(\delta_i^{-}+\frac{2\pi}{3}\right)} \\ i_{rc} = I^{+}e^{j\left(\delta_i^{+}+\frac{2\pi}{3}\right)} + I^{-}e^{j\left(\delta_i^{-}-\frac{2\pi}{3}\right)} \end{cases} \tag{5.2}$$

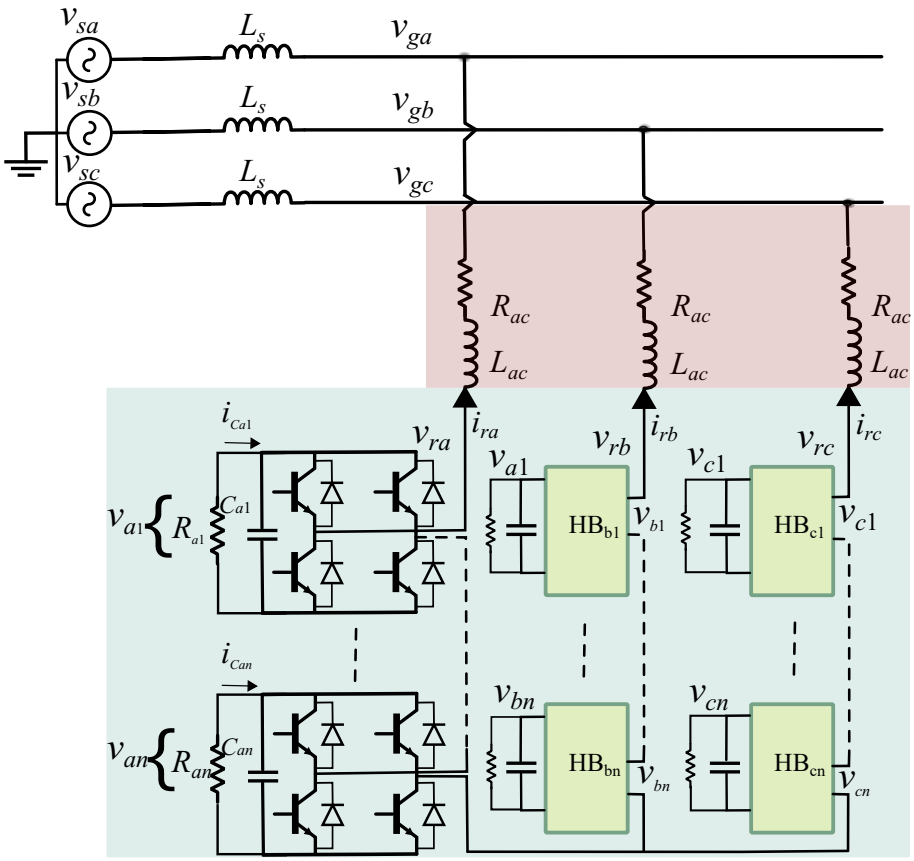


Figure 5.1: SSBC-STATCOM structure

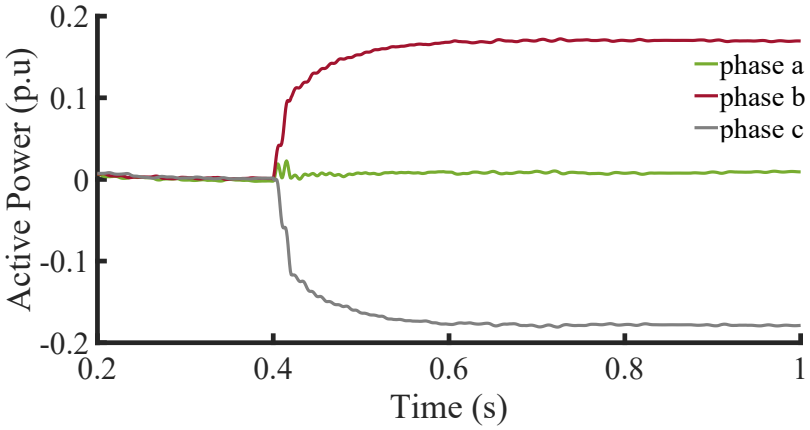
The active and reactive powers in each phase (p_a, p_b, p_c) can be calculated by the inner product of the phase current and voltage for each phase as

$$\begin{cases} p_a = \frac{V^+I^+}{2}\cos\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\cos\left(\theta_v^- - \delta_i^-\right) \\ \quad + \frac{V^+I^-}{2}\cos\left(\theta_v^+ - \delta_i^-\right) + \frac{V^-I^+}{2}\cos\left(\theta_v^- - \delta_i^+\right) \\ p_b = \frac{V^+I^+}{2}\cos\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\cos\left(\theta_v^- - \delta_i^-\right) \\ \quad + \frac{V^+I^-}{2}\cos\left(\theta_v^+ - \delta_i^- - \frac{4\pi}{3}\right) + \frac{V^-I^+}{2}\cos\left(\theta_v^- - \delta_i^+ + \frac{4\pi}{3}\right) \\ p_c = \frac{V^+I^+}{2}\cos\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\cos\left(\theta_v^- - \delta_i^-\right) \\ \quad + \frac{V^+I^-}{2}\cos\left(\theta_v^+ - \delta_i^- + \frac{4\pi}{3}\right) + \frac{V^-I^+}{2}\cos\left(\theta_v^- - \delta_i^+ - \frac{4\pi}{3}\right) \end{cases} \tag{5.3}$$

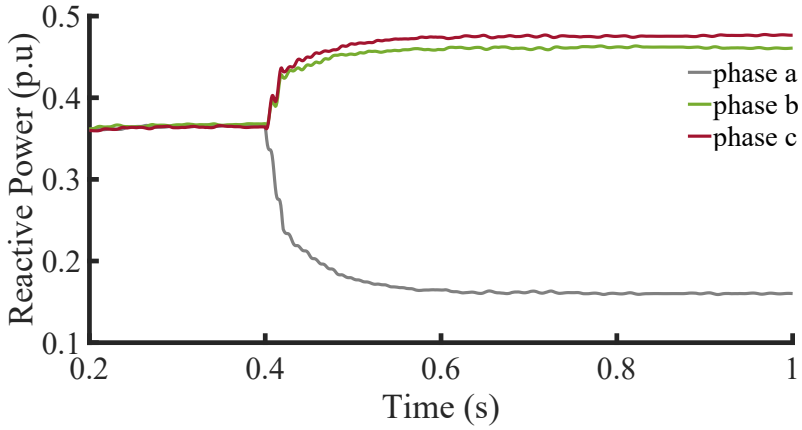
$$
\begin{cases}
q_a = \frac{V^+I^+}{2}\sin\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\sin\left(\theta_v^- - \delta_i^-\right) \\
\quad + \frac{V^+I^-}{2}\sin\left(\theta_v^+ - \delta_i^-\right) + \frac{V^-I^+}{2}\sin\left(\theta_v^- - \delta_i^+\right) \\
\\
q_b = \frac{V^+I^+}{2}\sin\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\sin\left(\theta_v^- - \delta_i^-\right) \\
\quad + \frac{V^+I^-}{2}\sin\left(\theta_v^+ - \delta_i^- - \frac{4\pi}{3}\right) + \frac{V^-I^+}{2}\sin\left(\theta_v^- - \delta_i^+ + \frac{4\pi}{3}\right) \\
\\
q_c = \frac{V^+I^+}{2}\sin\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\sin\left(\theta_v^- - \delta_i^-\right) \\
\quad + \frac{V^+I^-}{2}\sin\left(\theta_v^+ - \delta_i^- + \frac{4\pi}{3}\right) + \frac{V^-I^+}{2}\sin\left(\theta_v^- - \delta_i^+ - \frac{4\pi}{3}\right)
\end{cases}
\tag{5.4}
$$

From (5.3) and (5.4), it can be observed that each phase of the SSBC is characterised by different active and reactive powers resulting from the interaction between the positive and negative sequence components of the voltage and current. To show the effect of unbalanced condition on the operation of SSBC-STATCOM, simulation is performed when the system is injecting a negative-sequence current to the grid. For simplification, the capacitors are replaced by fixed dc-sources.

Fig. 5.2 shows the active and reactive power flowing in each phase of the SSBC configuration. The grid is balanced and the STATCOM is injecting 0.9 p.u. positive-sequence current in the grid. At $t = 0.5$s the negative-sequence current is stepped from 0 p.u. to 0.4 p.u. It is possible to observe from the figure that under this condition, different active and reactive powers will flow in each phase leg; due to the unbalanced active power flow, the divergence of dc-capacitor voltages between the phases will exist leading to system instability and degradation of the performance.



(a)



(b)

Figure 5.2: Thre phase power flow (a) active power (b) reactive power

Fig. 5.3 shows the diagram structure of the control system for SSBC-STATCOM. It can be divided into three main blocks: 1) inner current and overall balancing control, 2) individual balancing control, and 3) cluster-balancing control. In the previous chapter, a detailed description of the control strategy and its implementation has been thoroughly discussed. Therefore, in this section, detailed discussion will be devoted to the cluster balancing control based on zero-sequence method [17, 18].

5.3 Cluster Balancing Control Using Zero-Sequence Injection

5.3.1 Synchronous Reference Frame Based Control

The overall balancing control system presented in previous chapters defines the reference reactive power for the STATCOM and the necessary active power to keep

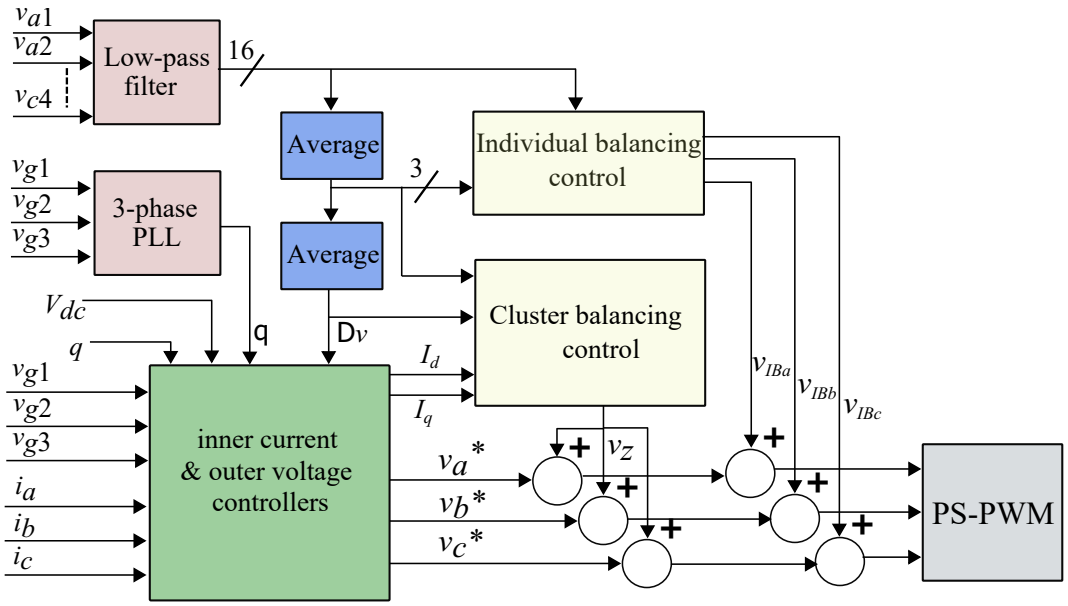


Figure 5.3: Overall control block diagram of SSBC-STATCOM

the mean *dc* capacitor voltages balanced and regulated to its reference voltage. As aforementioned, to maintain the mean *dc* capacitors voltages balanced, zero-sequence voltage (v_z) injection is necessary. The block diagram that described the cluster balancing method which achieved by injecting a common v_z into the clusters [35] is shown in Fig. 5.4

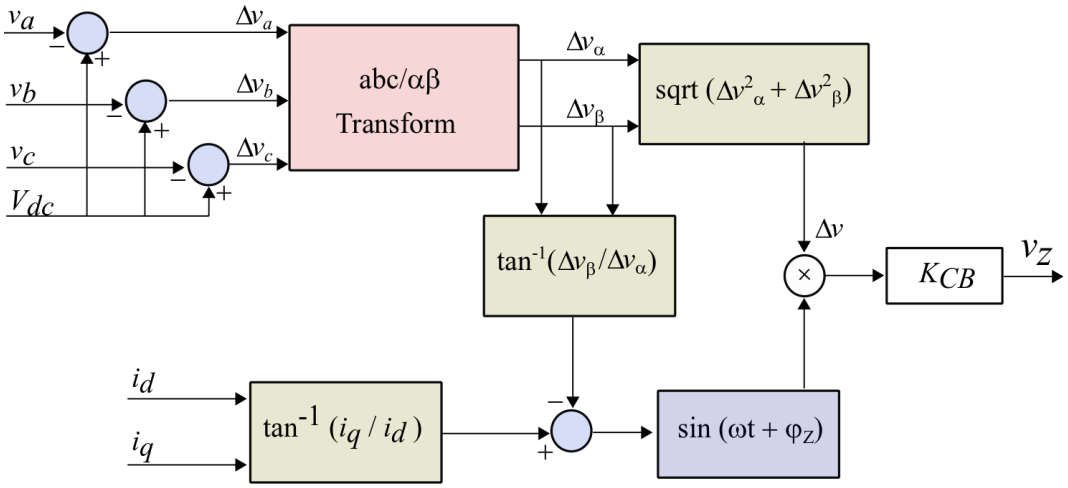


Figure 5.4: Overall control block diagram of SSBC-STATCOM

The differences between the arithmetical average *dc* capacitor voltage $\Delta\overline{v}_m$ of all the clusters, i.e., $\overline{v}_{dc}$ and the arithmetical mean *dc* capacitor voltage of each cluster $\overline{v}_m$ are obtained as follows:

$$\begin{bmatrix} \Delta\overline{v}_a \\ \Delta\overline{v}_b \\ \Delta\overline{v}_c \end{bmatrix} = \begin{bmatrix} \overline{v}_{dc} - \overline{v}_a \\ \overline{v}_{dc} - \overline{v}_b \\ \overline{v}_{dc} - \overline{v}_c \end{bmatrix} \tag{5.5}$$

Using the $abc/\alpha\beta$ transformation makes it possible to obtain the signals $\Delta\overline{v}_\alpha$ and $\Delta\overline{v}_\beta$ from the voltage differences $\Delta\overline{v}_a$, $\Delta\overline{v}_b$ and $\Delta\overline{v}_c$. The voltage differences on the abc-reference frames are transformed on the $\alpha - \beta$ reference frames as follows:

$$\begin{bmatrix} \Delta\overline{v}_\alpha \\ \Delta\overline{v}_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{5.6}$$

Thus, let $\Delta\overline{v}$ and θ_z be defined as

$$\begin{cases} \Delta\overline{v} = \sqrt{\Delta\overline{v}_\alpha^2 + \Delta\overline{v}_\beta^2} \\ \\ \theta_z = \tan^{-1}\frac{i_q}{i_d} - \tan^{-1}\frac{\Delta\overline{v}_\beta}{\Delta\overline{v}_\alpha} \end{cases} \tag{5.7}$$

Here, $\Delta\overline{v}$ is a root-mean-square value, and θ_z is a phase angle to represent a degree of the imbalance among dc capacitor voltages on the $\alpha - \beta$ reference frames. The zero-sequence voltage to be injected into each cluster can be obtained through the results from (5.7), i.e.,

$$v_z = K_{CB}\Delta\overline{v}\sin(\omega t + \theta_z) \tag{5.8}$$

The signal v_z must be added to the reference ac voltage signal of each bridge cell, as shown in Fig. 5.3. Equation (5.8) suggests that the magnitude of the zero-sequence voltage to be injected is proportional to the imbalance among the mean dc

capacitor voltages of the three clusters. The proper design of the proportional gain K_{CB} results in an accurate cluster-balancing response.

5.3.2 Analysis and Modelling of Cluster Balancing Control

The *dc* capacitor voltages in SSBC-STATCOM contain a 100-Hz component which harmfully affects the performance of the cluster balancing control. Therefore, filtering is necessary for obtaining good performance. Commonly, the low-pass filter (LPF) and moving average filter (MAF) are adopted. However, the selection of the controller gain (K_{CB}) is strongly affected under each filtering methods. This section is dedicated to discussing the design of K_{CB} taking into consideration the use of either an LPF or MAF for acquiring the mean *dc* capacitor voltages [18].

Fig. 5.5 shows the block diagram of the cluster balancing control considering phase a. The $D_a\,(s)$ represents the power loss and disturbance of phase a and $F\,(s)$ is the transfer function of the used filtering method.

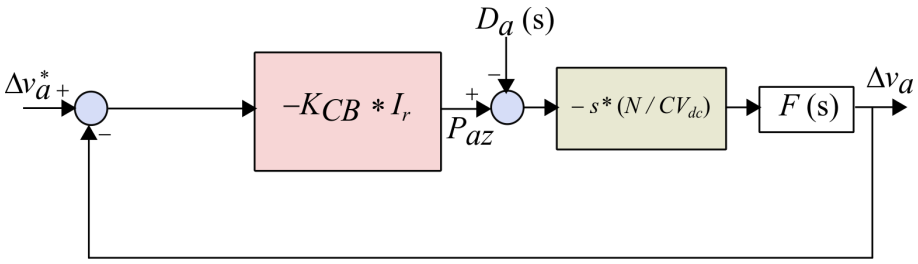


Figure 5.5: Cluster-balancing control diagram (for phase a)

5.3.2.1 Low-Pass Filter

Authors of [19] presented the use of a first-order LPF to extract the dc component from the dc capacitor voltage. The transfer function $F\,(s)$ can be given by

$$F_{LPF}\,(s) = \frac{1}{1 + sT} \tag{5.9}$$

From Fig. 5.5, the closed-loop transfer function can be written as

$$\frac{\Delta V_a}{\Delta V_a^*} = \frac{\frac{K_{CB}NI}{CV_{dc}T}}{s^2 + \frac{1}{T}s + \frac{K_{CB}NI}{CV_{dc}T}} \tag{5.10}$$

(5.10) is a second-order transfer function which allows a simple design of the damping factor ζ and natural frequency ω_n. They can be calculated as:

$$\begin{cases} \zeta = \sqrt{\frac{CV_{dc}}{K_{CB}NIT}} \\ \\ \omega_n = \sqrt{\frac{K_{CB}NI}{CTV_{dc}}} \end{cases} \tag{5.11}$$

By selecting $\zeta = 1$, K_{CB} and ω_n can be calculated using

$$\begin{cases} K_{CB} = \frac{CV_{dc}}{NIT} \\ \\ \omega_n = \frac{1}{2T} \end{cases} \tag{5.12}$$

Therefore, the cutoff frequency of the LPF must be defined to obtain the critical damping gain K_{CB}. Considering the critical damping factor ($\zeta = 1$), the response $\Delta\overline{v}_a(t)$ for a given initial value $\Delta\overline{v}_a(0)$ can be obtained from (5.10), as follows:

$$\Delta\overline{v}_a(t) = \Delta\overline{v}_a(0) \cdot (1 + \omega_n t)\, e^{-\omega_n t} \tag{5.13}$$

(5.13) depicts the response of $\Delta\overline{v}_a(t)$ when the cluster balancing control is enabled. The value of $\Delta\overline{v}_a(0)$ corresponds to the initial difference between the average dc capacitor voltage of all phases and the corresponding voltage of phase a.

5.3.2.2 Moving Average Filter

MAF has been succesfully used to eliminate the 100 Hz oscillation from dc capacitor voltage as reported in [144, 18]. The transfer function $F(s)$ using MAF is written as

$$F_{MAF}(s) = \frac{1}{N_S} \frac{1 - e^{-sN_S/f_s}}{1 - e^{-s/f_s}} \tag{5.14}$$

where f_s and N_S are the sampling frequency of the capacitor voltage and the number of samples taken by the filter. If the values of f_s is 200 kHz then the N_S is designed to be 2000 to eliminate the 100 Hz component which yields a moving window $T_{MAF} = 10$ ms. To simplify the analysis and the design of K_{CB}, the moving average filter can be approximated by first order equation as

$$F_{MAF}(s) = \frac{1}{1 + s\frac{T}{2}} \tag{5.15}$$

where T is refered as the window lenght of the filter. Note that (5.15) is obtained by approximating of the delay by the first-order $Padé$ approximation [145]. For capacitor voltage oscillation, MAF is designed to block sinusoidal disturbances of integer multiples of the frequency f_d in Hertz, i.e., $T = NT_s = 1/f_d$ (the frequency f_d is equal to twice the fundamental grid frequency $(i.e. f_d = 100\ Hz)$ for 50 Hz system.

To confirm the analysis, frequency responses using bode plots for MAF and LPF are shown in Fig. 5.6. Here, the similarity between the MAF and the LPF is clearly observed with approximation of $(T/2)$, mainly in a frequency range between 1 and 10 Hz. Thus, the critical damping gain of the cluster balancing control K_{CB} for the MAF can be obtained using the same formula of LPF described in (5.12).

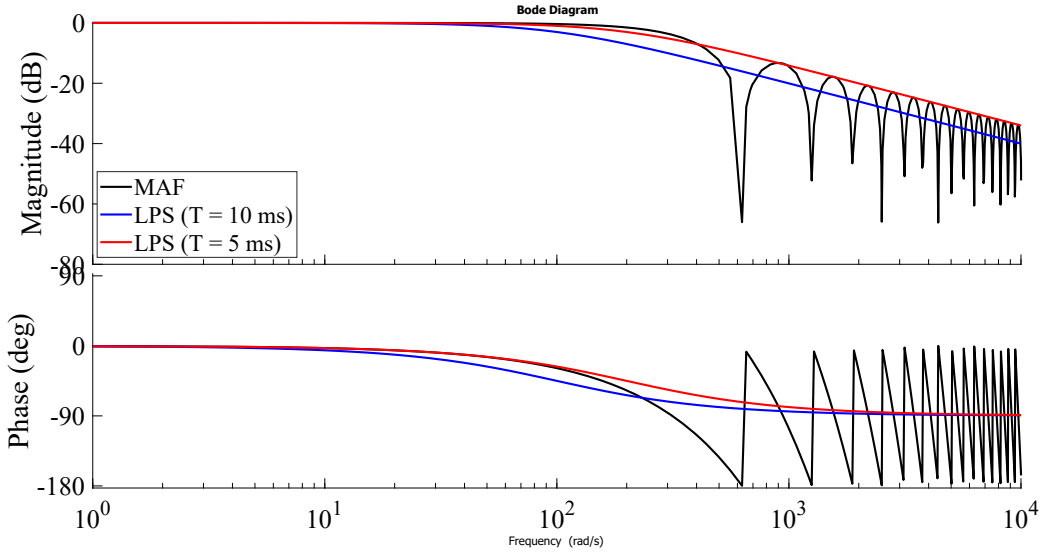


Figure 5.6: Frequency response of $F(s)$ for MAF and LPF

5.3.3 Simulation Results

5.3.3.1 Verification of Cluster Balancing Control Performance Using LPF and MAF

According to the analysis presented in 5.3.2, a cut-off frequency of 15 Hz and 32 Hz are selected for LPF and MAF respectively. Using (5.12), the values of the critical gain K_{CB} are calculated for both cases. To evaluate performance of the cluster balancing control using both filters, capacitor voltage unbalance is created by connecting different resistors in the dc-side of each H-bridge unit ($R_a = R_b = 55\,\Omega, R_c = 45\,\Omega$). The obtained results are shown in Fig. 5.7.

As can be observed, in both cases, the average dc capacitor voltages of all clusters are getting balancing and Δv (Fig. $5.7(c)$.) is reduced after the control was enabled at $t = 1\,s$. However, the oscillation caused by double-frequency component 100 Hz in the Δv remains in the case of LPF which affects steady state performance of the whole system. This can be observed from the injected v_z waveform in Fig. $5.7(d)$. In addition, the response time of cluster balancing control is much faster in the case of MAF. It should be noted that to remove the oscillation, lower cut-off frequency can be used for the LPF case but the speed response and requirements of implementation will be compromised. Using higher cut-off frequency, the controller response can be

improved, however, the oscillations will increase. Therefore, MAF outperforms LPF and brings significant improvement to the cluster balancing control.

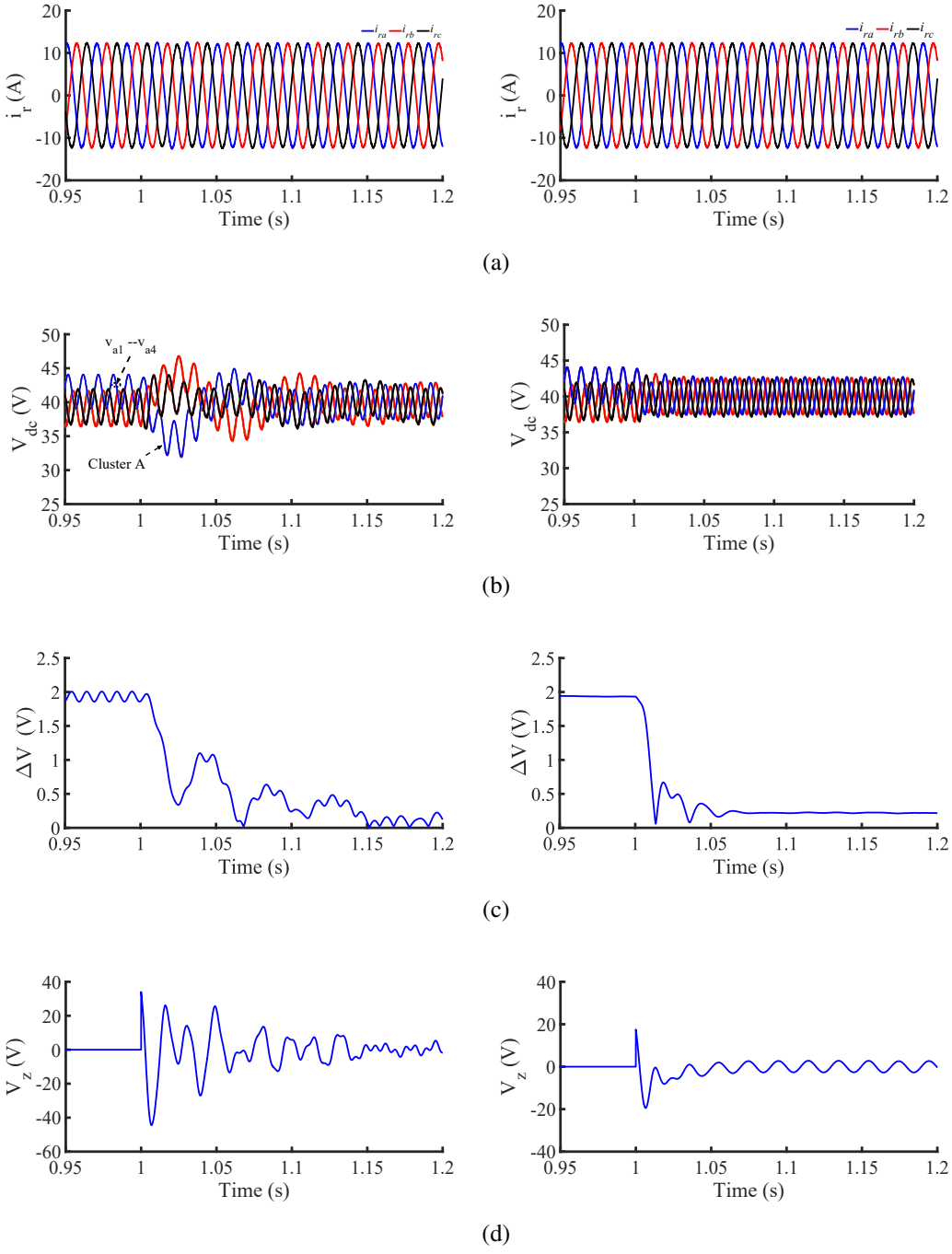


Figure 5.7: Cluster balancing control performance with LPF (left-side column) and MAF (right-side column)

5.3.3.2 Operation Under Capacitive and Inductive Modes

The results in Fig. 5.8 validates the performance cluster balancing control of the SSBC-STATCOM in both modes of operation (i.e. capacitive and inductive). The worst-case i.e. a transition from full inductive to full capacitive (-12 to 12 A) scenario is considered. As can be seen, for both methods, a rapid adjustment of reactive power is achieved with perfect balancing of the cluster capacitor voltages.

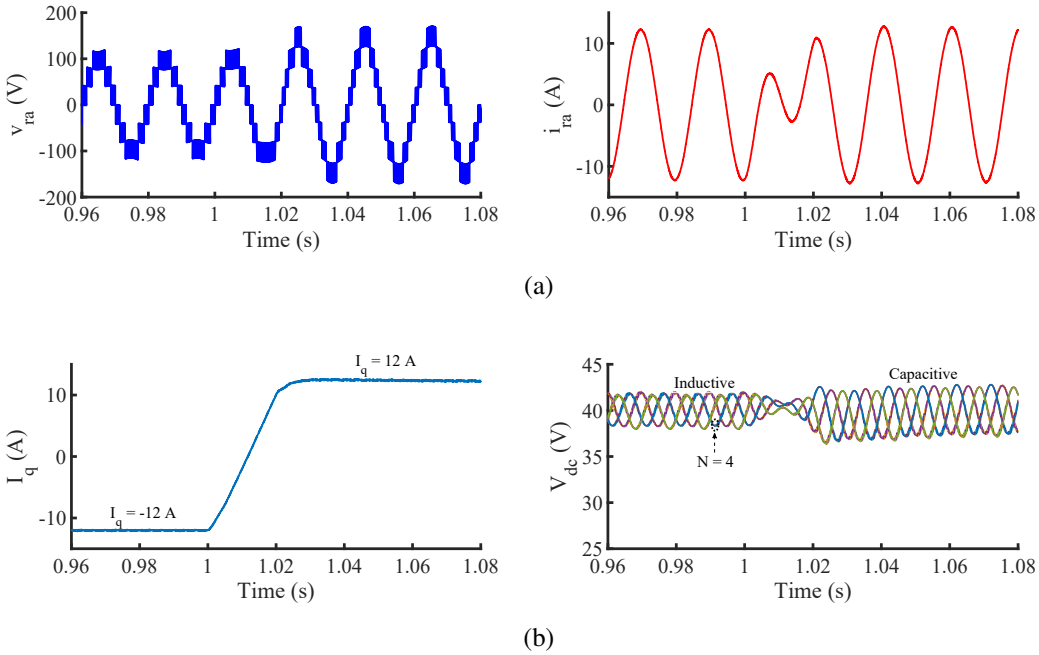


Figure 5.8: Operation of cluster balancing control under capacitive and inductive operation modes

5.3.3.3 ZVRT Capability of SSBC-STATCOM

The Distribution STATCOM (D-STATCOM) is intended for installation on distribution system. Modern grid codes have high requirements to maintain the reliability and availability of the grid during abnormal conditionns. The latest codes require inverters to operate during faults by injecting reactive power. This requirements is referred to as low/zero voltage ride-through capability (ZVRT/LVRT) [146, 147]. Thus, to guarantee seamless operation of D-STATCOM during severe faults, LVRT/ZVRT capability is necessary. As discussed before, during severe voltage sags [148, 149], the ac mains voltages become asymmetrical causing divergence in the input dc capacitor voltages which results in triggering the protection circuits of the system. Therefore, it is required to have ZVRT feature to avoid undesirable shutdown

of the STATCOM. The analysis here is applied to phase to ground faults as in the case of line faults, it is recommended to disconnect the STATCOM from the system immediately [18]. Thus, SSBC-STATCOM is subjected to the following types of sags:

1) a single-phase voltage sag with a depth of 100%.

2) a two-phase voltage sag with a depth of 100%.

3) a three-phase voltage sag with a depth of 100%.

Generally, the unbalance active power flow among the clusters resulted from the the aformentioned faults can be determined by the relationship of the asymmetrical ac mains voltages and D-STATCOM currents. In spite of that it creates capacitor voltage divergence. Therefore, the necessary zero-sequence voltage can be determined through voltage feedback control loop of the dc capacitors [113, 18].

5.3.3.4 Simulation Results for ZVRT Capability of SSBC-STATCOM

This section presents simulation results for the ZVRT capability when the SSBC-STATCOM is operated under single-, double- and three- phase sag with voltage depth of 100% and a duration of 100 ms. The voltage sag generated during 1.2 kVAr capacitive operation.

During sags, the STATCOM control supports reactive power injection with balanced current injection during all three cases (as shown in Fig. 5.9). It can be also observed that the dc-input capacitor voltages in the three cases are approximately balanced with little deviation (less than 2 V). For safety reasons, operation for 100 ms is considered after the faults occurence; for longer sags, the protection should be enabled for safety reasons.

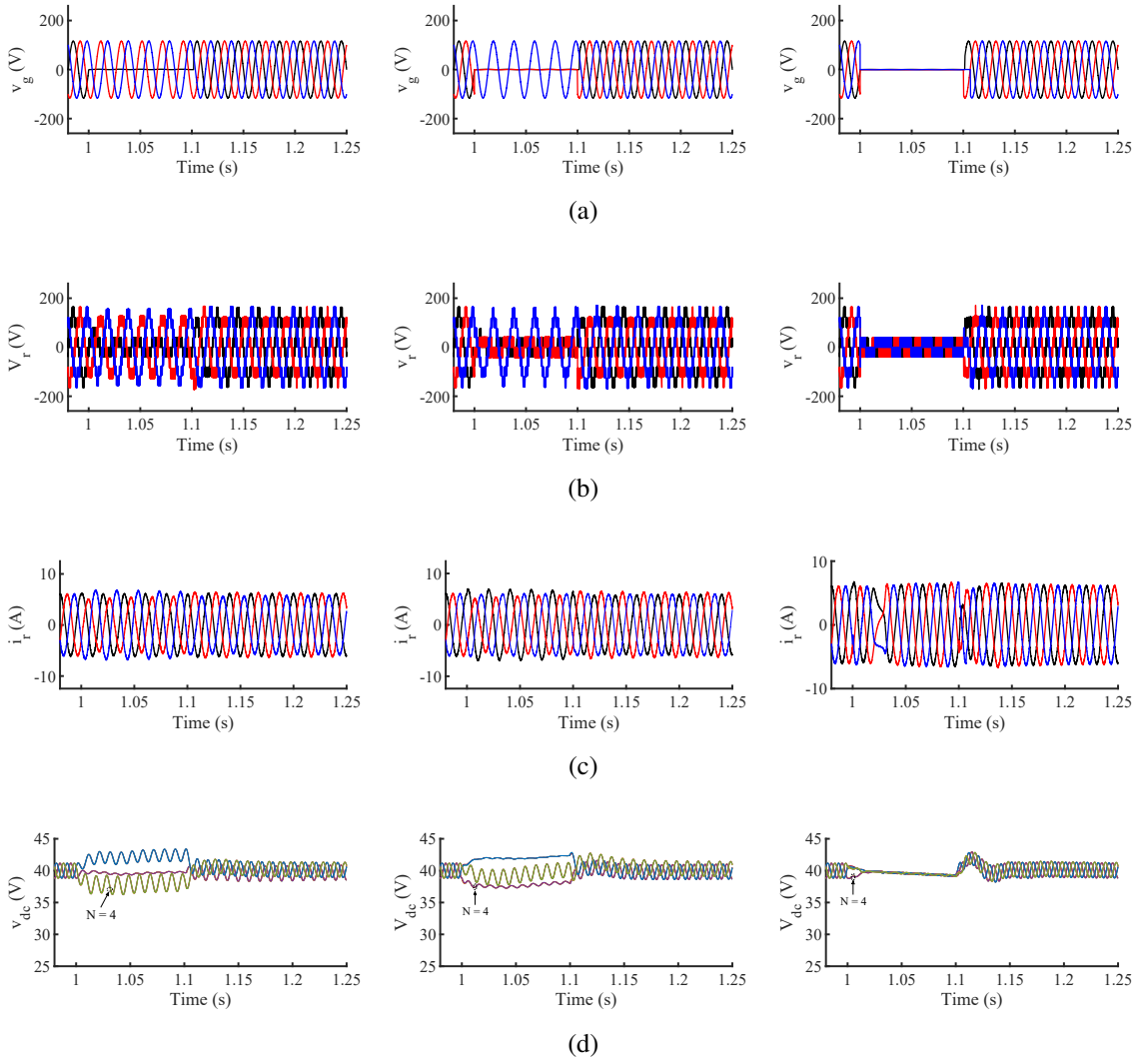


Figure 5.9: SSBC-STATCOM response during 100% single-phase, double-phase and three-phase voltage sags

5.3.4 Dual Synchrouns Current Control Scheme

In order to increase the immunity against voltage sags, grid codes have evolved from the disconnection to the ridethrough, and nowadays to the voltage support strategy. Actual grid codes include reactive current injection to support the grid voltage so that the risk of disconnection during sags could be minimized to smaller zones close to the fault location. Next generation of grid codes is being developed to achieve advanced objectives. Most of the control proposals for advanced voltage support during sags are based on symmetric sequences. The basis of these controllers is the decomposition of the unbalanced grid voltages into the positive and negative sequence voltages.

Two current controllers are used, namely, dual current controller, for separately control the positive sequence and negative sequence currents. The positive sequence is controlled in the positive synchronous reference frame (SRF), while the negative sequence is controlled in the negative SRF. The current commands appear as dc in their frame, and there is no need to build a tracking controller for an ac signal. Thus, using this scheme, it is possible to avoid expanding the bandwidth of the PI controller by increasing gains to avoid risk of making system unstable [150, 114, 151].

In the positive SRF, the positive-sequence converter voltages $v^*_{r,dq^{+1}}$ are determined by

$$v^*_{r,dq^{+1}} = V_{g,dq^{+1}} - \underbrace{\left(K_p + \frac{K_i}{S}\right)}_{PI}\left(I^*_{r,dq^{+1}} - I_{r,dq^{+1}}\right) + j\omega L_{ac} I_{r,qd^{+1}} - R_{ac} I_{r,dq^{+1}} \quad (5.16)$$

where PI denotes a PI controller. In the negative SRF, the negative-sequence converter voltages $v^*_{r,dq^{-1}}$ are determined by

$$v^*_{r,dq^{-1}} = V_{g,dq^{-1}} - \underbrace{\left(K_p + \frac{K_i}{S}\right)}_{PI}\left(I^*_{r,dq^{-1}} - I_{r,dq^{-1}}\right) - j\omega L_{ac} I_{r,qd^{-1}} - R_{ac} I_{r,dq^{-1}} \quad (5.17)$$

The terms $j\omega L_{ac} I_{r,qd^{+1}}$and $R_{ac} I_{r,dq^{+1}}$,are inserted to decouple $dq-$axes dynamics. The procedure of obtaining $\left\{V_{g,dq^{+1}}, V_{g,dq^{-1}}\right\}$ voltage components is identical to that of obtaining the $\left\{I_{r,dq^{+1}}, I_{r,dq^{-1}}\right\}$ current components which is explained in the following section.

5.3.4.1 Positive and Negative Voltage and Current Measurements

The most intuitive way to control a current vector, consisting of positive- and negative- sequence components, is to use a current controller based on two synchronous

reference frames, rotating at the fundamental grid frequency in the positive and the negative directions respectively. Equations (5.16) and (5.17) show the structure of these controllers, which is based on a double SRF (DSRF). This allows decoupling the effect of the negative-sequence voltage component on the dq-reference frame signals detected by SRF rotating with positive angular speed, and vice versa, which makes possible accurate grid synchronization under unbalanced grid faults and enhances the inner current control by seperately control the positive and negative current vectors.

The measured currents are transformed into the positive and negative reference frames by using the Park transformation, $\left[T_{dq^{+1}}\right]$ and $\left[T_{dq^{-1}}\right]$, being

$$\left[T_{dq^{+1}}\right] = \left[T_{dq^{-1}}\right]^T = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \tag{5.18}$$

It is worth pointing out that these phase angles should be estimated by an accurate grid synchronization system like the ones presented in the previous chapter. The controller in each frame uses PI controllers to regulate the injected currents. It should be noted in this figure that the terms for decoupling the dq signals (ωt) on the positive and the negative sequences have different signs, due to their opposite rotation directions.

Considering that the current vector to be injected into the grid is given by the expression

$$i = I^+ \begin{bmatrix} \sin(\omega t + \delta^+) \\ \sin\left(\omega t + \delta^+ - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \delta^+ + \frac{2\pi}{3}\right) \end{bmatrix} + I^- \begin{bmatrix} \sin(\omega t + \delta^-) \\ \sin\left(\omega t + \delta^- + \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \delta^- - \frac{2\pi}{3}\right) \end{bmatrix} \tag{5.19}$$

Its projection on the positive and negative synchronous reference frames, rotating at $+\omega t$ and $-\omega t$ respectively, can be written as

$$i_{dq^{+1}} = \begin{bmatrix} i_{d^{+1}} \\ i_{q+1} \end{bmatrix} = \begin{bmatrix} \bar{i}_{d^{+1}} \\ \bar{i}_{q+1} \end{bmatrix} + \begin{bmatrix} \tilde{i}_{d^{+1}} \\ \tilde{i}_{q+1} \end{bmatrix} = \underbrace{I^{+} \begin{bmatrix} \cos(\delta^{+}) \\ \sin(\delta^{+}) \end{bmatrix}}_{DC\ terms}$$

$$\underbrace{+ I^{-} \cos(\delta^{-}) \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + I^{-} \sin(\delta^{-}) \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix}}_{AC\ terms} \tag{5.20}$$

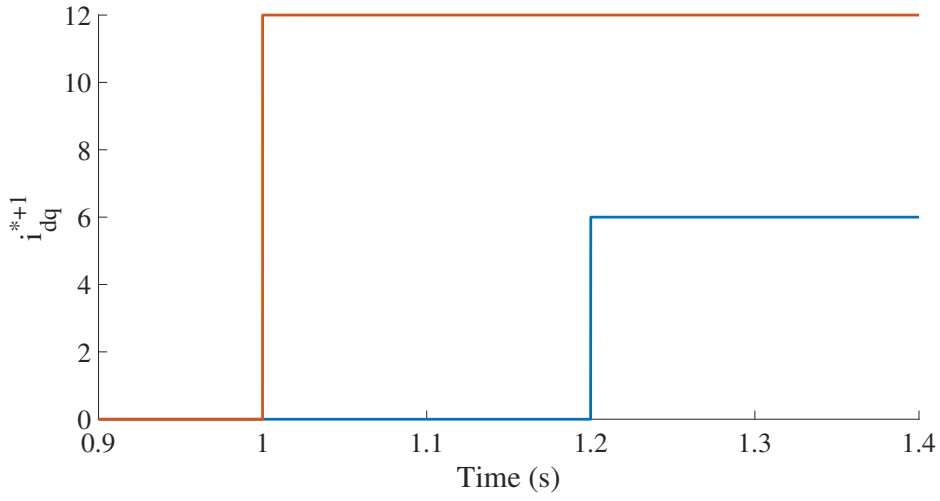
$$i_{dq^{-1}} = \begin{bmatrix} i_{d^{-1}} \\ i_{q-1} \end{bmatrix} = \begin{bmatrix} \bar{i}_{d^{-1}} \\ \bar{i}_{q-1} \end{bmatrix} + \begin{bmatrix} \tilde{i}_{d^{-1}} \\ \tilde{i}_{q-1} \end{bmatrix} = \underbrace{I^{-} \begin{bmatrix} \cos(\delta^{-}) \\ \sin(\delta^{-}) \end{bmatrix}}_{DC\ terms}$$

$$\underbrace{+ I^{+} \cos\left(\delta^{+}\right) \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + I^{+} \sin\left(\delta^{+}\right) \begin{bmatrix} -\sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix}}_{AC\ terms} \tag{5.21}$$

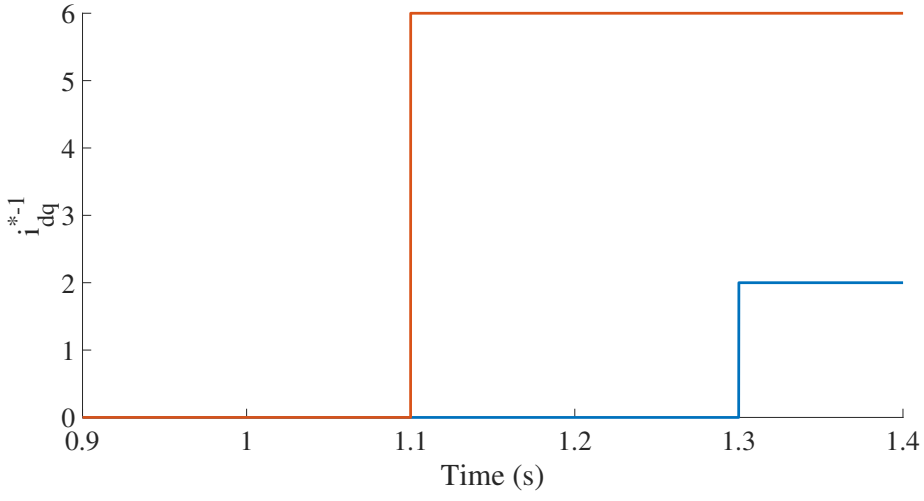
The expressions shown in (5.20) and (5.21) give evidence of the cross-coupling between the d- and q- axes signals of both synchronous reference frames. This coupling effect is manifested by a 2ω oscillation overlapping the dc signals on the dq axes, being ω the fundamental grid frequency. The amplitude of the 2ω oscillations on the dq axes of the positive-sequence reference frame matches the mean value on the dq axes of the negative-sequence one, and vice versa.

To illustrate the effect of the cross-coupling between the positive and negative reference frames, STATCOM injecting positive- and negative-sequence currents into the grid has been considered. The reference currents for this power converter, expressed on the positive and negative reference frames, I_{dq}^{*+1} and I_{dq}^{*-1} , are shown in Fig. 5.10. When the decoupled current control system is used for controlling the injection of the

reference currents shown in Fig. 5.10, the measured currents I_{dq}^{+1} and I_{dq}^{-1} , expressed on the positive and negative dq-axes are shown in Fig. 5.11. It is illustrated in this figure, how the 2ω oscillations are produced on both positive and negative sequence currents when the alternative-sequence current components are injected [151].



(a)

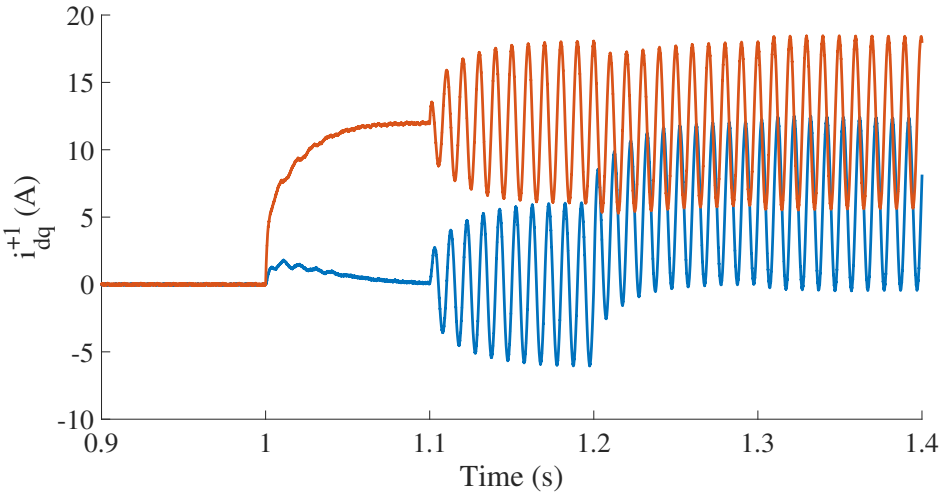


(b)

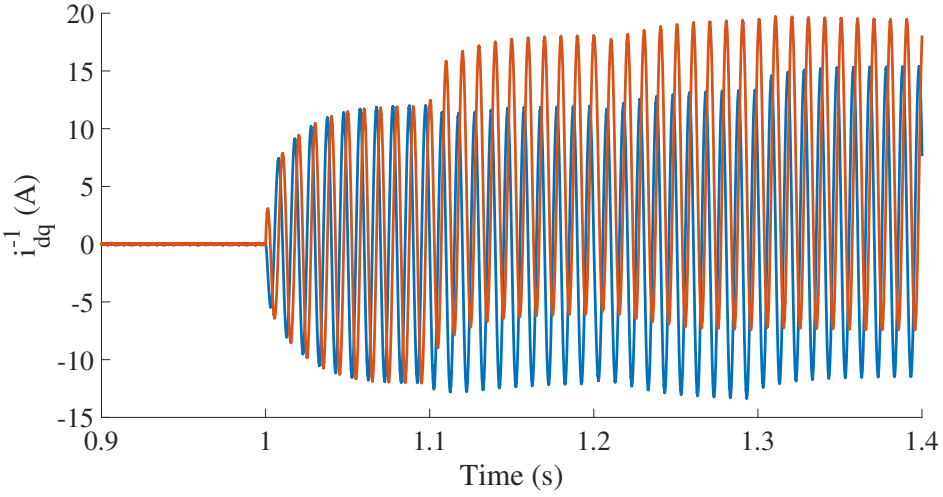
Figure 5.10: Injection of the reference currents for both positive and negative sequences

5.3.4.2 Voltage and Current Measurements Using Notch Filter

Oscillations at 2ω in the measured currents cannot be canceled out by the PI controller, which gives rise to steady-state errors when tracking the reference currents. The expressions in (5.20) and (5.21) can be written as



(a)



(b)

Figure 5.11: Measured currents for both positive and negative sequences

$$i_{dq^{+1}} = i_{dq^{+1}} = \bar{i}_{dq^{+1}} + \tilde{i}_{dq^{+1}} = \bar{i}_{dq^{+1}} + \bar{i}_{dq^{-1}} e^{-2j\omega t} \tag{5.22}$$

$$i_{dq^{-1}} = i_{dq^{-1}} = \bar{i}_{dq^{-1}} + \tilde{i}_{dq^{-1}} = \bar{i}_{dq^{-1}} + \bar{i}_{dq^{+1}} e^{2j\omega t} \tag{5.23}$$

From (5.22) and (5.23), the positive sequence appears as dc in the positive SRF, whereas the negative-sequence appears as 100 Hz ac. Similarly, the negative-sequence appears as dc in the negative SRF, whereas the positive sequence appears as 100 Hz ac.

Hence, by applying a low-pass filter or a 100-Hz notch filter to the current in the positive SRF, the positive-sequence can only be measured, and likewise, negative-sequence can be obtained. Since low-pass filter blocking 100 Hz causes instability problems because it significantly limits control bandwidth, a 100 Hz notch filter is used alternatively.

5.3.4.3 Zero-Sequence Voltage Injection

The control system of the SSBC-STATCOM must guarantee that the active power is equally distributed among the phase legs, to compensate for the system losses and keep the charge of the *dc*-input capacitors. Considering SSBC configuration, a zero-sequence voltage can be added to all phases to fulfill this requirement. Assuming an unbalanced condition of the system, the phasors of the converter phase voltage and current for phase a can be written as

$$v_{ra} = V^{+}e^{j\theta_v^{+}} + V^{-}e^{j\theta_v^{-}} + V_z e^{j\theta_z} \tag{5.24}$$

$$i_{ra} = I^{+}e^{j\delta_i^{+}} + I^{-}e^{j\delta_i^{-}} \tag{5.25}$$

Analogous relations hold for the other two phases of the converter. ZSVI allows two degrees of freedom, in terms of amplitude (V_z) and angle (θ_z) of the injected zero-sequence voltage. The goal is to find a suitable value for V_z and θ_z to remove the interaction between the sequence components and thus provide an uniformactive power distribution among phases. Considering phases a and b and considering zero-sequence voltage injection, the total active power can be written as

$$\begin{cases} p_a = \frac{V^+I^+}{2}\cos\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\cos\left(\theta_v^- - \delta_i^-\right) \\ \quad + \frac{V^+I^-}{2}\cos\left(\theta_v^+ - \delta_i^-\right) + \frac{V^-I^+}{2}\cos\left(\theta_v^- - \delta_i^+\right) \\ \quad + \frac{V_zI^-}{2}\cos\left(\theta_z - \delta_i^-\right) + \frac{V_zI^+}{2}\cos\left(\theta_z - \delta_i^+\right) \\ \\ p_b = \frac{V^+I^+}{2}\cos\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\cos\left(\theta_v^- - \delta_i^-\right) \\ \quad + \frac{V^+I^-}{2}\cos\left(\theta_v^+ - \delta_i^- - \frac{4\pi}{3}\right) + \frac{V^-I^+}{2}\cos\left(\theta_v^- - \delta_i^+ + \frac{4\pi}{3}\right) \\ \quad + \frac{V_zI^-}{2}\cos\left(\theta_z - \delta_i^- - \frac{2\pi}{3}\right) + \frac{V_zI^+}{2}\cos\left(\theta_z - \delta_i^+ + \frac{2\pi}{3}\right) \end{cases} \tag{5.26}$$

The first two terms in (5.26) indicate the active power expressions associated with the positive and negative-sequence components. These terms are equal in all phases and can be controlled through the overall dc-link voltage controller**.** The third and fourth terms denote the active power generated by the interaction between positive- and negative sequence components. This interaction is responsible for the uneven power distribution between the phases. Finally, the last two terms are the active power terms generated by the ZSVI. Two main components in (5.26) can be identified as an active power component that is common between the phases (P_{nom}) and a component caused by the interaction between the different sequences $\left(P_{difm}\right)$ where $m = a, b, c$ as

$$\begin{cases} p_{nom} = \frac{V^+I^+}{2}\cos\left(\theta_v^+ - \delta_i^+\right) + \frac{V^-I^-}{2}\cos\left(\theta_v^- - \delta_i^-\right) \\ \\ p_{difa} = \frac{V^+I^-}{2}\cos\left(\theta_v^+ - \delta_i^-\right) + \frac{V^-I^+}{2}\cos\left(\theta_v^- - \delta_i^+\right) \\ \quad + \frac{V_zI^-}{2}\cos\left(\theta_z - \delta_i^-\right) + \frac{V_zI^+}{2}\cos\left(\theta_z - \delta_i^+\right) \\ \\ p_{difb} = \frac{V^+I^-}{2}\cos\left(\theta_v^+ - \delta_i^- - \frac{4\pi}{3}\right) + \frac{V^-I^+}{2}\cos\left(\theta_v^- - \delta_i^+ + \frac{4\pi}{3}\right) \\ \quad + \frac{V_zI^-}{2}\cos\left(\theta_z - \delta_i^- - \frac{2\pi}{3}\right) + \frac{V_zI^+}{2}\cos\left(\theta_z - \delta_i^+ + \frac{2\pi}{3}\right) \end{cases} \tag{5.27}$$

Under ideal conditions, the interaction between sequences is the only disturbing factor that leads to the uneven power distribution between the different phases. Therefore, calculating an appropriate zero-sequence voltage amplitude and phase that makes $p_{difa} = p_{difb} = 0$ will be sufficient to guarantee the balancing of the dc-

capacitor voltages. However, in practical applications, other factors (such as different components characteristics) will impact the active power flowing in the phase legs. Therefore, (5.27) can be solved for a generic case to find the appropriate zero-sequence voltage. By introducing two new variables κ_1 and κ_2, defined as

$$\kappa_1 = \frac{V^+ I^-}{2} \cos\left(\theta_v^+ - \delta_i^-\right) + \frac{V^- I^+}{2} \cos\left(\theta_v^- - \delta_i^+\right) \tag{5.28}$$

$$\kappa_2 = \frac{V^+ I^-}{2} \cos\left(\theta_v^+ - \delta_i^- - \frac{4\pi}{3}\right) + \frac{V^- I^+}{2} \cos\left(\theta_v^- - \delta_i^+ + \frac{4\pi}{3}\right) \tag{5.29}$$

Expanding the cosine terms in (5.26), p_{difa} and p_{difb} can be rewritten as

$$\begin{aligned} p_{difa} = \kappa_1 + V_z \cos(\theta_z) \underbrace{\left[\frac{I^-}{2} \cos\left(\delta_i^-\right) + \frac{I^+}{2} \cos\left(\delta_i^+\right)\right]}_{\kappa_3 = \frac{1}{2}\Re\{i_{ra}\}} + \\ + V_z \sin(\theta_z) \underbrace{\left[\frac{I^-}{2} \sin\left(\delta_i^-\right) + \frac{I^+}{2} \sin\left(\delta_i^+\right)\right]}_{\kappa_4 = \frac{1}{2}\Im\{i_{ra}\}} \\ p_{difb} = \kappa_2 + V_z \cos(\theta_z) \underbrace{\left[\frac{I^-}{2} \cos\left(\delta_i^- + \frac{2\pi}{3}\right) + \frac{I^+}{2} \cos\left(\delta_i^+ - \frac{2\pi}{3}\right)\right]}_{\kappa_5 = \frac{1}{2}\Re\{i_{rb}\}} + \\ + V_z \sin(\theta_z) \underbrace{\left[\frac{I^-}{2} \sin\left(\delta_i^- + \frac{2\pi}{3}\right) + \frac{I^+}{2} \sin\left(\delta_i^+ - \frac{2\pi}{3}\right)\right]}_{\kappa_6 = \frac{1}{2}\Im\{i_{rb}\}} \end{aligned} \tag{5.30}$$

The set of equations above can be simplified in order to isolate the terms that involve the zero-sequence voltage as

$$p_{difa} = \kappa_1 + \kappa_3 V_z \cos(\theta_z) + \kappa_4 V_z \sin(\theta_z)$$
$$p_{difb} = \kappa_2 + \kappa_5 V_z \cos(\theta_z) + \kappa_6 V_z \sin(\theta_z) \tag{5.31}$$

where $\kappa_3, \kappa_4, \kappa_5, \kappa_6$ have the meaning as indicated in (5.30). Solving (5.31), the phase angle and amplitude of the zero-sequence voltage are

$$\theta_z = \arctan \frac{(p_{difb}-\kappa_2)\kappa_3-(p_{difa}-\kappa_1)\kappa_5}{(p_{difa}-\kappa_1)\kappa_6-(p_{difb}-\kappa_2)\kappa_4}$$
$$V_z = \frac{p_{difa}-\kappa_1}{\kappa_3\cos(\theta_z)+\kappa_4\sin(\theta_z)} = \frac{p_{difb}-\kappa_2}{\kappa_5\cos(\theta_z)+\kappa_6\sin(\theta_z)} \tag{5.32}$$

5.3.4.4 Operation Range of SSBC-STATCOM Using ZSVI

According to (5.32) and based on the variables $\kappa_1 - \kappa_6$ in (5.32), it is possible to conclude that the SSBC is mainly sensitive to the amount of positive- and negative-sequence currents that the converter exchanges with the grid. To analyse the sensitivity of the ZSVI, two case studies are investigated. It is assumed that the grid is balanced (thus, the grid voltage is only constituted by a positive-sequence component) while the converter is exchanging both positive- and negative-sequence current with the grid. For simplicity, two operating conditions are here considered: *i*) the two current sequences have the same phase angle (for example, both positive- and negative-sequence currents are injected into the grid), *ii*) the current sequences are opposite in phase (for example, positive-sequence current is injected into the grid while the negative-sequence is absorbed by the compensator). Table 5.1 summarizes the different sequence components for the considered cases. The corresponding zero-sequence voltage are calculated using (5.32).

Table 5.1: Calculation of zero-sequence voltage for different combination of positive and negative sequence quantities

	v^+, θ_v^+	v^-, θ_v^-	i^+, δ_i^+	i^-, δ_i^-	v_z
SSBC-STATCOM	$V^+, 0$	$0, 0$	$I^+, \pm\frac{\pi}{2}$	$I^-, \pm\frac{\pi}{2}$	$\frac{A}{\sqrt{3}(I^{-2}-I^{+2})}$
	$V^+, 0$	$0, 0$	$I^+, \mp\frac{\pi}{2}$	$I^-, \pm\frac{\pi}{2}$	$\frac{B}{\sqrt{3}(I^{-2}-I^{+2})}$

Other parameters in Table 5.1 are defined as follow:

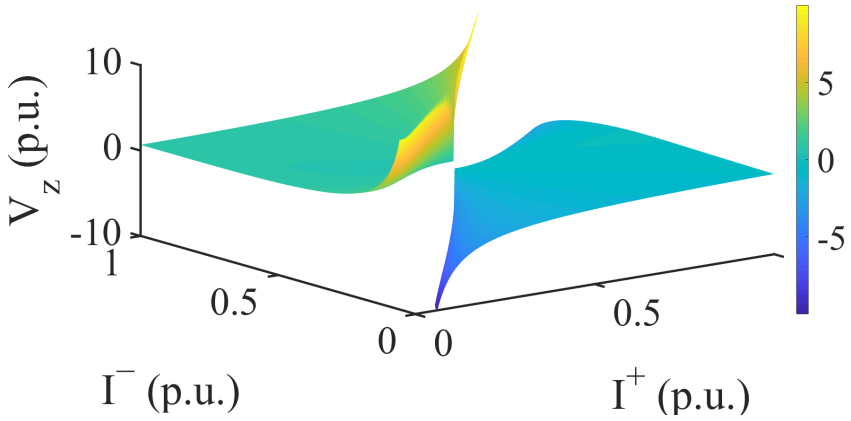
$$A = \sqrt{C^2 \left(I^- + I^+\right)^2 + 12 \left(I^- - I^+\right)^2 p_{difa}^2}$$
$$B = \sqrt{C^2 \left(I^- - I^+\right)^2 + 12 \left(I^- + I^+\right)^2 p_{difa}^2} \tag{5.33}$$

with

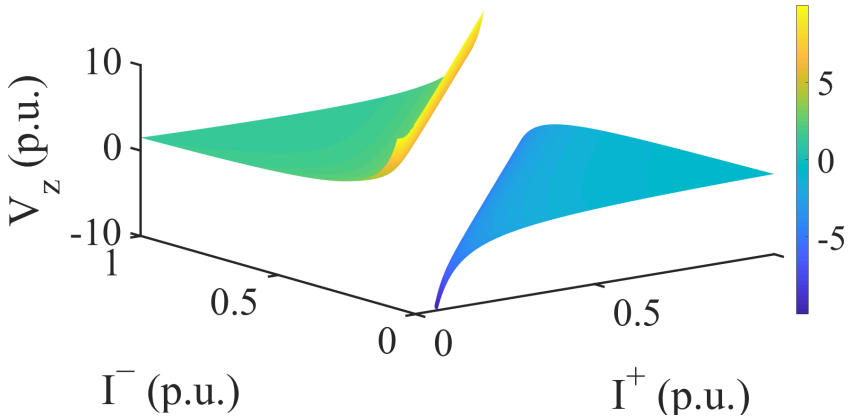
$$C = 2p_{difa} \ + 4p_{difb} - \sqrt{3}V^+ I^- \tag{5.34}$$

The solution for the zero-sequence voltage shows that a practical limitation exists with an infinite zero-sequence requirement needed under specific operating conditions. In the specific, the operating range is limited by the degree of unbalance (I^-/I^+). From Table 5.1, it can be observed that v_z tends to infinity when the ratio (I^-/I^+) approaches 1, i.e. a theoretically infinite voltage for the reference point voltage to allow power distribution among phases when the amplitude of the exchanged negative-sequence current equals the amplitude of the positive-sequence. In practical applications, the maximum attainable output voltage of the converter leg will determine the maximum degree of unbalance that the converter can cope with before losing the controllability of the *dc*-link voltages. It is of importance to stress that the singularity is independent of the assumptions in Table 5.1 and will occur in any unbalanced condition if the current ratio tends to 1.

Fig. 5.12 shows the relation between positive- and negative-sequence currents and zero-sequence voltage amplitude for SSBC-STATCOM when $\delta_i^+ = \delta_i^- = \frac{\pi}{2}$ and $\delta_i^+ = -\delta_i^- = \frac{\pi}{2}$. For simulation, V^+ is equal to 1 p.u. while p_{difa} and p_{difb} are set to 0.2 p.u. and 0.1 p.u. respectively. It can be observed that in both operating conditions, the singularity occurs when $I^+ = I^-$.



(a)



(b)

Figure 5.12: Relationship between zero-sequence voltage and positive- and negative-sequence currents for SSBC-STATCOM (a) $\delta_i^+ = \delta_i^- = \frac{\pi}{2}$ (b) $\delta_i^+ = -\delta_i^- = \frac{\pi}{2}$

It is possible to observe from Fig. 5.12 that although SSBC-STATCOM is sensitive to the degree of unbalanced in the current, the required amount of zero-sequence component needed for capacitor balancing also highly depends on the relative phase-shift between the sequence components. For this reason, it is of interest to investigate the impact of the relative phase-shift between the current sequence components on the required amount of zero-sequence voltage.

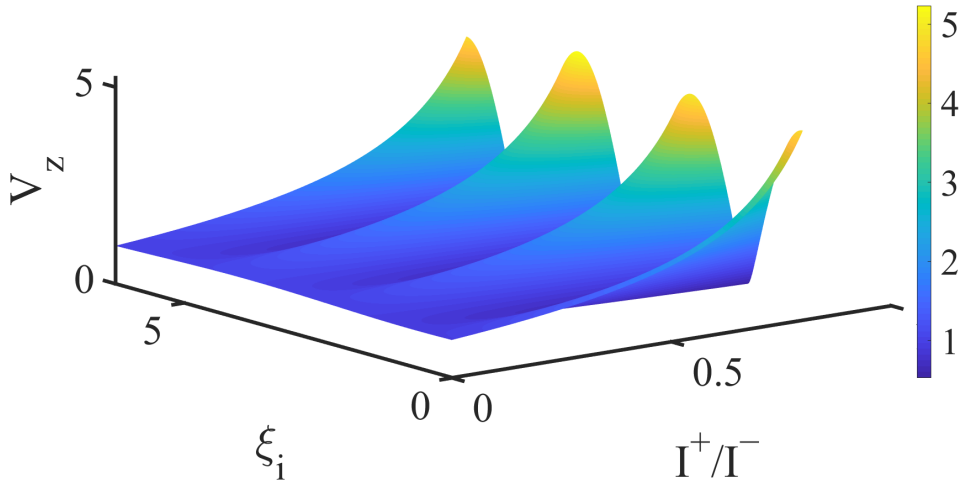


Figure 5.13: Relationship between zero-sequence voltage and phase-shift between positive and negative sequence currents for SSBC-STATCOM

Fig. 5.13, depicts the relationship between the magnitude of zero-sequence voltage V_z and the phase-shift (ξ_i) between the current components for different degree of unbalance of the injected currents (I^-/I^+). It is observed that the highest zero-sequence voltage is required when the positive and negative sequence currents are aligned which corresponds to $2\pi/3, 4\pi/3$ and 2π phase-shifts. While the lowest demand for zero voltage injection occurs when the two components are in opposite phase ($i.e.\pi/3, \pi, 5\pi/3$).

5.3.4.5 Simulation Results

When STATCOM is employed for industrial applications such as flicker mitigation, the goal is to control both positive and negative sequence components. The results of SSBC-STATCOM operating with DSRF based ZSI method is shown in Fig. 5.14. As expected from the previous analysis, an increase of the degree of the unbalance represented by I^-/I^+ (i.e. Fig. 5.14a) leads to a higher required amplitude of the zero-sequence voltage as shown in Fig. 5.14f. The control has deteriorated when $I^- = I^+ = 1$. The results verify the viability of the control to maintain the capacitor voltage well-balanced.

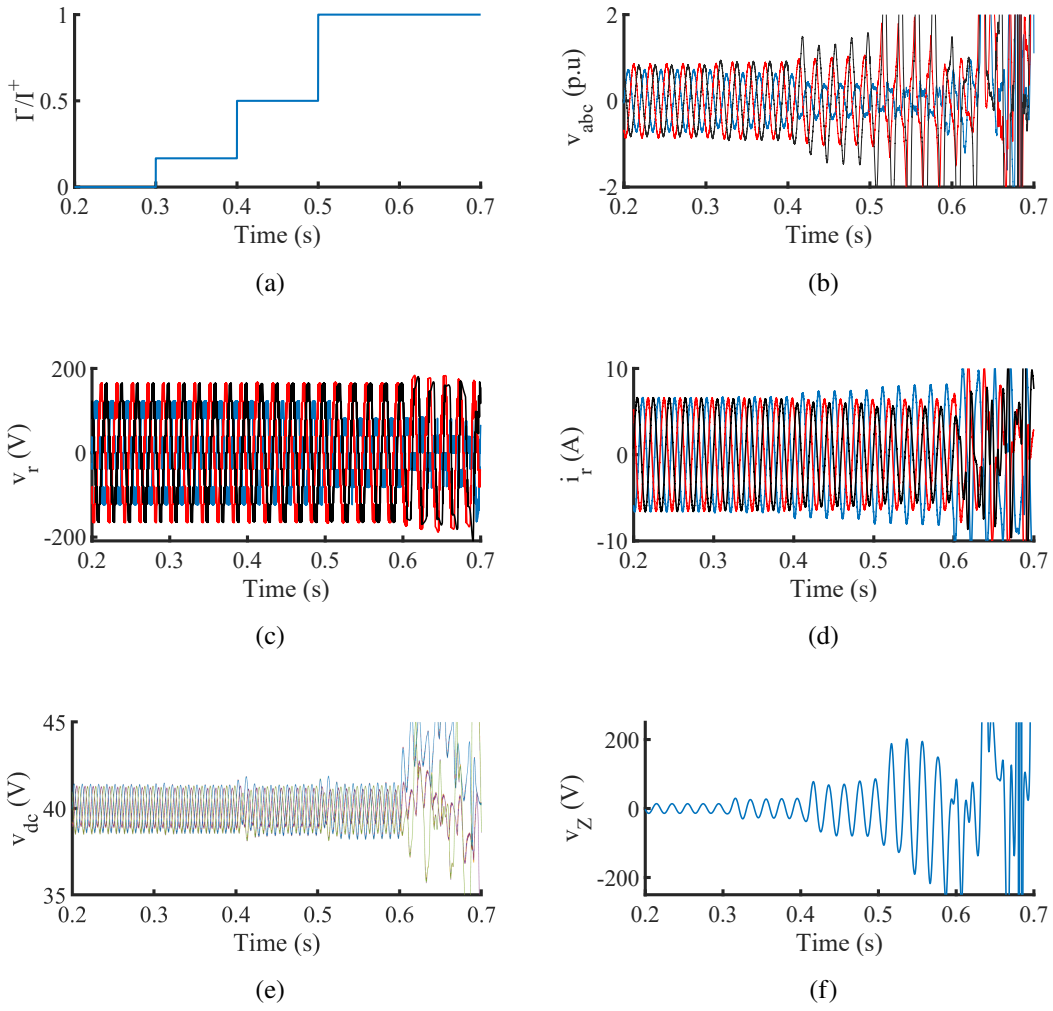


Figure 5.14: Simulation results of DSRF operation with ZSI method (a) I^-/I^+(b) modulating signals (c) output voltage (d) line current (e) capacitor voltages (f) zero sequence voltage

5.4 Summary

In this chapter, the effect of the unbalanced operation on SSBC-STATCOM has been investigated. Zero-sequence voltage allows maintaining the dc-link voltage of the different cells balanced in case of unbalanced operation. Analysis is devoted to zero-sequence voltage (v_z) SRF and DSRF control scheme. All related issues are deeply investigated and simulation results are presented to support the analysis. For the first case, the design is carried out considering the use of either MAF or LPF to mitigate the second harmonics oscillating component that appears on the dc voltage. Consequently, the improved performance of MAF based cluster balancing control is confirmed. Besides, simulation results verified the viability of the method under severe

sags. For industrial applications that require both positive and negative sequence control, DSRF based zero-sequence voltage injection is introduced. It has been shown that there are special operating conditions where the zero-sequence component is unable to control the active power in each phase to zero. This is due to a singularity that exists in the solution for the calculation of the zero-sequence components. The singularity is governed by the equality between the positive- and the negative-sequence component of the injected current.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Summary

The thesis starts by giving an overview of FACTS devices. Their role and classification are addressed. A comparison between the traditional shunt devices (i.e. SVC) and STATCOM is made. Due to the limitation of the SVCs, i.e. bulky size, high installation cost, and slow response time, the STATCOM is increasingly used for reactive power compensation and power quality improvement in the distribution and transmission of electrical power. A detailed literature review on STATCOM is covered. This includes the inverter topologies, control strategies, and modulation techniques. The comparison between various MVSI topologies is made and the superiority of Single-Star Bridge-Cell (SSBC) for STATCOM is highlighted. To directly connect a STATCOM to the point of common coupling and to improve the performance of the harmonics of the output voltage, higher levels of SSBC is required. Therefore, the work investigates the effect of increasing the number of levels on the design and implementation cost of SSBC STATCOM power components (active and passive components). A detailed study is done on the proper design of the STATCOM components to achieve commercial satisfaction and stable performance. The effect of each active and passive components on the performance is investigated. The work tries to disclose the relationship between the STATCOM implementation cost and the number of levels in both low and medium voltage systems. Two case studies are considered for this purpose (i.e. 400V and 11kV). The outcomes of this analysis can be extended to other multilevel topologies.

In terms of the STATCOM control, the two commonly used control approaches, namely the direct and indirect control schemes are critically compared. For a fast and efficient control of reactive power, the direct control scheme (i.e. based on controllable M_I) is favored. Multilevel SSBC-STATCOM direct control is composed of three layers which are output voltage control, internal current control, and capacitor voltage

balancing. Although PI regulators are commonly used for their simplicity and ease in the implementation, the STATCOM system is essentially nonlinear, therefore, in this work, a nonlinear controller a backstepping nonlinear control based on Lyapunov function design is proposed to regulate the overall capacitor voltage and hence improve the performance and robustness. Besides, detailed control design and implementation of the proposed control of SSBC-STATCOM using FPGA is discussed. The performance of the method was tested under V_{dc} step change and variation of system impedance and compared with the PI control approach. The phase-shifted PWM (PS-PWM) method is selected in this work to be a competitive alternative for the direct control scheme of the STATCOM due to its inherited capability of equal distribution of power and semiconductor stress among H-bridge units, easy to be implemented and perfectly suitable for the commonly hierarchical control scheme. To use the PS-PWM in the direct control of 9-level SSBC STATCOM, the switching angles of each H-bridge are determined by comparing (on-line) low-frequency reference (i.e. modulation) with high-frequency triangular signal (i.e. carrier). The modulation signal is implemented using FPGA considering other balancing control layers (individual and cluster balancing control layers). The practical implementation of the PS-PWM method has been discussed in detail. To verify the performance of the proposed control with all other layers control, a simulation model of 9-level SSBC STATCOM using Matlab/Simulink is developed, and steady-state and dynamic performance are discussed in detail. Hardware verification of the presented system and control design is conducted using 142 V 2 kVAr SSBC based STATCOM. The results verify the effectiveness of the design and give practical guidance on testing and implementation.

Because of the nonlinear behavior of the SSBC-STATCOM system, PI regulators are not sufficient for robust and good performance. For this reason, the work was dedicated to the application of backstepping control for regulating the dc-bus voltage of SSBC-STATCOM. The approach guarantees Lyapunov energy function, hence, enhances the stability and robustness of the system. The performance of the method was tested under V_{dc} step change and variation of system impedance and verified practically.

To guarantee seamless operation of STATCOM during severe faults, Low Voltage Voltage Ride Through (LVRT) capability is necessary. During severe voltage sags, the ac mains voltages become asymmetrical causing divergence in the input dc capacitor voltages which results in triggering the protection circuits of the system. Therefore, it is required to have an LVRT feature to avoid an undesirable shutdown of the SSBC STATCOM. Thus, in this thesis, a thorough analysis is done to study the system and unbalance condition. The method of Zero-sequence voltage (v_z) is used to balance the capacitor voltage by adding its waveform to the three-phase ac voltages of the SSBC converter. It can redistribute the active powers between the three clusters without drawing a negative sequence current. Since v_z only changes the virtual reference potential point of the SSBC, it does not affect the line to line voltages and correspondingly currents, thus it produces no effect on the total power. Mathematical derivation of the v_z using positive and negative sequence is provided and control of STATCOM is simulated with the dual synchronous current control scheme.

6.2 Conclusion

Due to the disadvantages of high cost and large size of transformer-based two-level converters solution for STATCOM, multilevel converters based solutions are alternatively utilized. However, the selection of the number of levels has a direct impact on system design, performance, and cost. Besides, from the control point of view, the capacitor voltage balancing is a fundamental issue for the correct operation of the system. Thus, this work is dedicated to exploring the impact of increasing the number of levels on the STATCOM design connected to different voltage levels. A detailed explanation about the control of STATCOM considering capacitor voltage balancing under balanced and unbalanced grid is investigated. For increasing the stability of the control, the backstepping control design approach is introduced. The system design and control implementation are targeted for 9-level SSBC STATCOM. Comprehensive simulation and experimental results are provided for the validation of system and control design.

As cost and reliability are the main detrimental factors, this study highlights the component cost-effectiveness of different levels for 400 V and 11 kV STATCOMs. The results show that the cost of the 400 V system is proportional to the number of gate

drivers and capacitor voltage sensors. Thus, the solution for the optimal design of these two components is required to adopt a higher number of levels. In contrast, for medium voltage application (e.g. 11 kV system), it is recommended to adopt higher levels as the cost is dramatically decreased due to the cost of power switches and dc capacitors. In this way of design, the harmonics' performance is initially set to fulfill the IEEE 519 standard in which it indicates the operating switching frequency. Accordingly the other passive and active components can be selected. It should be noted that a tradeoff is always considered to come up with the perfect design.

Although PI regulators are commonly used for their simplicity and ease in the implementation, the STATCOM system is essentially nonlinear, therefore, in this work, a backstepping nonlinear control based on Lyapunov function design is proposed to regulate the overall capacitor voltage. Besides, detailed control design and implementation of the proposed control of SSBC-STATCOM using FPGA is discussed. Experimental set-up was designed to verify the results practically which confirmed the robustness and stability of the proposed control approach. In addition, the performance of the proposed method under V_{dc} step change and variation of system impedance has been analyzed and results were compared with the traditional PI controller. Besides, simulation results is presented to demonstrate the advantage of the proposed control for post-fault operation, which will enhance both system reliability and availability.

FPGAs, with their parallelism capability, prove to be more suitable for implementing control of SSBC-STATCOM. A higher number of levels increases modulation complexity due to the higher number of switches that need to be controlled. For the digital implementation of STATCOM control, digital signal processors (DSPs) and field-programmable gate arrays (FPGAs) are preferred options. However, due to the limitation of I/O built-in pins in typical DSPs, FPGAs are becoming dominant to be used for pulse modulation in MMCC based systems. Therefore, in addition to the achieved cost reduction from the easy configuration of FPGA hardware resources for specific applications, a dramatical reduction of execution time can be achieved due to the potential parallelism offered by FPGAs, hence significant performance is obtained compared to software-based processors. In this work, detailed control implementation

of SSBC-STATCOM using Cyclone V FPGA is discussed and the results are verified using 142 V SSBC-STATCOM hardware set-up.

6.3 Future Work

The focus of this thesis was to design and implement a PS-PWM-based direct control scheme for SSBC STATCOM. To improve its robustness, a backstepping design control approach is adopted. The work illustrates the internal control of the system considering the unbalanced condition and the system is designed considering Insulated Gate Bipolar Transistor (IGBT). However, considering the evolution of new technologies and real practical implementation of distribution STATCOM, it is recommended that further research and engineering focus to be undertaken in the following areas:

- **Design of SSBC STATCOM Considering Wide Band Gap (WBG) Devices**

The demand for low power density and high efficiency are the desired characteristics of power converters. Besides, the harsh operating environment and the long operation hours of the converters impose more restrictions in terms of reliability and lifetime issues compared to other automotive applications. To fulfill the weight and reliability requirements, Wide Band Gap (WBG) devices (i.e. SiC and GaN) are very promising solutions. The material properties of WBG devices allow a significant reduction of the on-resistance as well as enable operation under high switching frequency with a comparable voltage and current ratings of that of Si switches. Hence, low switching and conduction losses are achieved comparatively. Also, the capability of operation under high junction temperature of WBG devices allows a significant reduction in heat sink design. These features result in lower power density of the converters which facilitate their adoption for aircraft power applications. However, for improving the efficiency the multilevel technology is commonly applied for STATCOM. The selection of the number of levels has a direct impact on the system complexity and cost as discussed in this work. Therefore, the adoption of WBG devices for SSBC STATCOM will affect the design of the active and reactive components due to the possibility of achieving high efficiency and harmonic performance with few levels. Therefore, a design study of

STATCOM with WBG devices considering the cost and performance is left for future work.

- **Control Stability and Interaction between Multiple STATCOMs**

The connection of single STATCOM for lone power system network is not the efficient solution due to the following reasons 1) reactive power compensation capability of single STATCOM is not sufficient to fulfill the requirements through long distances, and accordingly might not be able to maintain the bus voltages, 2) economically, small distributed STATCOM can be less expensive than a single-STATCOM solution and 3) more than one STATCOM can achieve better damping. Thus, by having multiple STATCOMs installed adjacently, a better voltage profile over the grid can be obtained, and the STATCOMs can share the load burden. Additionally, the flexibility of operation is available to facilitate maintenance, and, for example, one STATCOM can be disconnected from the grid for maintenance or adjustment while the others are online. However, improper design of the STATCOMs controllers could interact negatively imposing stability problems of the grid. Thus, during the development of the multiple-STATCOM facility, a huge effort is required on controllers tuning to avoid this problem. As know, mostly different vendors are handling STATCOM projects which means a kind of cooperation between vendors should be installed or otherwise enhancing the local controllers of each STATCOM should be developed. This issue is fundamental for the real implementation of STATCOMs and it is an important direction for future work.

- **STATCOM Application to Avoid New Transmission Lines Construction**

The existing transmission grid in many industrialized countries is congested after a period of low investment relative to generation and load growth. Also, emerging requirements such as mandates for renewable energy and regulation to increase the scope of power markets, are anticipated to further stress the transmission grid. The level of renewable penetration in many systems is already so high that existing renewable generators regularly experience curtailment. Growing opposition to the construction of new transmission infrastructure exists worldwide. Consequently, companies are

investigating optimal means to utilize existing transmission facilities to a higher degree of capacity. FACTS controllers (e.g. SSSC, SVC, and STATCOM) at critical points in the grid can be used to increase the dynamic stability of the system and thereby allow the transmission of additional power through the grid. However, no study quantifies the viability of this solution. Considerably, examining the effectiveness of the STATCOM solution for avoiding the construction of new lines is an interesting direction for future work.

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1. **A. M. Saif**, M. Tinari, P. Ciammaichella, C. Buccella, S. D. Gennaro and C. Cecati, "Backstepping Control for Multilevel STATCOM," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 3412-3419, doi: 10.1109/ECCE44975.2020.9235864.

2. **A. M. Saif**, C. Cecati, and C. Buccella, "Ripple Voltage Mitigation for Multilevel SSBC STATCOM" 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), Nanjing, China, 2020.

3. **A. M. Saif**, C. Cecati, E. De Paulis and C. Buccella, "On Control Design and Implementation of Multilevel SSBC STATCOM Using FPGA," IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 3559-3564, doi: 10.1109/IECON.2019.8926882.

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