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Development of circuits and systems for optical data links in biomedical applications

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Glossary

Analog-to-Digital Converter	(ADC)
Photodiode	(PD)
Bit Error Ratio	(BER)
Light Emitting Diode	(LED)
Time Division Multiplexing	(TDM)
Frequency Division Multiplexing	(FDM)
Radio Frequency	(RF)
Electromyography	(EMG)
Electrocardiogram	(ECG)
Electroretinogram	(ERG)
Electrooculography	(EOG)
Medical Implant Communications Service	(MICS)
Wireless Medical Telemetry Service	(WMTS)
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Specific Absorption Rate	(SAR)
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Transimpedance Amplifier	(TIA)
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master control unit	(CU MASTER)
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decoder control unit	(CU DECOD)
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Look-Up-Table	(LUT)
Configurable Logic Blocks	(CLB)
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ABSTRACT

In biomedical applications, optical communication links guarantee high data rates, low power consumptions and high electromagnetic compatibility. From these considerations, in this Thesis novel circuits and systems for optical data links in biotelemetry applications have been developed. More in detail, a complete biotelemetry system has been designed and implemented, both with discrete components and as full-custom integrated circuit. It includes digital architectures for the data coding/decoding, employing an UWB-based modulation technique, and analogue circuits to drive lasers and for the signal conditioning of photodiodes. The system has been firstly implemented and tested by using commercial devices so achieving data rates up to 300 Mbps with an energy efficiency of 37 pJ/bit and a maximum BER of 10^{-10}. Subsequently, the developed solution has been suitably designed, at transistor level, for its microelectronic integration in AMS 0.35 μm standard CMOS technology and, after its fabrication, has been fully characterized with data rates up to 250 Mbps so obtaining an energy efficiency of 160 pJ/bit with a maximum BER of 10^{-10}. Moreover, possible applications of the system are also reported, such as a neural recording system (work in collaboration with the Centre for Bio-Inspired Technology, Imperial College London, UK), a tactile sensory feedback system (work in collaboration with the COSMIC Lab, DITEN, University of Genova, Italy) and an event-driven serial communication on optical fiber for robotic applications (work in collaboration with iCub Facility, Istituto Italiano di Tecnologia - IIT, Genova, Italy). Furthermore, the acquired skills have been employed to design optoelectronic circuits and systems to be applied to optical transcutaneous oxygen sensing solutions that result to be particularly important for the fight against the COVID-19 pandemic. More in detail, different full-custom integrated photodiodes and analogue front-end circuits for their interfacing, as well as an optical wireless power transfer system, have been also developed (work in collaboration with the Worcester Polytechnic Institute, Worcester, USA). Finally, further related works, always concerning biomedical applications, are reported as appendices.

INTRODUCTION

The future electronic and optoelectronics systems for industrial, medical and life sciences applications will employ an increasing number of sensors to measure different physical and chemical parameters like pH values, humidity, temperature in exothermic and endothermic chemical processes, spatial parameters, object shapes and surface roughness. The data generated by the sensors must be acquired and elaborated to performing autonomous operations or parameters monitoring. For example, the improvements in biomedical engineering allow to extract and process information carried out by neural and biological signals and to control external electrics and electronics life-aid apparatus, like body-machine and/or brain-computer-interfaces, with the aim to recover a satisfactory life quality of patients with physical and/or neurological diseases [1] [2]. In these regards, prosthetic limb, for example, must be equipped with arrays of tactile sensory systems interacting with the external environment to restore as much as possible the sense of touch of a human limb. Moreover, the stimulation of neuronal cells is useful against uncontrolled epilepsy [3]. Also, for the neuronal clinical applications a large number of sensors are necessary to record these signals that can come-from or go-to the brain cortical area by means of the design and implementation of implantable bidirectional biotelemetry links that connect specific internal parts of the patient body to be monitored or activated by external equipment.

The previous two applications are examples, similar to many others, that highlight the aim of the research in neuronal medical fields that, for many aspects, are not so dissimilar from those ones related to the developments of humanoid robots. All these applications have in common the acquisition of a large amount of data from different kinds of sensors, the elaboration of these data to permit autonomous decision-making activities with the subsequent elaboration of procedures for the activation of devices and/or the generation of stimuli. Typically, these analog signals must be transmitted from the sensors to a read-out circuitry that uses them as its input data.

The circuitry, in turn, provides the signal digital conversion by using an Analog-to-Digital Converter (ADC) and then, passes the digitized data to a processing unit. In general, the processing unit runs a statistical learning algorithm on the data to extract the meaningful information about the physical variations, for example in life-aid apparatus, of the touched object and, on this basis, drives a stimulator that provides to generate a series of electro-tactile stimuli understandable by the patient [4]. In this case, a large number of tactile sensors together with other types of sensors (depending on the specific application and use)

must be employed with fast response electronic circuitries for obtaining human-like touch sensing capabilities. Similar considerations can be done for the transcutaneous implanted systems that acquires neural signals and transfers them from inside to outside (and vice versa) of the patient body suffering physical and/or neurological diseases. The neural signals are analog electrical pulses detected by micro- and nano-sensor arrays directly inserted into the patient brain [5]. An implanted electronic circuitry is used to acquire the signals from these sensors and to digitally decode them in a form to be transmitted to external controlling and/or actuation devices. In this case, whatever be the transmission methodology, the implemented transcutaneous telemetries must operate at high data rates with exceptional energy-efficiency in terms of very low overall power consumption. This is an important system issue for ensuring the health of the patient since the power spent to activate the telemetry operations for the data acquisition and transmission is dissipated as heat in the tissue and can cause severe damage if the dermal thermal limits are exceeded. For this, the consequent specific requirement in transcutaneous implanted systems is to obtain their operation in the low-voltage and low-current regime [6] [7].

From the above discussed applications, it would be clear that the type of sensors to be employed is directly related to the specific applications but the general requirements are the design and fabrication of electronic analog/digital circuitries for the acquisition, elaboration and transmission of a very large number of data with fast response times (i.e., very large frequency bandwidth) to compel the requirements of an immediate response to stimuli and the activation of body-machines, prosthetics devices and/or brain-computer-interfaces.

In this Thesis are reported in detail the implementation of optoelectronic systems together with the electronic analogue and digital circuitries designed for the coding and decoding processes of the sensor-generated voltage signals for the applications above outlined: activation, control and transmission of stimuli for tactile sensory feedback in prosthetic devices; implantable biotelemetry system for neural signal recording and biological data monitoring. For these applications the transmission of the coded data towards the decoding circuitry is achieved by means of an optical link that is composed of a large bandwidth semiconductor laser and Si Photodiode (PD). As reported in the Literature, for the coded data transmission can be used different approaches like: (*i*) simple wire connections in percutaneous systems that are, however, uncomfortable and potentially cause of infections and diseases [8] and, (i), radiofrequency techniques employing antennas as the wide band transmitters and receivers [9]. The drawbacks of these approaches for the applications which are interested in, are the resulting poor electromagnetic compatibility and signal

integrity [10] and the increase of the electrical power as the operation frequency increases that can generate dermal injuries. Moreover, these data transmission techniques cannot be or are difficult to be integrated in small dimensions even if attempts have been recently reported in miniaturizing the radiofrequency devices [11].

On the other hand, the optical data transmission links based on optoelectronic components avoids all these drawbacks because they are ideally insensitive to electromagnetic disturbances (i.e., the optical carrier frequencies are many orders of magnitude higher than those ones of the electromagnetic radiation achievable with electronic circuitries), guarantee the best achievable signal integrity with minimum Bit Error Ratio (BER), can be fabricated using the standard Si CMOS integrated technology in micrometer square resulting area so allowing operations at very low-voltage and low-power. Moreover, as happens in the optical long/medium/short haul telecommunication networks, the achievable very large frequency bandwidth of the optoelectronic devices (i.e., laser and PD) and of the optical fibers used for the optical links allows using the same transmission channel to transmit the signals generated by different kinds of sensor arrays. This is an important advantage of the optical links respect to the other possible transmission technologies and greatly simplify the hardware of the prosthetic and biomedical devices. The latter is preferred to transmit data in prosthetic devices and in robots while the free space propagation is used in implantable system so avoiding the use of wired and radiofrequencies techniques [12].

The typical optical transmission link requires to accomplish the following implementation steps: (i) the ADC conversion of the sensor signals and the data pre-processing; (ii) the coding process for the generation of a sequence of digital data by using a suitable coding scheme for the transmission of also the Clock synchronization signal [13]; (iii) the generation of a sequence of current pulses replica of the digital ones; (iv) the generation of a sequence of laser pulses replica of the current ones; (v) the conversion of the sequence of laser pulses in a sequence voltage pulses generated by the PD; (vi) the transmission Clock recovery for the final decoding process and data post-processing. In the following paragraphs all these steps will be described in detail for tactile sensory feedback systems in prosthetics devices and for implantable biotelemetry systems. Due to the present Covid-19 global pandemic, another important application of optoelectronic systems is the measuring of respiration parameters such as the partial pressure of oxygen and carbon dioxide in the blood, the respiration rate, and the peripheral blood oxygen saturation. In this sense, several optoelectronic analog front-end based on the fluorescent oxygen sensing technique have been reported [14]. Also in these cases, the systems require a light source (typically

semiconductor lasers or Light Emitting Diode (LED)'s emitting at some specific wavelength), PD and electronics circuitries necessary for the signal conditioning, such as transimpedance amplifier, driver and digital elaboration unit.

1. DATA LINK SYSTEMS – STATE OF THE ART

In this chapter, a generic data link architecture for biomedical applications, such as biotelemetry systems, is described. In particular, biotelemetry is a specific field of telemetry that permits transmission of biological information from a subject to a remote monitoring site as reported in Figure 1. The sensor signals are first converted to the electrical signals and after arranged for their transmission by employing Time Division Multiplexing (TDM) or Frequency Division Multiplexing (FDM) techniques. Then, the multiplexed signals are modulated according to the transmission line characteristics and transmitted toward the receiver system. Typically, the receiver is composed of a suitable detectors (i.e. for optical link a PD) and of amplifiers and filters able to regenerate the current or voltage signals coming from the detector. At this time, the information carried out by the signals are decoded and used as monitoring of biological parameters or as active feedback to drive control equipment. As shown in Figure 1, the biotelemetry systems can make use of Radio Frequency (RF) techniques or light free propagation for the wireless applications (e.g., for space satellite communication links) and coaxial cables or optical fibers for all those applications for which wireless transmission is not possible [15].

For example, if light is used to transmit information inside the body of a robot, in general, straight propagation is not available and the transmission can be easily obtained by employing an optical fiber. If now we restrict our attention on the implantable medical devices, they are electronic devices able to perform Electromyography (EMG), Electrocardiogram (ECG), Electroretinogram (ERG) and Electrooculography (EOG) of

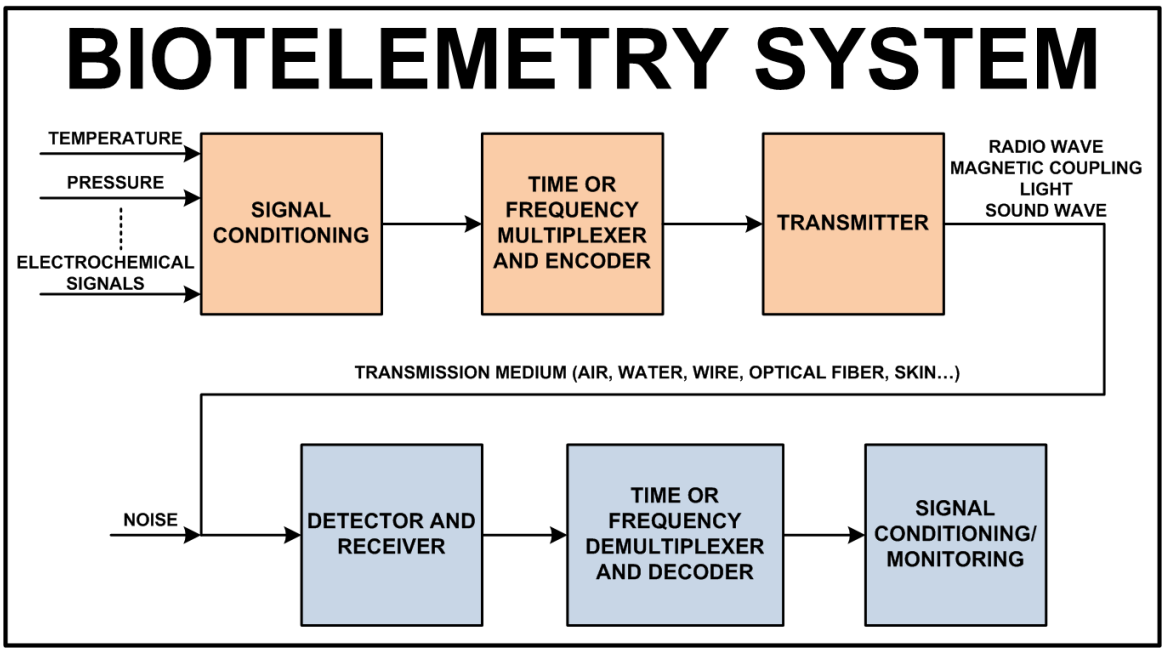


Figure 1 - The block diagram of a generic biotelemetry system.

the patient by sending current signal probes to various parts of the patient body. In general, an implantable device consists of two subsystems: an internal subsystem located underneath the patient body skin and an external one acting as the controller of the all the operations to be performed. The external subsystem is also used for powering the implantable device and for sending the achieved data to external equipment, for example, for the physician monitoring.

Especially for implanted biotelemetry systems, several characteristics must be considered [16]:

- *Low Power Consumption*: Low power consumption is the main requirement for medical implantable devices where the large dissipation in power increases the possibility to damage the soft tissues of the human body. The changing of batteries or their recharging is, generally, inconvenient, difficult, costly and even risky for the patient; all implantable medical devices need to use as less as possible electrical power.
- *High Reliability:* A failure of the implantable medical device can produce pain, damage or even the death of the patient. Since device maintenance is also costly and risky for the patient, any effort must be done to guarantee the maximum possible reliability of the implanted devices.
- *Low Voltage Signals*: Most of the natural signals generated inside the human bodies (e.g., the neural signals) as well as the corresponding output signals of the electronic transducers are in the range from few tens of μV to 1 V. This means that special care must be done in sensing and amplifying the signals assuring, at the same time, to design and implement very low noise electronic conditioning circuitries.
- *Low Frequencies:* The frequency of biological signals varies from a fraction of Hz to several kHz, Moreover, most of the implantable devices are powered by low-frequency (<1 MHz) magnetically coupled coils that are often frequency modulated to include the data telemetry. Nowadays, the design of the implantable devices must comply the standard of the Medical Implant Communications Service (MICS) with a frequency band ranging from 401 MHz to 406 MHz [17].
- *Small Size:* Implantable devices need to be as small as possible in size in order to be as small as possible invasive for the patient body. Taking into consideration the CMOS technology, this does not always mean that the silicon area should be as small as possible, because an increase the silicon area can be fruitful for including also external components and this can reduce the overall device complexity. In

addition, the use of some methods such as the auto-zeroing techniques, the FPGA paradigm and the artificial intelligence methodology can help to minimize the overall device size.

In recent years, numerous methods for the realization of low power and high data rate implantable RF biotelemetry transmitters have been presented in the Literature to perform wireless communications. The common implementation for these wireless transmitters is the use of the 433 MHz Wireless Medical Telemetry Service (WMTS) frequency band. A transmitter with the 433 MHz WMTS band presents advantages in the transmitter power consumption. in minimizing the free-space path losses and operation frequency. However, poor antenna efficiency due to reduced size of the implantable device is an unavoidable drawback. In order to reduce the size of the antenna in the transmitter, the use of the 2.4 GHz Industrial, Scientific and Medical (ISM) frequency band has been proposed but, for this frequency band, the power level of the transmitted signal is more attenuated by the human. The skin penetration depth δ of an electromagnetic field is estimated by the following relation:

$$\delta = \frac{1}{\omega}\sqrt{\frac{\mu\varepsilon'}{2}\left(\sqrt{1+\left(\frac{\sigma}{\mu\varepsilon'}\right)^2}\right)} \tag{1}$$

where ω is the frequency of the signal, ε' the real part of the tissue permittivity, μ the tissue permeability and σ the tissue conductivity. It is worth noting that, assuming for simplicity constant the material parameters, the skin penetration depth is inversely proportional to the frequency. Thus, RF devices using the 2.4 GHz ISM frequency band and those ones operating at higher frequencies are attenuated more than the devices working in the 433 MHz WMTS frequency band: this strongly limits the available penetration depth for the transmitters [18]. Another limit for a FR-based communication is the Specific Absorption Rate (SAR), defined as:

$$SAR = \frac{1}{V}\int \frac{\sigma(r)|E(r)|^2}{\rho(r)}\,dr \tag{2}$$

where σ is the sample electrical conductivity, E the RMS electric field, ρ the sample density and V the volume of the sample. The SAR is a measure of the rate at which the electromagnetic energy is absorbed per unit mass by a human body when exposed to electric fields with a frequency ranging between 100 kHz and 10 GHz. For example, in the European Union, for mobile phones and other similar hand-held devices, the SAR limit is 2 W/kg averaged over the 10 g of tissue absorbing most of the electromagnetic signal.

On the other hand, using light for the data transmission, the following advantages over the conventional RF telemetry are expected [19]:

- It is possible to achieve wide-band signal transmission relatively easily. This corresponds to the possibility of information transmission with a good frequency characteristic or a high-speed temporal response. In another view, it indicates the possibility of high-speed large-capacity transmission of information.
- It is possible to control much easier the electromagnetic interference respect to the RF telemetry. The light signal in optical telemetry does not produce interference effects with electromagnetic signals of other instruments. Moreover, also the shielding and securing safety can be done in a relatively easy way.
- The legal restrictions in using light for data communication are not as strict as for the RF-based systems.

To design an optical biotelemetry system, it is necessary to choose the wavelength of the optical source featuring as the transmitter (i.e., the laser wavelength) on the basis of the absorption spectra of the major constituents of a human skin shown in Figure 2. Any wavelength of light, or ultraviolet-visible-infrared range, can be used for optical telemetry in principle. However, with ultraviolet light, the adverse effect on our health becomes a problem in a prolonged use. As for visible light, there may be a psychological effect on the subject. Further, in this wavelength, there are many sources of optical noise such as indoor lighting. With infrared light particularly of 700–1200 nm wavelength, such problems are few. Moreover, in this wavelength, the optical absorption of body tissue is relatively low, and we can expect high optical transmission through our body. For wavelengths less than 700 nm and greater than 1200 nm the absorption of the haemoglobin and water are predominant, respectively. Furthermore, for these wavelength values used in optical fiber communication, there are a large availability of semiconductor lasers and detectors.

On the other hand, possible spatial misalignments between the optical source and the sensitive area of the photodetector represents the main disadvantage in optical wireless biotelemetry. Finally, for what concerns biotelemetry based on ultrasonic sources, these kinds of device can accomplish a good level of biocompatibility at the expenses of a low data rate and large transducer size. For these reasons, they are not suitable for implanted biotelemetry. Another important aspect in implanted biotelemetry systems is the choice of the modulation technique that impacts on the overall power consumption, bandwidth and system efficiency. Figure 3 shows the most common modulation techniques employed in biomedical devices [16].

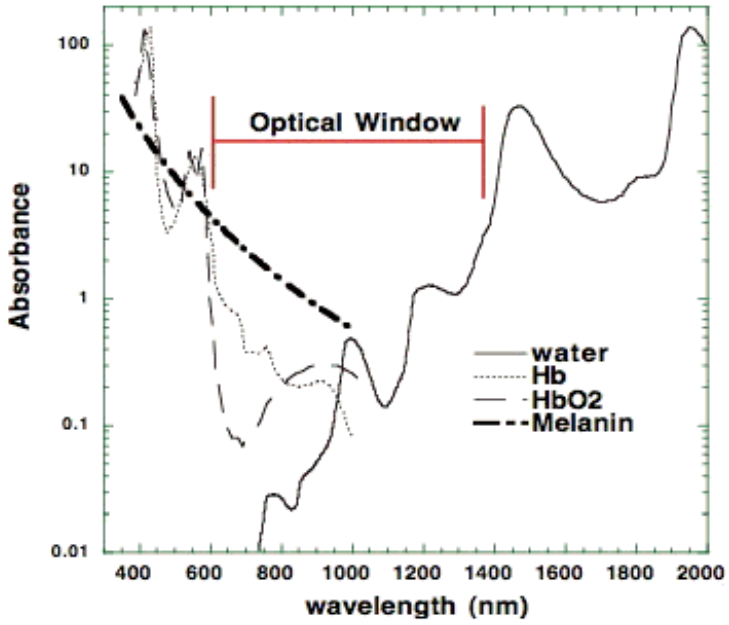


Figure 2 - Absorption spectra of human skin constituents.

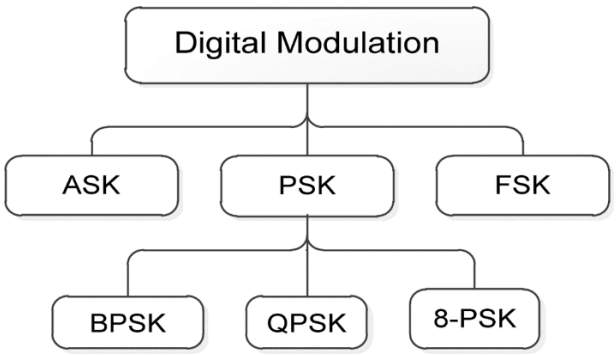


Figure 3 – Modulation techniques commonly used in biomedical devices.

Where Amplitude Shift Keying (ASK), Phase Shift Keying (PSK) and Frequency Shift Keying (FSK) are classic Amplitude, Phase and Frequency modulations, respectively. The transmission of multiple bit for each Symbol can be easily implemented in PSK modulations (i.e. Biphase Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK) or 8-PSK).

The ASK or On/Off Keying (OOK) is the simplest digital modulation used to implement wireless telemetry in bio-devices and biomedical implanted devices. In these types of modulation no carrier is used during the transmission and this help to minimize the power consumption of the modulator. The principle of ASK transmission is explained as shown in Figure 4 and Equation 3:

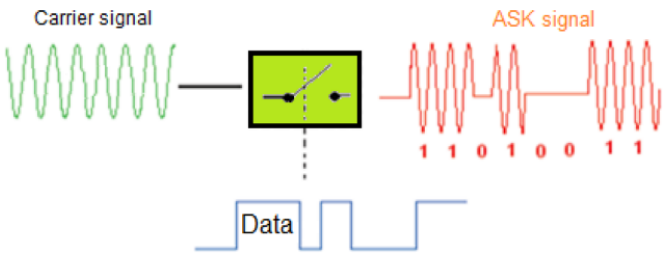


Figure 4 - Principle of ASK modulation.

where ASK is the modulated signal defined as the product of *b(t)* (the binary Data message) and *c(t)* (the carrier signal). The E_b is the bit energy and T_b the bit duration. Two are the methods used to operate the ASK demodulation: the coherent and non-coherent detection.

$$ASK\ (t) = b(t) \times c(t)$$
$$b(t) = \begin{cases} \sqrt{E_b}\ for\ Data = 1 \\ 0 \quad for\ Data = 0 \end{cases} \tag{3}$$
$$c(t) = \sqrt{\frac{2E_b}{T_b}}\cos(\omega_c t)$$

The coherent method employs the carrier phase information for the detection by means of a product detector and a phase-locked beat frequency oscillator. In the non-coherent methods, no carrier phase is used for the detection that is based on filtering the signal energy within allocated spectra and envelope detectors. From the characteristics of the two types of detection, the non-coherent method is that one more widely choose for its simplicity and low power consumption. In particular, the performance degradation of the non-coherent method is equal to about 1–3 dB if compared to that one of the coherent detection since it depends on the energy per bit to noise power spectral density ratio E_b/N_0. On the other hand, the operation principle of the FSK modulation technique is to send the binary data at two different frequencies. In the non-coherent FSK modulation, the two frequencies are associated to the transmission of the {1} and {0} as it is shown in Figure 5. The bit association can be simply represented by the following two relations:

$$S_1(t) = A\ cos(2\pi f_1 + \phi_1), \quad kT \le t \le (k+1)T \qquad bit = 1$$
$$S_2(t) = A\ cos(2\pi f_2 + \phi_2), \quad kT \le t \le (k+1)T \qquad bit = 0 \tag{4}$$

where ϕ_1 and ϕ_2 are the initial phases at t=0 of the two sinusoidal waves that, in general, do not have the same value. T is the bit period of the binary data. This type of modulation can be generated by suitably switching the modulator output line between two oscillators.

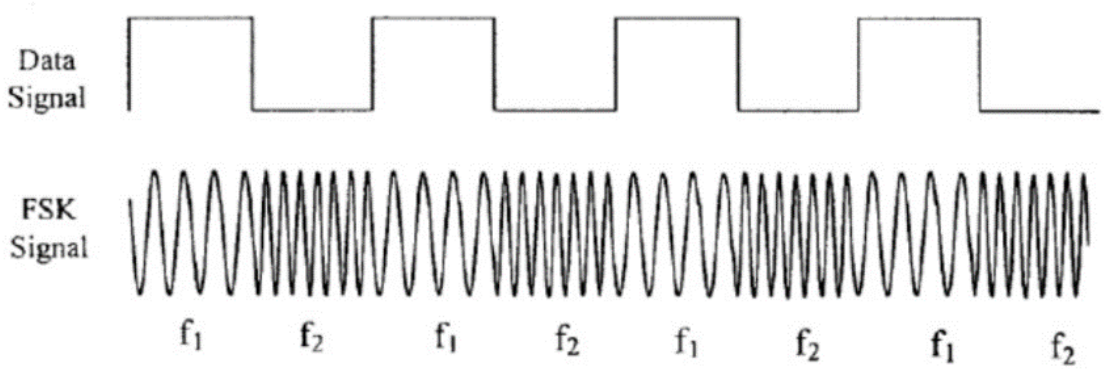


Figure 5 - Principle of FSK modulation.

In the coherent type of FSK modulation, the two signals $S_1(t)$ and $S_2(t)$ must have the same initial phase ϕ at t=0.

In the end, the simplest version of the PSK can be considered an ASK modulation where each Non-Return to Zero (NRZ) data bit of value 0 is mapped into a −1 and each NRZ 1 is mapped into a + 1. As shown in Figure 6, the resulting modulated signal can assume a value equal to the signals $S_1(t)$ or $S_2(t)$ with a phase variation of 180° coherent with the data that must be transmitted.

$$S_1(t) = A\ cos(2\pi f_c), \qquad kT \le t \le (k+1)T \qquad bit = 1$$
$$S_2(t) = -A\ cos(2\pi f_c), \qquad kT \le t \le (k+1)T \qquad bit = 0 \tag{5}$$

The data demodulation procedure for the PSK technique is more complicated than those ones for the ASK and FSK techniques, because it requires a carrier recovery system that must guarantee the best S/N versus BER values. Some examples of a complete data link system, representing the state-of-the-art for biotelemetry applications, are described in the following. In Ref. [20] it is proposed an implantable 64-channel closed-loop Near-Field Communication (NFC) system for real-time monitoring of gastric electrical activity. As shown in Figure 7, the system is composed by an implantable unit and an external unit.

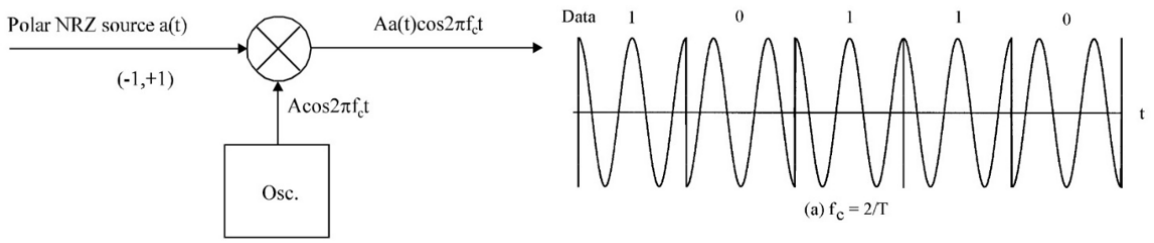


Figure 6 - Principle of PSK modulation.

The internal unit is able to acquire, encode and transmit a bitstream through two coupled coils. The same coils are used also to provide power to the implantable unit. The external unit demodulates the incoming data using an envelope detector embedded in the Radio Frequency Identification (RFID) reader (TRF7970, Texas Instruments -TI-), decodes them by the microcontroller and perform a real-time monitoring through an ISM-band RF transceiver or stores the data locally on a microSD memory card. Moreover, the external unit manages the wireless power transfer towards the implantable unit. Starting from the bitstream to be transmitted, panel (a) in Figure 8, a Manchester encoding illustrated in panel (b) generates a transition '0'-'1' if a logic state equal to zero is transmitted or a transition '1'-'0' for the logic state one. The digital sequences of '0's and '1's are encoded by differential pulse position algorithm (see panel (c) of Figure 8) at the implantable unit, and the encoded data modulated over a 13.56 MHz carrier signal, can be seen by the envelope detector at the external unit (see panel (d) of Figure 8). In vitro studies demonstrated that the system can successfully records the signals akin to gastric bioelectrical activity from 64 independent channels with a sampling rate of 16 samples per second per channel through the inductive NFC at a data rate of 125 kb/s that simultaneously recharges the implantable unit local battery. In Ref. [21] is reported an optical telemetric link capable of providing a high data rate at a low power consumption for the transcutaneous transmission of neural signals. As well as the previous case, the telemetric link is designed for operation as the interface between an implanted cortical array and an external receiver, as reported in Figure 9.

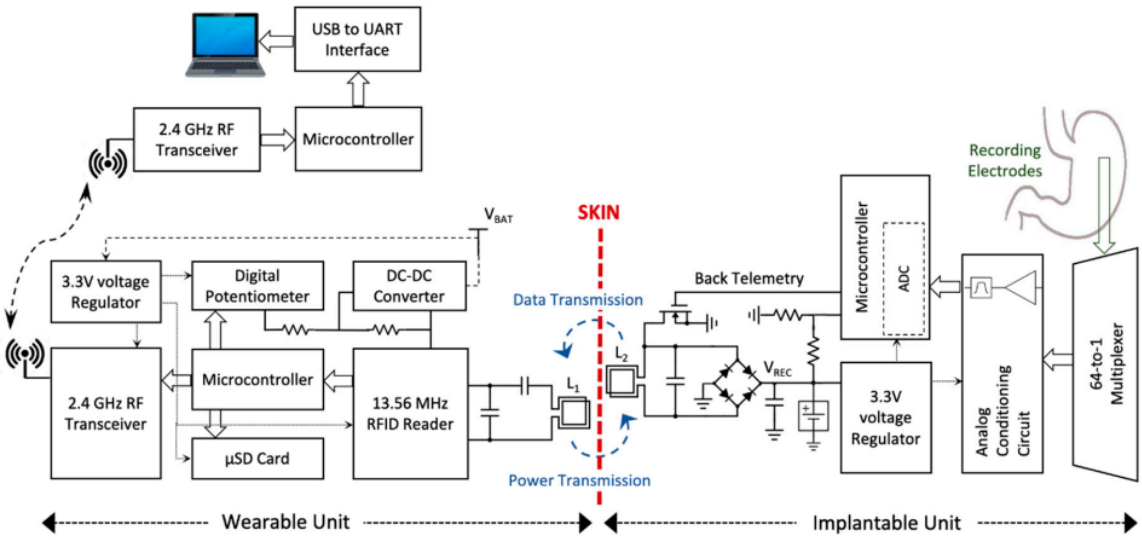


Figure 7 – The detailed block diagram of a NFC communication system.

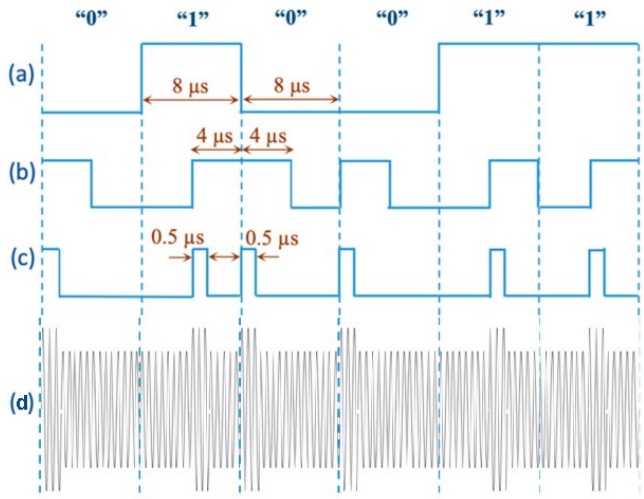


Figure 8 – Data coding algorithm of a pulsed Manchester encoding.

The basic principle of the communication system is very similar to a fiber optics communication link, but the transmission medium is fundamentally different. Human skin is a multi-layered material composed of epidermis, dermis and sub-dermis and, when a light beam passes through this layer stack, photons experience reflection, absorption and scattering. Thus, in order to collect the largest numbers of photons, the authors have used a Si photodiode with a large size of the sensitive area. The major drawback of this architecture is the reduced response time of the system because large sensitive area photodiodes have great junction capacitances limiting their operation bandwidth.

In Figure 10, the authors of Ref. 10 have realized an integrated low power current mirror circuitry for driving a Vertical Cavity Surface Emitting Laser (VCSEL) emitting at the wavelength of 850 nm (see panel A) and (see panel B) a transimpedance amplifier for the conditioning of s Si p-i-n photodiode.

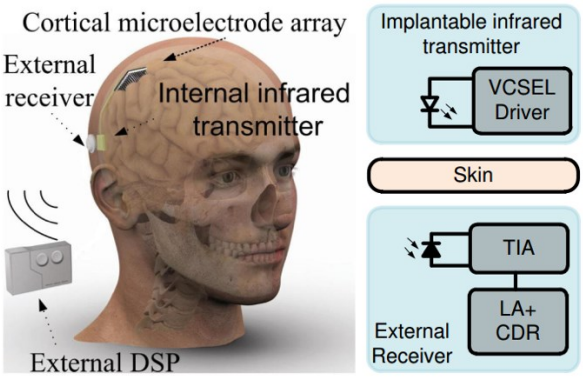


Figure 9 - Block diagram of an optical transcutaneous link.

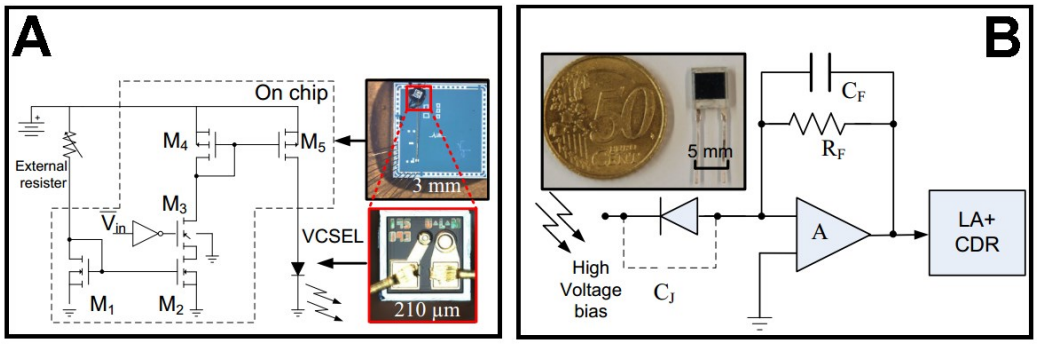


Figure 10 - Electronic interfaces of (A) the internal device and (B) the external device of an optical transcutaneous link.

The overall system is able to transmit data using a simple non-return-to-zero (NRZ) modulation though a 2.5 mm thick perfused tissue at a data rate of 100 Mbps with a BER $<2\times10^{-7}$ (evaluated by using an FPGA board) and an overall electrical power consumption of 2.1 mW.

The same authors present in [22] a bidirectional optical transcutaneous telemetric link for brain machine interface. Using the bidirectional link reported in Figure 11, it is possible to observe neural activity and apply neural stimuli accordingly. However, it is important to avoid any form of optical cross-talk between the two communication channels that share the same transmission medium, as illustrated in Figure 12. The authors use a VCSEL emitting at 680 nm for the downlink transmit data from the external base unit to the implantable one. A second VCSEL emitting at 850 nm is utilised in the uplink for data transmission from the implantable unit to the external device. In order to avoid unintentional detection of the 680 nm downlink signal, an optical bandpass filter with a transmission efficiency of 95% is used to block this unwanted signal and allow most of the 850 nm signal to pass through the skin. In this way, in the optical downlink, the data are transmitted at the data rate of 1 Mbps through a 2 mm of porcine skin with a power consumption of 290 µW in the implantable receiver.

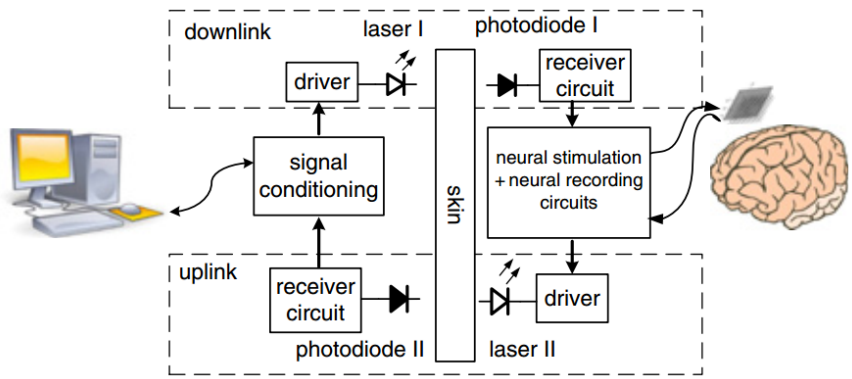


Figure 11 - Block diagram of a bidirectional optical transcutaneous link.

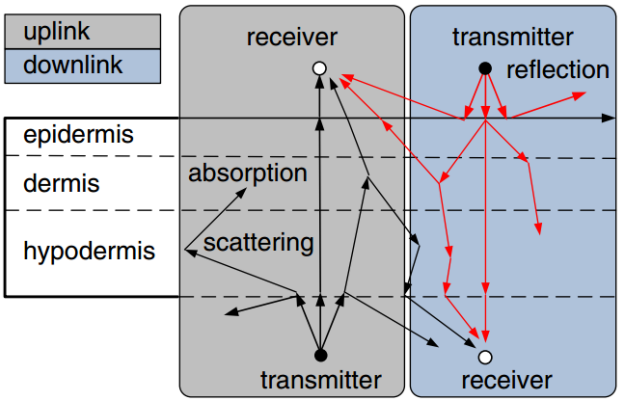


Figure 12 - Scattering, absorption and reflection of an optical signal in human skin.

This corresponds to a transmission efficiency of 290 pJ/bit. In uplink, the data rate is of 100 Mbps with an electrical power consumption of 3.2 mW in the implanted transmitter. This corresponds to a transmission efficiency of 32 pJ/bit.

In Ref. [23] the authors propose a low-power, high data rate impulse Ultra-WideBand (UWB) RF transmitter. The system is shown in Figure 13. Starting from a clock signal and the data stream to be transmitted, the system generates a train of voltage pulses where the position of the pulses determines the transmitted bit implementing a Pulse Position Modulation (PPM). The generated pulses control a Low-Dropout Regulator (LDO) that supplies the oscillator. The transmitter occupies 0.055 mm^2 in 0.13µm CMOS technology and is capable of transmitting pulses at a frequency of 135MHz. The electrical power consumption is equal to 10pJ/bit. In Table 1, the comparison of achieved performances of the state-of-the-art of wireless biotelemetry solutions that can be found in Literature is presented. The results show that the optical data link is a good choice in biotelemetry applications, even if other solutions are commonly used.

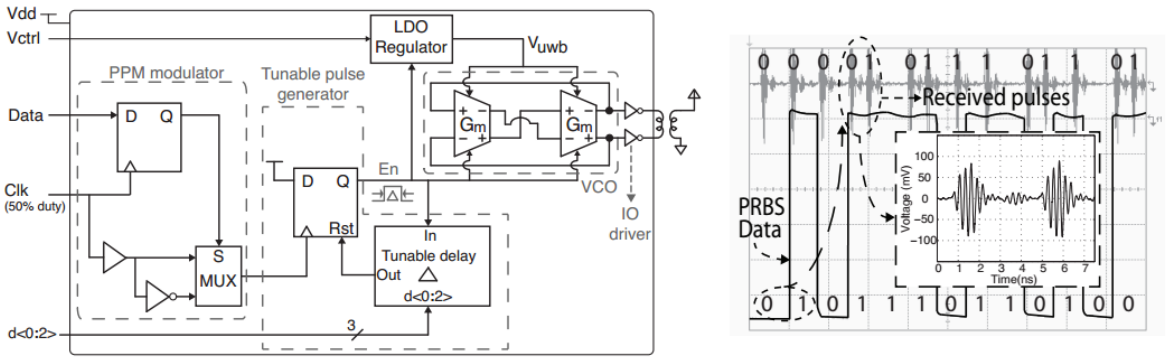


Figure 13 – Block diagram of an IR-UWB transmitter architecture (on the left) and some related experimental results (on the right).

Table 1 - Main characteristics of wireless biotelemetry systems in the literature.

Reference	Publication Year	Bitrate [Mbps]	Energy Efficiency [pJ/bit]	BER	Implementation Type	Data Link Type	Maximum Operating Distance [mm]	Coding Technique
[20]	2019	0.125	50400 (TX)	N.A.	Discrete components	Inductive	50	LSK
[21]	2014	100	21	$< 10^{-7}$	Integrated TX Discrete RX	Optical	2.5	N.R.Z.
[22]	2015	100	290	N.A.	0.35 µm CMOS	Optical	2	N.R.Z.
[23]	2013	135	10	N.A.	0.13µm CMOS	IR-UWB	120	PPM
[24]	2015	67	30	$< 10^{-7}$	Integrated TX Discrete RX	IR-UWB	500	OOK

2. OPTICAL DATA LINK – DESIGN AND IMPLEMENTATION

This chapter reports the implantable/transcutaneous biotelemetry architecture for brain machine interfaces designed and implemented by the candidate. The system uses a novel optical wireless communication system to achieve a highly energy-efficient link. The project was carried out in collaboration with the Centre for Bio-Inspired Technology of the Department of Electrical and Electronic Engineering - Imperial College London (UK).

In particular, the time diagram shown in Figure 14 illustrates the used data coding process based on a Synchronous On-Off Key (S-OOK) modulation paradigm that is able to combine both the input bitstream and the clock signals. Starting from the top of the Figure 14, the first periodic waveform is the Clock signal. For each Clock period a bit {1} or {0} of the Bit Stream can be transmitted. The Clock signal is recognized by the decoding block because for each Clock period, a laser pulse is generated independently from which bit is transmitted.

Thus, this represents the Synchronism Pulse having the same period of the Clock signal and is used for the Clock recovery operation. Referring now to the Bit Stream waveform, for this timing architecture, if a bit {1} must be transmitted, a laser pulse is generated at a time corresponding to a half-period of the Clock signal. On the other hand, if a bit {0} must be transmitted, no laser pulse occurs at a time corresponding to a half-period of the Clock signal. Thus, the resulting Transmitted Pulsed Signal is formed by an aperiodic sequence of laser pulses where only those ones transmitting the Clock signal have a defined frequency. The described transmission paradigm is a modified version of the

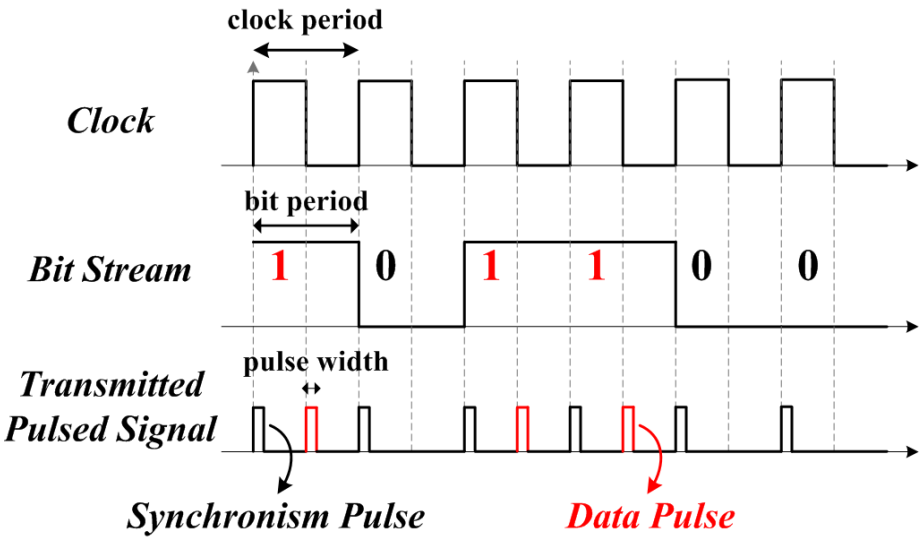


Figure 14 - Timing diagram showing the data coding process using an S-OOK modulation.

classical OOK modulation scheme and has been designed for the systems that must operate in the low-voltage and low-power regime. Respect to the OOK modulation scheme, in fact, Figure 14 shows that the laser operates only for a time corresponding to the laser pulse duration that can be shorter or much shorter than the Clock period. For example, it is now possible to employ VCSEL devices able to generate laser pulses with a duration of few tens of picoseconds. As a consequence, the described mode operation minimizes the electrical power consumption of the overall optical transmission link.
The following Paragraphs describe the design, implementation and experimental results of the developed optical data link implemented using both discrete components and Integrated Circuit (IC) solutions.

2.1. Design and implementation - discrete components solution

The overall scheme, reported in Figure 15, includes a microprobe array that acquires neural signals and convert them in digital signals (realized by the Imperial College London) and others analog/digital blocks which are described in the following Paragraphs of this Chapter. In particular, the Transmitter module is composed of three blocks and of a VCSEL. The first block (Pre-Processing) is a Data Acquisition System (DAS) that controls the acquisition and serialization of the data. The second block (Data Coding) performs the coding of the data that have been previously digitally converted and serialized. The output of this block is a sequence of voltage pulses suitably codified that must contain also a synchronization Clock signal needed to properly transmit and receive the information contained in the signal sequence generated by the sensors. The last block is the Laser Driver that receives in input the sequence of the coded pulses and transforms it in a sequence of current pulses, exactly a replica. This sequence of current pulses must have an amplitude greater than the threshold level to activate the VCSEL laser action (i.e., the amplitude of each current pulse of the sequence must exceed the value of the VCSEL threshold current). In this way, the VCSEL generates a sequence of laser pulses that is the counterpart of that one generated by the coding process. Thus, the digitally converted data containing the information on the changes of the physical/chemical parameters measured by the sensors are optically transmitted. Referring to Figure 15, also the Receiver module is composed of three blocks and of an optoelectronic device, the PD. The PD, usually a Si photodiode with frequency bandwidth equal or larger than that one of the VCSEL, generates current pulses that follow the same temporal shape of the transmitted laser pulses with amplitudes proportional to their intensities. By using an electrical scheme that

employs a Transimpedance Amplifier (TIA), the output of the Photodiode Conditioning Block is a sequence of voltage pulses from which it is possible to obtain the information transmitted by the optical communication link through a suitable decoding operation performed by the Data Decoding Block. In the end, the data are elaborated by the Post Processing Block.

The system operates an UWB communication up to a data rate of 300 Mbps with a BER less than 10^{-10}, and an energy efficiency of 37 pJ/bit, value estimated for a post integration system. The system can handle, for example, up to 16- bit 1024 channels of broadband neural data sampled at 18 kHz with only 11 mW of electrical power consumption.

The system was realized using discrete components (commercial components/custom PCB for analog blocks and a Xilinx KCU105 Field-Programmable Gate Array (FPGA) for digital blocks).

The following sub-Paragraphs describe the design of each sub-blocks presented in Figure 15, sorted according to the dataflow. Subsequently, the implementation of the system and the experimental results obtained are shown.

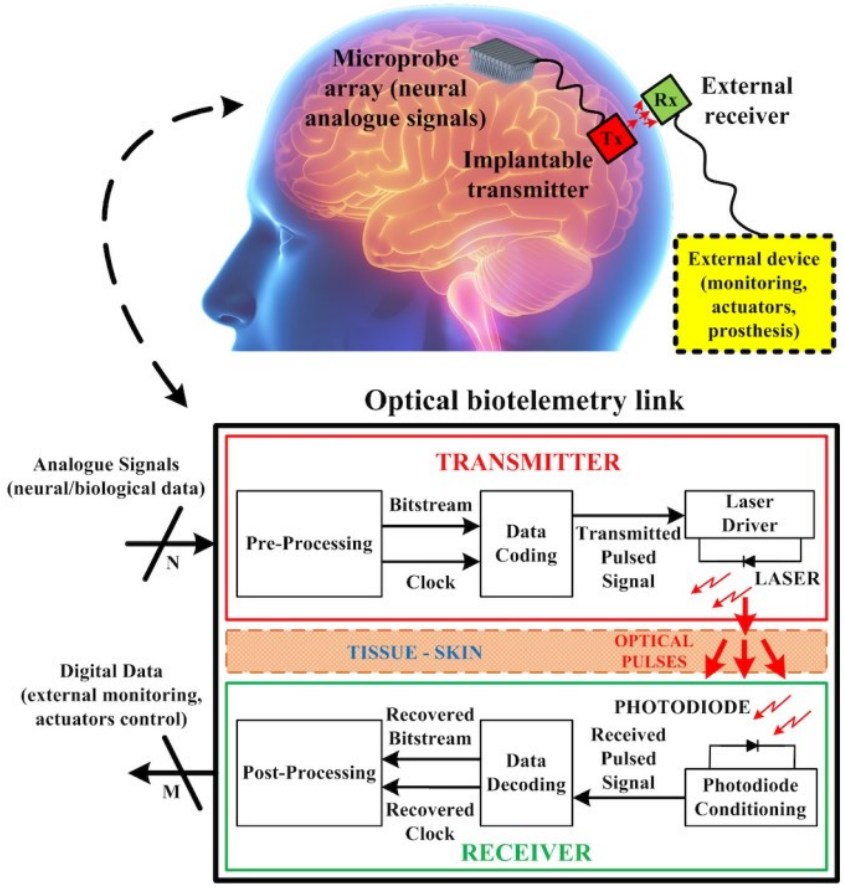


Figure 15 – Block scheme of the developed transcutaneous optical biotelemetry system.

2.1.1. FPGA implementation of a digital architecture for data pre-processing and UWB coding

The implementation of the data coding technique schematically discussed in the previous section, requires the design and the development of suitable digital architectures. The possible solutions must ensure reliable coding and decoding operations even at high data rate with an overall high-power efficiency. For these purposes, an FPGA-based architecture has been used for the preliminary implementation of the digital solutions and for the fast prototyping of the system using commercial discrete components. In particular, the following described architectures have been implemented on a Xilinx FPGA Kintex Ultrascale board even if the implemented digital solutions have been designed to be implemented also on other families of FPGA boards.

The function of the pre-processing circuit, reported in Figure 16, is to generate a single bitstream from multichannel sampled data by interleaving the different channels/samples using the TDM paradigm. This has been designed to process up to 1024 channels of data sampled at 18 kHz with a 16- bit resolution. The pre-processing circuit operates as follows: for each sample, the DAS control unit (CU DAS) sequences through all the data channels storing each 16-bit sample in the word register, First In First Out (FIFO) type Parallel In Parallel Out (PIPO) buffer). The word length is thus 2× 8-bit. The initial portion of this register is pre-loaded with a pre-set starting sequence that forms the Header of the data packet. Each packet contains a single sample across all the 1024 channels (i.e., 2048 bytes) added to the starting sequence. In order to ensure that the output is a continuous bitstream (i.e., a continuous serialization of the composed data packages), the master control unit

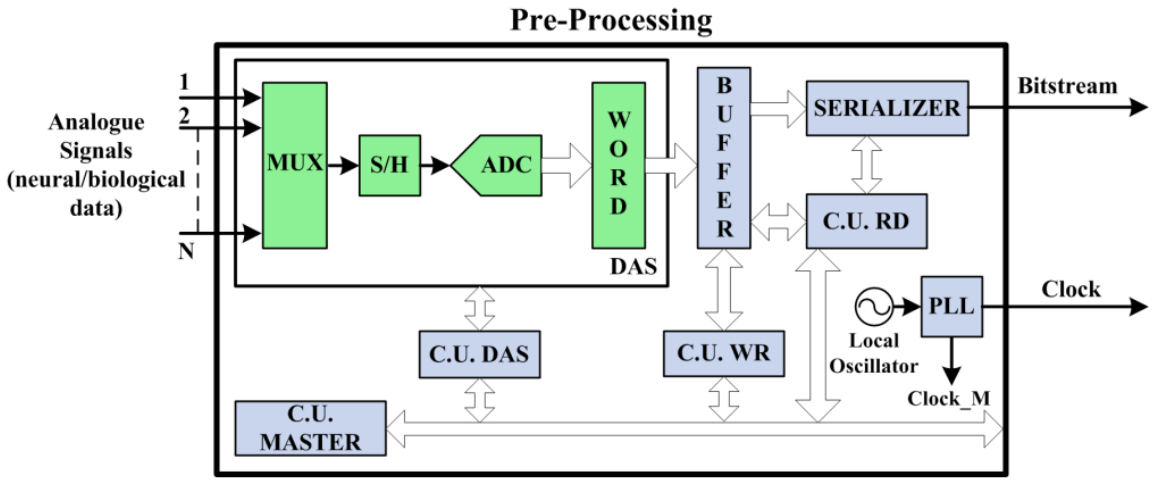


Figure 16 - Pre-processing circuit, implemented on FPGA, showing the organisation of the different control units (CUs) for the data acquisition system.

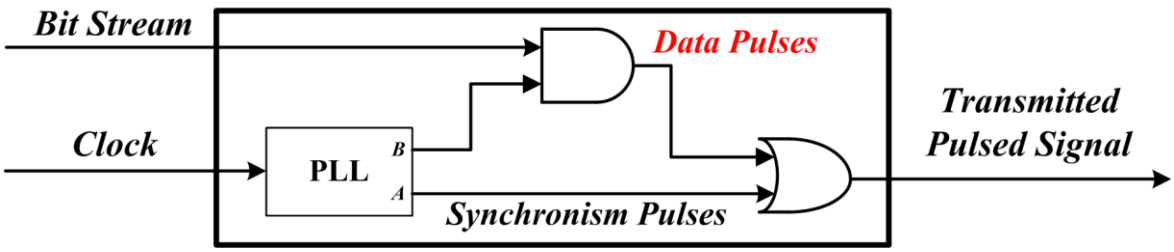


Figure 17 - Digital logic scheme of the Data Coding block.

(CU MASTER) coordinates the timing of all the operations/functions (i.e., the data acquisition, data read and data write) of the overall pre-processing block. Additionally, a local oscillator provided on the FPGA board allows the implementation of a Phase-Locked Loop (PLL) block to provide an internal reference clock (i.e., Clock M @ 300 MHz) for the system synchronization.

According to Figure 17, the data coding can be implemented by using a PLL and two logic gates. The PLL, already realized as a basic block inside the FPGA, generates two pulsed signals starting from the input Clock signal (i.e., the Synchronism Pulse). The first pulse at the PLL terminal A is generated in correspondence of the rising edges of the Clock signal, and the second pulse at the PLL terminal B is generated synchronized with the falling edges of the Clock signal. These two pulsed signals have the same frequency with a relative phase difference of 180° and a selectable duty-cycle in order to guarantee the desired pulse width. The signal at the PLL terminal B is combined with the Bit Stream (see Figure 14) through an AND digital logic gate so that the Data Pulses are generated only when the Bit Stream assumes the 'high' logic state (i.e., corresponding to the logic value {1}). Finally, the output of the AND gate is combined with the Synchronism Pulses by means of an OR digital logic gate. Consequently, the resulting combination of these two pulsed signals provides a train of voltage pulses corresponding to the Transmitted Pulsed Signal that is employed as the input control signal of the Laser Driver block.

2.1.2. Analogue conditioning circuits for lasers and photodiodes

In this Paragraph we will describe some possible solutions for the implementation of the analogue electronic circuitries able to drive the VCSEL laser used as the transmitter the implemented UWB optical wireless communication. Preliminary implementations and fast prototyping of the designed circuits have been obtained by using commercial discrete components. In particular, referring to the Transmitter module of the system, the VCSEL can be controlled through a driving circuit based on current mirrors, as shown in Figure 18. This circuit topology operates a conversion of the voltage pulses corresponding to the

coded data stream to be transmitted (i.e., the sequence of the Transmitted Pulsed Signal) in Current Pulses to drive the VCSEL laser. The circuit presents also the capability to regulate both the pulsed current amplitude and a DC current level through two resistive trimmers R_{trim1} and R_{trim2}, respectively. The laser action takes place if the sum of the pulsed and DC currents is greater than the VCSEL laser threshold current. In these conditions, the resulting laser pulse peak intensity is proportional to the value of the corresponding amplitude of the driving current pulse. R_{bias} and R_{load} are equal to 100 Ω, Rtrim1 and Rtrim2 are 1 kΩ trimmers, the circuit operates from a single VCC=5 V supply voltage using a BFG520 NPN 9 GHz wideband bipolar RF transistor.

The Figure 19 shows the time response of the circuit with input pulses having an amplitude equal to 3.3V.

A different approach is implemented in Figure 20 where a single transistor stage is used to convert the input voltage pulses into current pulses for driving the VCSEL laser. In this case the values of the passive components are: C1=100 nF, C2=1.8 pF, R1=82 Ω, R2=50 Ω, R_{TRIM1}=5 kΩ.

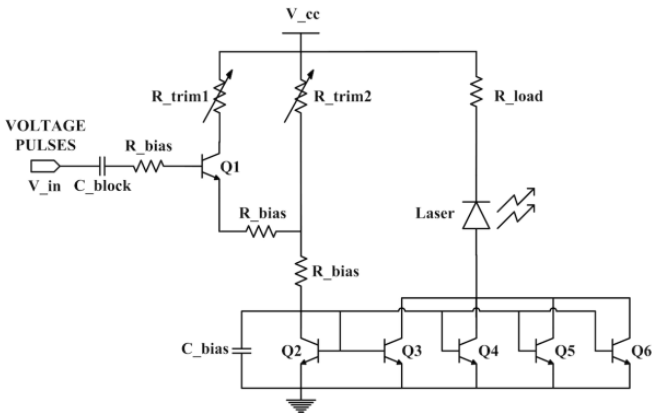


Figure 18 - Schematic circuit for the laser biasing and driving.

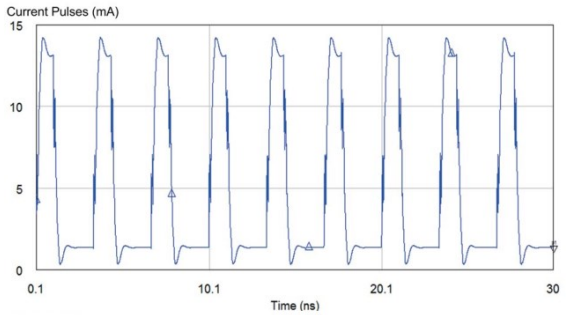


Figure 19 - Simulation of the sequence of driver generated output current pulses.

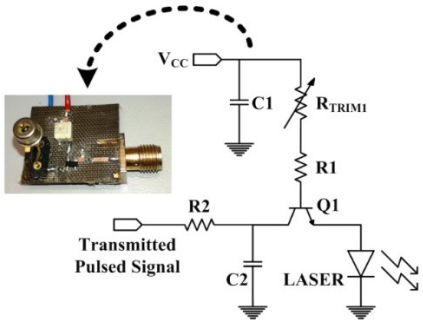


Figure 20 – Schematic circuit of the laser driver and its PCB implementation.

Also in this case, the circuit operates from a single V_{CC}=5 V supply voltage using a BFG520 NPN 9 GHz wideband bipolar RF transistor. The design, optimization and simulation of both the circuits have been performed through AWR Microwave Office tools. The circuits have been implemented using a Printed Circuit Board (PCB) prototype. The PCB uses a TLX8 (high volume fiberglass reinforced microwave) substrate with a Dielectric constant (ε_r) of 2.50 to minimise parasitic and discrete Commercial Off-The-Shelf (COTS) components (i.e., transistors for high-frequency/RF applications).

The PD conditioning circuit inserted within the receiver sub-system (refer to Figure 15) is based on a multi-stage TIA shown in Figure 21(a). This circuit uses a cascade of four (wideband ERA-1SM+InGaP HBT monolithic) Darlington pair stages to convert the received sequence of photocurrent pulses generated by the PD into a corresponding sequence of voltage pulses. A suitable gain is essential to ensure that the generated voltage pulses have an amplitude higher than the digital logic threshold needed for a correct detection of a "high" logic level operated by the subsequent Data Decoding block. The main characteristics of the circuit are the following: $V_{BIAS} = V_{CC} = 5$ V, L1 = L2 = L3 = L4 = 33 nH, C1 = C3 = C5 = C7 = C9 = 100 nF + 100 pF, C2 = C4 = C6 = C8 = C10 = 470 pF, R1 = 1 kΩ, R2 = 50 Ω, R3 = R4 = R5 = R6 = 180 Ω.

ERA-1SM+ (RoHS compliant) is a wideband amplifier that allows for high dynamic range operation, unconditionally stable and internally matched to 50 Ohms. These characteristics guarantee an amplification S_{21} parameter over 40 db, almost flat in a range from DC to 4 GHz. Moreover, the system has a K factor always greater than 1, this value ensures the stability of the amplifier, as reported in Figure 22. The panel (C) of Figure 21 shows the PCB layout performed through the AWR Microwave Office tools, while the image in panel (b) shows the physical realization of the transimpedance amplifier that includes an FDS-025 PD.

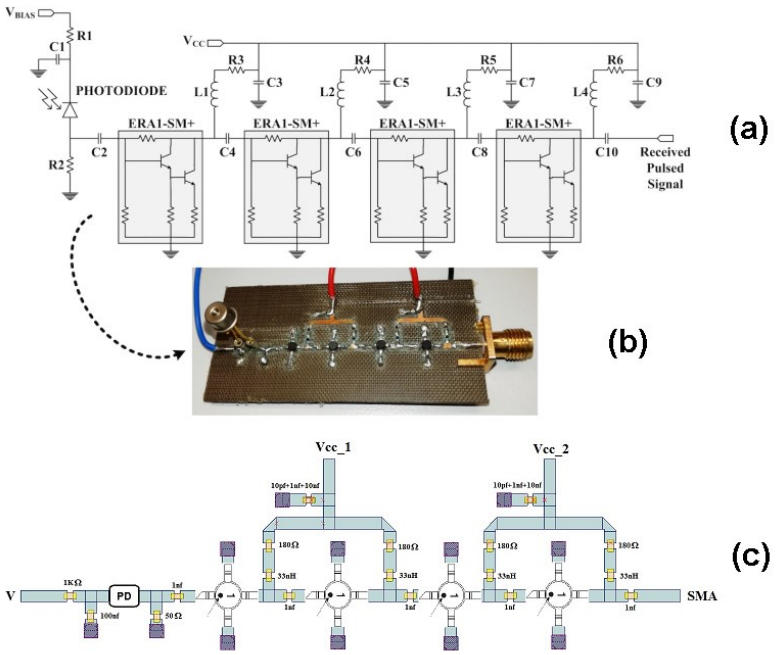


Figure 21- Schematic of the photodiode conditioning circuit (a), its PCB implementation (b) and PCB layout (c).

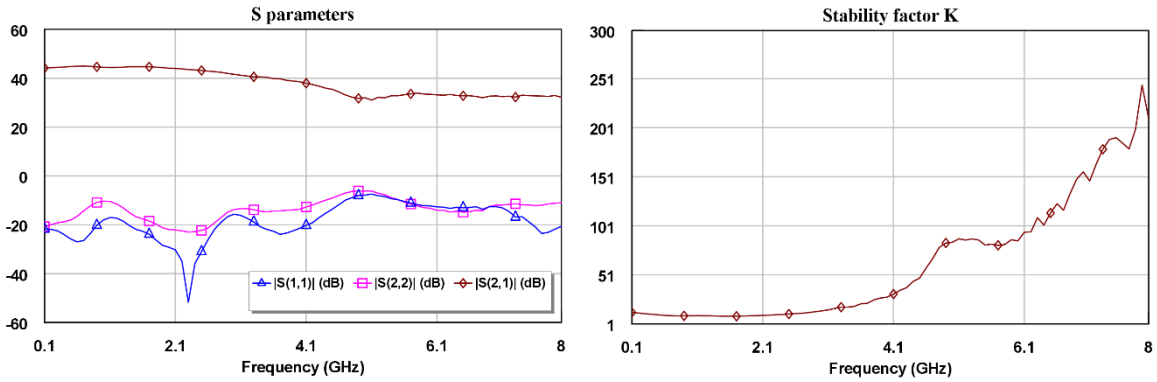


Figure 22 - S parameters and stability factor K of the transimpedance amplifier.

2.1.3. FPGA implementation of a digital architecture for UWB data decoding and post-processing.

The implemented data decoding circuit is shown in Figure 23. The circuit receives the sequence of the signal photo-generated by the PD (i.e., the PD generated photocurrent pulses with amplitude proportional to the intensity of the sequence of the VCSEL pulses obtained as the output of the conditioning circuit) and recovers the clock and serial data stream. This operation is implemented as follows:

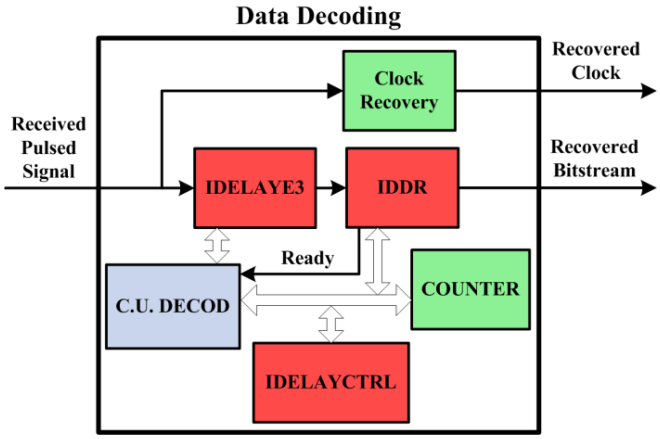


Figure 23 - Data decoding circuit, implemented on FPGA, that recovers also the clock signal.

both the clock recovery and the IDELAYE3 blocks share the input signal. In particular, IDELAYE3 is a programmable delay line that adds a finite and discrete delay (up to 512 delay taps, each ranging from 2.5 ps to 15 ps) to the input pulsed signal. The IDDR block then takes in the delayed signal (through IDELAYE3) together with the recovered clock, and generates two output signals, capturing the input signal on the rising and falling edges of the recovered clock. The first output signal (i.e., the ready signal) is high if correctly captures the synchronization pulse (on the rising edge). The second output signal (the recovered bitstream) captures the serial data (on the falling edge) providing that the synchronisation pulse is correctly aligned. The decoder control unit (CU DECOD) ensures the correct alignment by varying the programmable delay until the ready signal remains in the 'high' logic state for at least 50 clock periods (≈166.5 ns). Furthermore, the IDELAYCTRL block has been included to provide further compensation (to the programmable delay) to supply voltage and/or system temperature variations.

The clock recovery circuit (within the data decoding circuit described above) is shown in Figure 24. This circuit consists of a D-type Flip-Flop (D-FF), a PLL and a latch. The circuit operates as follows: the input signal feeds the D-FF clock (with D input set to high) in a such a way that the Q output is asserted high whenever a pulse is detected. The latch then provides a finite 'delay' before resetting the D-FF. Specifically, the output Q remains in the high logic state for a time interval T_{FF} given by:

$$T_{FF}(Q = 1) = T_{LOOP} + T_{LATCH} + T_{RST} \quad (6)$$

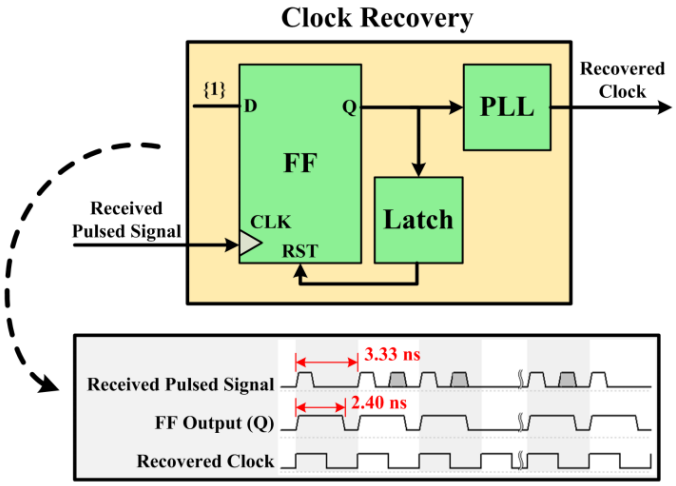


Figure 24 - Clock recovery circuit, implemented on FPGA, that recovers a symmetrical clock from the received pulse stream.

where T_{LOOP} is the physical time delay introduced by the feedback loop that connects the D-FF output Q to the latch and the latch to the RST input of the D-FF, T_{LATCH} is the response time of the latch and T_{RST} is the time necessary to the D-FF to make effective the reset operation. This overall 'delay' is intentionally selected to be equal to about 75% of the clock period (τ=3.3 ns). In this way, if a data '1' is received, the synchronisation and the data pulses are effectively merged into a single longer pulse. For this, a 2.4 ns time interval is achieved using a manual place & route operation for the implementation of the clock recovery circuit. This time interval ensures that for each clock period only one pulse will be generated, irrespective of the data that has been encoded. Then, the subsequent PLL completes the clock recovery by adjusting it in order to have a 50% duty cycle while also reducing the jitter. The employed PLL (integrated in the FPGA board) is capable of managing and locking the input signals at an operating frequency ranging from 70 MHz to 933 MHz providing a 50% duty-cycle output signals with the best precision of 200 ps (i.e., the maximum error that can affect the output duty-cycle). However, since transmission errors can occur (e.g., introduced by the communication channel), it is important to evaluate the impact they might have to the clock recovery.

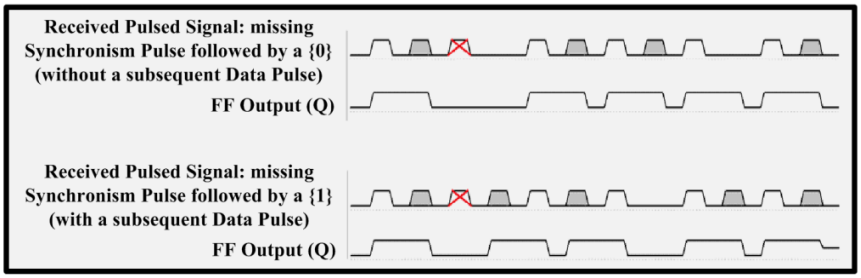


Figure 25 - Example showing the impact of transmission errors in the clock recovery circuit.

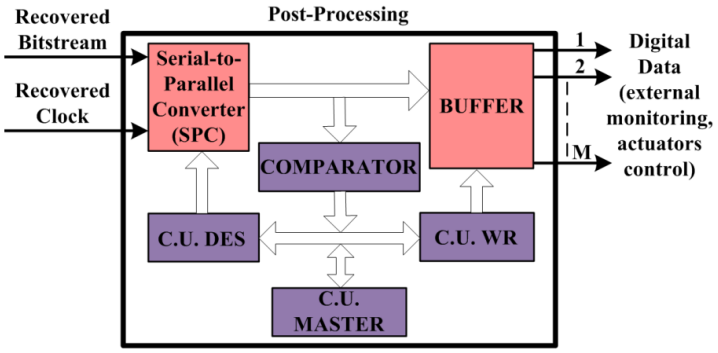


Figure 26 - Post-processing circuit, implemented on FPGA, that recovers the individual channel data.

Figure 25 shows an example showing the transient response of the clock recovery circuit in the presence of different transmission errors (e.g., missing synchronisation pulses). This can result in one of the following two events if: (*i*) the next pulse is another synchronization pulse (i.e., without a subsequent data pulse) there will be no low-to-high transition at the D-FF output (input to PLL, see top of Figure 25); (*ii*) there is a subsequent data pulse, the D-FF output (input to PLL) will have a phase shift of 180° until a further data '0' (i.e., missing data pulse) occurs (see bottom of Figure 25). A series of tests conducted on the FPGA board have demonstrated that, in both the cases, the PLL output maintains the recovered clock locked at 300 MHz. This remains the case also in the presence of multiple repeated errors that occur at the PLL input, thus guaranteeing good robustness for the overall communication system. The post-processing circuit is shown in Figure 26.

The synchronous serial data that has been recovered is firstly stored in a SIPO register (Serial-to-Parallel Converter (SPC)). The master control unit (CU MASTER) continuously verifies and checks the received data packets using the comparator block. When the Header that defines the beginning of the transmitted data packet, is correctly identified, the CU MASTER activates the control units (CU WR and CU DES). These units allow for the serial data packets to be split into individual data channel and saved in the register buffer that provides the output. This operation is continuously performed and repeated for each data packet that is received and identified by the Header.

2.1.4. Experimental setup and measurements

This sub-Paragraph describes the experimental setup and reports on the results of the characterization of the overall communication system analyzed in Paragraph 2.1.

The architecture of the system implemented by using commercial components is shown in Figure 27. Several measurements have been performed to fully characterize the system

operating at 300 Mbps, corresponding to a bit period of 3.3 ns. In particular, to evaluate the electrical power consumption and the BER, the data digitalization operations performed by the pre-processing circuit have been emulated using a True Random Number Generator (TRNG). The TRNG employed, described in the appendix A, generates a bit sequence (i.e. the random bitstream) of length 2^{34}-1 and is implemented using the FPGA board. More in detail, the test unit generates a random bitstream that is coded and transmitted following the dataflow previously described in Figure 14. Once the bitstream is transmitted and decoded, the obtained data are compared bit to bit with the transmitted random bitstream generated by the TRNG, in order to evaluate the BER. Moreover, a mechanical XYZ translation stage has been employed to optically align the VCSEL emitted beam respect to the sensitive area of the photodiode considering a FDS-025 PD by Thorlabs (high-speed Si-based PD with 47ps response time and 250µm active area diameter) in the plane (X;Y) perpendicular to the laser beam propagation direction Z. All measurements have been taken using a digital storage oscilloscope (6GHz, 20GS/s LeCroy WaveMaster 8600A digital oscilloscope).

A simplified schematic describing the relative positions of the VCSEL and the photodiode used for the optical characterization of the communication link is reported in Figure 28, The tissue sample used here in between the VCSEL and the Photodiode was a section of cleaned porcine skin, gently tensioned by employing a custom made holder, to mimic a human skin layer [25]. The porcine skin consisted of the epidermal, dermal and adipose layers with an average thickness of approximately 3.5 mm.

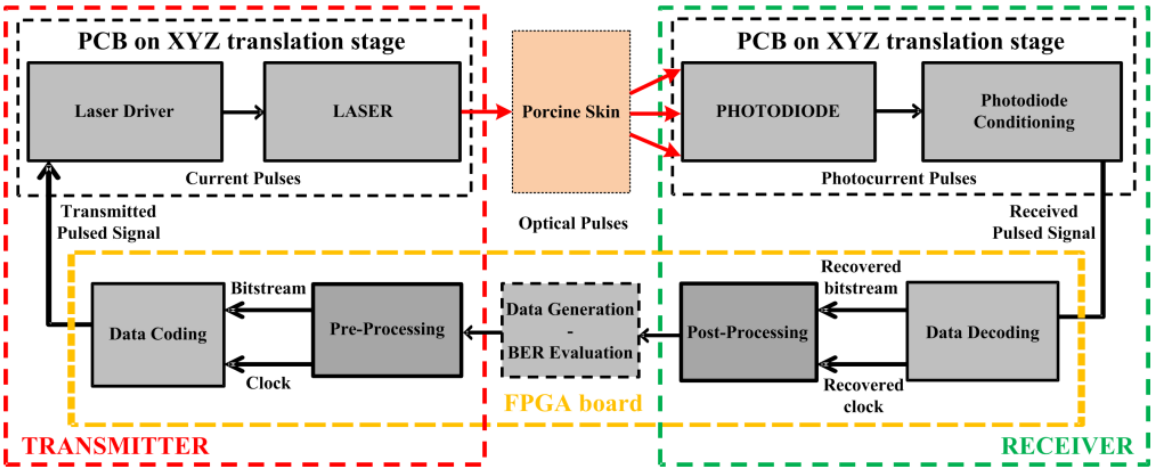


Figure 27 - Top-level system architecture of the implemented optical biotelemetry (Unit Under Test) completed by the test system.

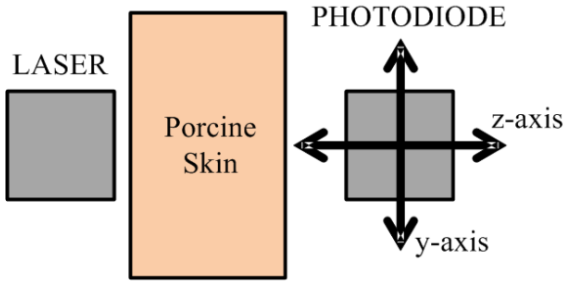


Figure 28 - Schematic of the experimental setup for characterizing the optical biotelemetry showing the relative position of the transmitter (the VCSEL Laser), of the tissue (the porcine skin), and the receiver (the photodiode) mounted on an XYZ translation stage for precise adjustment.

The photodiode conditioning PCB was attached with the photodiode to the XYZ-translation stage that uses micrometer heads allowing for a precise adjustment with a 20 µm resolution that corresponds approximately to 1/10th of the photodiode sensitive area. For the optical characterization of the optical link system, we have performed a series of measurements to evaluate the degree of the maximum misalignment between the VCSEL and the photodiode that allows the optical link still operates with satisfactory BER values. This characterization is important in real implantable systems because the natural movement of the human body and/or variations of the external condition can produce unwanted and unpredictable misalignments between the implanted and the external part of the optical link. We proceeded by first positioning the porcine tissue in close contact with the VCSEL. The VCSEL is then driven by the sequence of current pulses generated by the laser driver that allow the lasing of the VCSEL. For any distance Z of the photodiode from the porcine skin, the measurement always started positioning the photodiode to achieve the maximum of the photocurrent. This correspond to adjust the photodiode position by using the micrometer heads located along the (X;Y). The overall link performance is then assessed by its ability to correctly detect the VCSEL laser pulses for each value of the distance Z of the PD from the porcine skin by moving it in the (X;Y) plane. Specifically, any voltage pulse detected at the output of the PD conditioning circuit above the value of 1 V can be robustly sampled by the FPGA board (i.e., they have an amplitude equal or greater that the digital threshold for a correct acquisition by the FPGA board). On the contrary, voltage pulses received with an amplitude below 1 V can result in the generation of errors n the transmission data.

The realized experimental setup is shown in Figure 29. The VCSEL and the photodiode are mounted on their respective PCBs and, as stated above, they are initially positioned to be perfectly aligned and in close contact with the tissue. The relative positions are then varied accordingly to characterize the optical link.

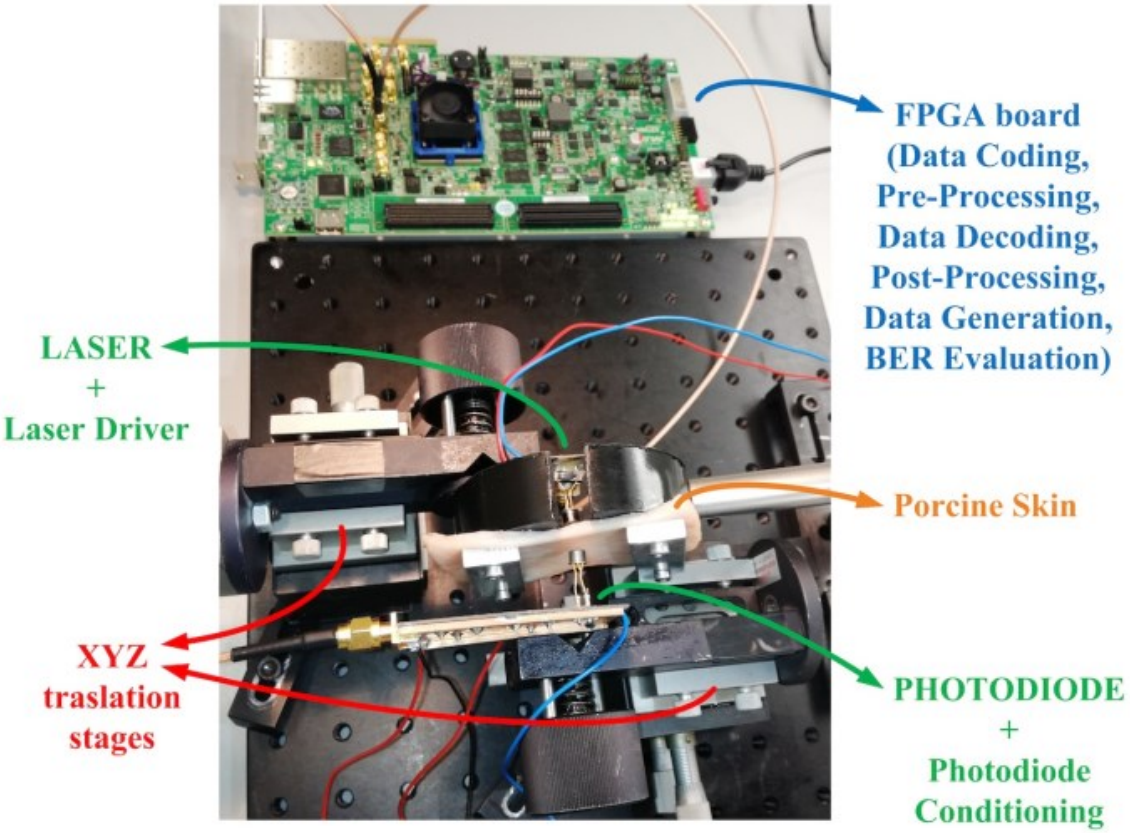


Figure 29 - Experimental setup for characterizing the developed optical biotelemetry system.

Using the system implemented with commercial components, captured waveform (using oscilloscope) of the system operating at 300 Mbps is shown in Figure 30. The reported waveforms have been obtained for a perfect alignment between the VCSEL and the photodiode sensitive area and demonstrate the correct operation of the optical link by observing the matching between the received decoded bitstream and the transmitted data. The measured waveforms demonstrate the presence of a time latency between the transmitted and the recovered bitstreams equal to about 12 ns. This is mainly due to the execution time for the clock recovery and the data decoding processes. To assess the quality of the transmitted signal (i.e., the coded pulses), multiple acquisitions of the resulting waveforms have been as shown in Figure 31 (a). The measured amplitude variation and time jitter are lower than 150 mV and 150 ps, respectively. To assess the quality of the received signal (i.e., the recovered bitstream), an eye diagram has been produced as reported in Figure 31 (b). The measured amplitude variation and time jitter are lower than 150 mV and 200 ps, respectively.

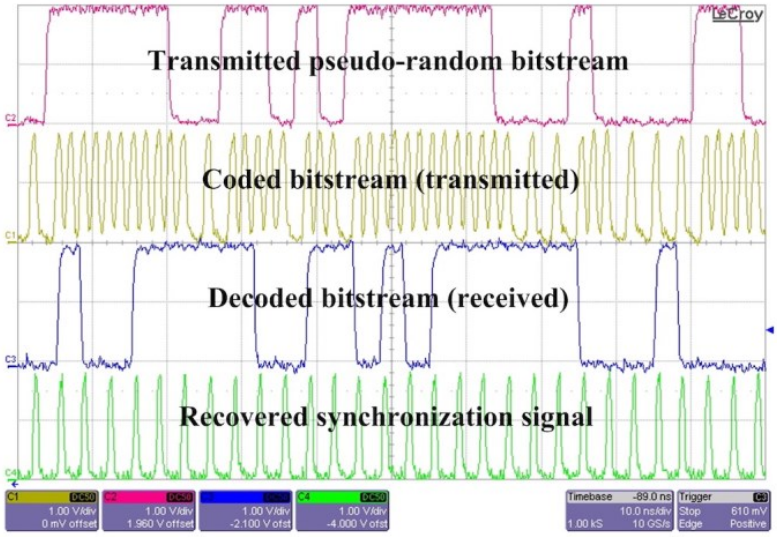


Figure 30 - Experimental measurement: main signals during the transmission of a true random bitstream at 300 Mbps. The waveforms reported from top to bottom refer to: (in purple) the input bitstream of true random data; (in yellow) the transmitted coded pulses; (in blue) the decoded data; (in green) the recovered clock signal.

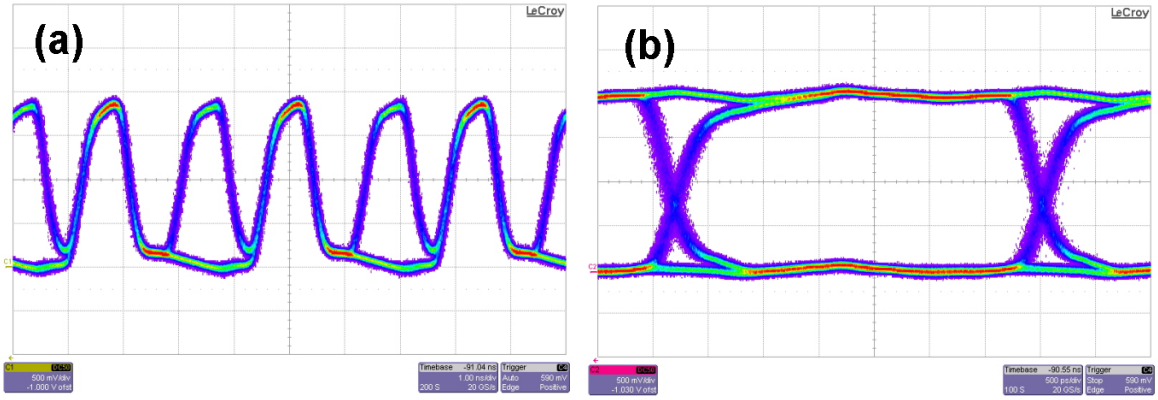


Figure 31 - Multiple acquisitions of the transmitted (a) and eye-diagram (b) of the received signal (i.e., the recovered bitstream).

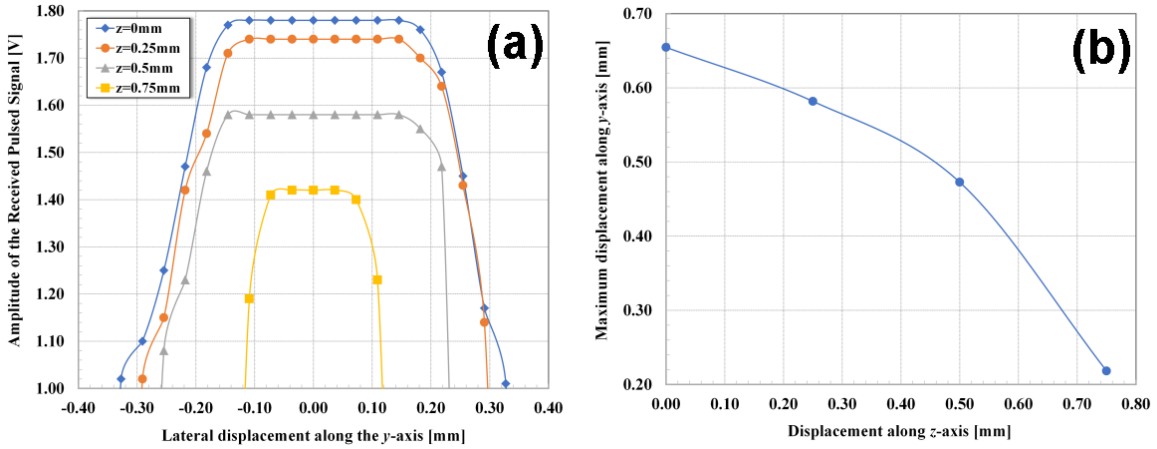


Figure 32 - Optical link sensitivity to lateral misalignment between the VCSEL and the photodiode (a); receiver spatial operability range in terms of the maximum possible lateral displacement between the VCSEL and the photodiode (b).

At this point, a series of measurements were performed to assess the sensitivity to lateral misalignments (i.e., in the (X;Y) plane perpendicular to the VCSEL beam propagation

direction) as a function of the distance variation Z between the VCSEL and the photodiode. Lateral misalignment was achieved by adjusting the position of the photodiode in the Y-axis and/or the X-axis off from the perfect alignment. During these measurements, the VCSEL position remained fixed and the maximum average pulsed optical power was maintained below 2 mW with a laser pulse width of about 900 ps and at a pulse repetition rate of 300 MHz. The results are reported in Figure 32 (a). The measurements were repeated for misalignment in the X-axis that gave very similar results to those ones obtained for the Y-axis misalignment. For the measurements taken for Z=0, the photodiode is positioned in contact with the porcine skin without pressing it. This is the condition of the minimum distance between the VCSEL and the photodiode that result to be 3.5 mm, corresponding to the approximate thickness of the porcine skin sample. The results show (as expected) that as the lateral misalignment (or proximity between emitter and detector) increases, the recovered voltage pulse amplitude decreases. The spatial range of operability defined as the the condition for the detection of voltage pulses with amplitudes equal or greater than the digital threshold for a correct decoding of the transmitted data, thus, depends on both the lateral misalignment and change as a function of the distance Z between the VCSEL and the photodiode. The behavior of the spatial operability as a function of the distance Z is reported in panel (B) of Figure 45. From this Figure we observe that the maximum lateral misalignments decrease as the displacement between the VCSEL and the photodiode increases, determining a maximum possible displacement equal to 0.75 mm.

It is important to note that although the employed system uses encoded laser pulses, this is different to the case of employing RF waveform in a UWB modulation scheme. We demonstrated that the use of short laser pulses for the described optical link comply with standard UWB specifications since the laser pulses have a duration much less than 1 ns and a transition time of less than half the pulse. Therefore, any energy emitted within the electromagnetic spectrum corresponding to the laser pulse bandwidth needs to comply with the relevant regulations. The power spectrum of the transmitted signal is reported in Figure 33, demonstrating that the emitted energy fulfills the Federal Communications Commission (FCC) standard mask on the power spectrum of modulated/pulsed signals (i.e., the signal power emission limits for communication systems) [26].

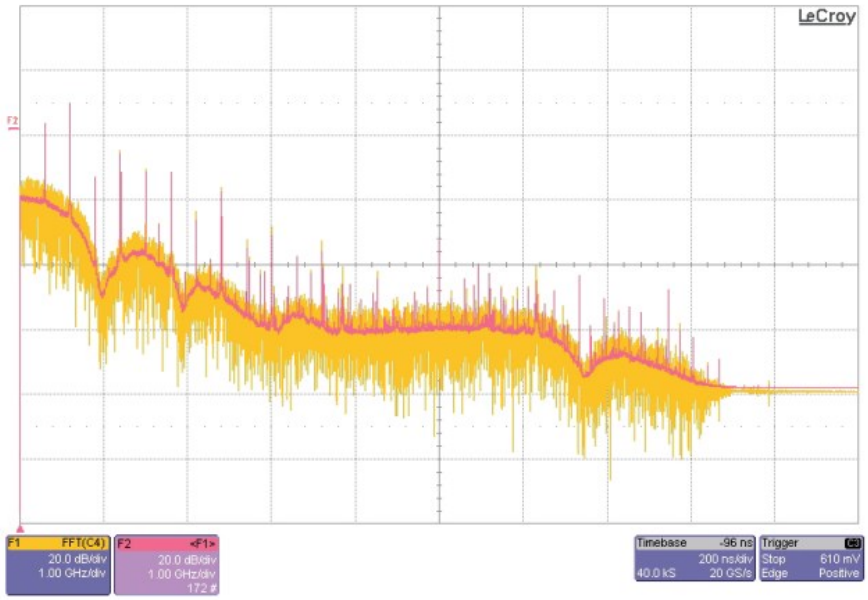


Figure 33 - Power spectrum of the transmitted pulse signal.

2.2. Design and implementation – CMOS integrated solution

In this Paragraph, the design, fabrication, implementation and experimental characterization of an integrated bidirectional communication System-on-Chip (SoC) for transcutaneous bidirectional optical biotelemetry links are reported. The developed architecture implements the same UWB-inspired pulsed coding technique described in Figure 14 and contains a transmitter and a receiver to achieve a simultaneous bidirectional link, following the scheme reported in Figure 34. The dataflow and the purpose of each block implemented is the same described previously in Figure 15, except for the pre-processing/post-processing blocks that are not present in this first version of the chip.

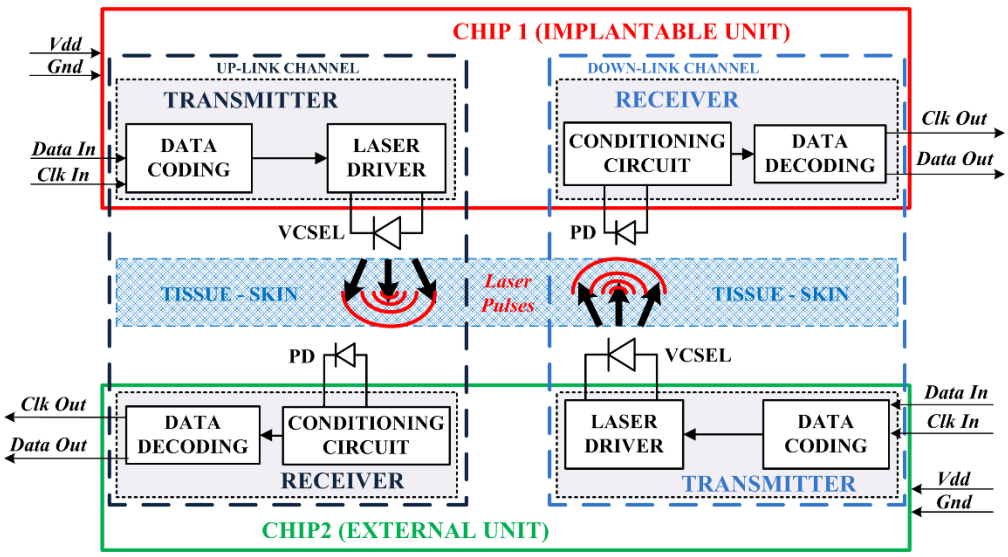


Figure 34 - Block scheme of the implemented IC for optical data link in biotelemetry systems.

The overall system has been developed in CMOS integrated technology using the Cadence Design Systems Virtuoso tool suite using a commercially-available 0.35 µm CMOS technology provided by AMS. The complete system layout including also the integrated PDs and the physical bondpads (with ESD protections) is shown in Figure 35. The overall size of complete test chip design is 1.6×2 mm^2. It should be noted that the core circuits themselves only occupy approximately 0.13 mm^2 (the transmitter: 53 transistors and 1 resistor; the receiver: 60 transistors). The simulated circuit operates with a single 3.3 V supply voltage,

Preliminary experimental results validated the correct functionality of the overall integrated system demonstrating its capability to operate, also in a bidirectional mode, at bit rates up to 250 Mbps with pulse widths down to 1.2 ns and a minimum total power efficiency of about 160 pJ/bit in the conditions for which the transmitter and the receiver work simultaneously on the same chip.

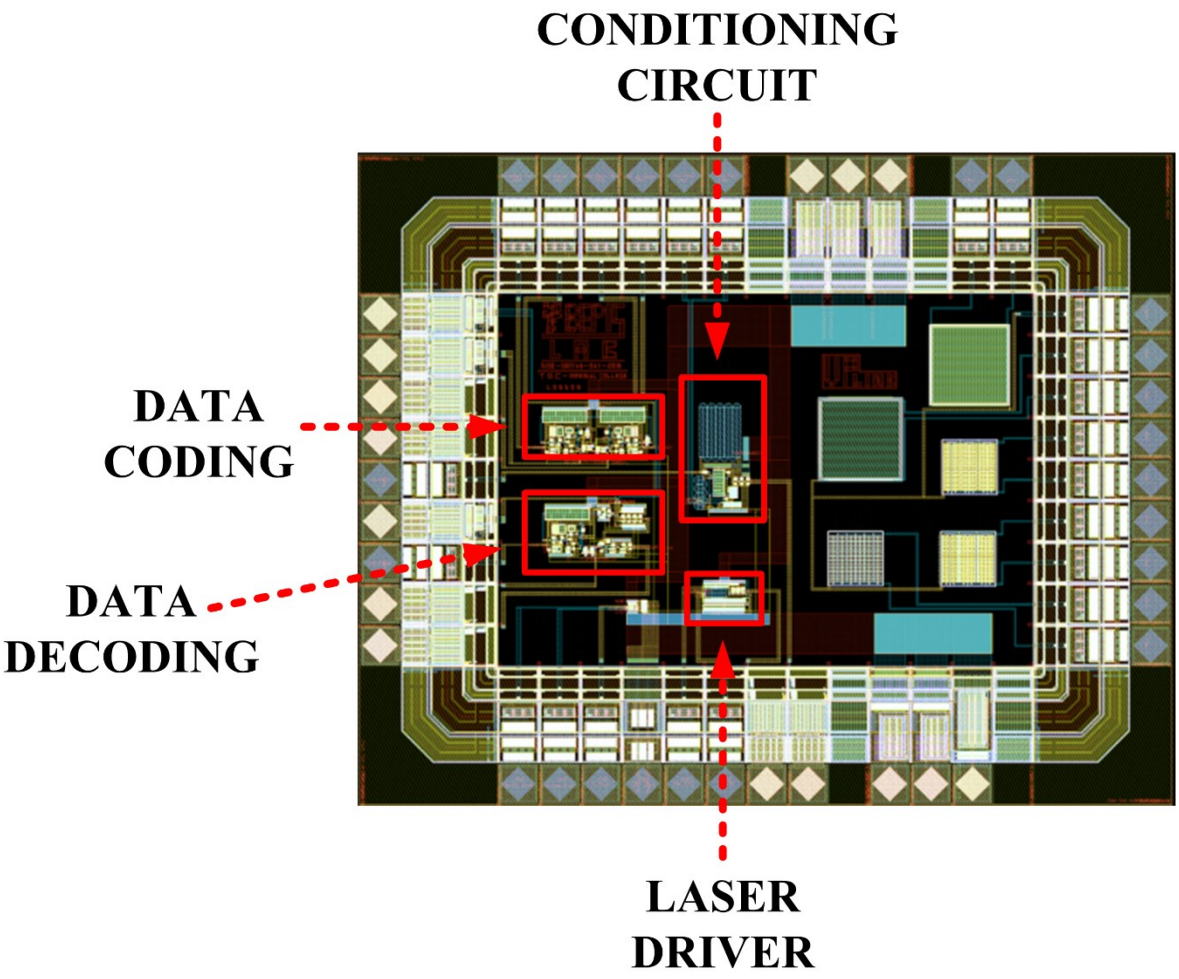


Figure 35 - Complete layout design of the optical biotelemetry system.

Both the versions (the integrated circuit and using discrete components) employ a VCSEL laser (VCSEL-850 by Thorlabs) emitting at the wavelength of λ=850 nm and a high-speed PD (FDS-025 by Thorlabs). Additionally, a suitable test-bench has been implemented on the FPGA board for the emulation and generation of the bit streams, as well as of the master Clocks and the pulse trains.

The following sub-paragraphs describe before the design of each sub-blocks present in Figure 34, and show the implementation of the system and the experimental results obtained. Moreover, in the last sub paragraph the design of on-chip PDs is reported evaluating the response time for different sizes and geometries. The VCSEL has not yet been integrated because requires a careful additional study and is not compatible with the used standard CMOS technology.

2.2.1. Design of a digital architecture for UWB data coding

It is possible to integrate the coding block on chip by using the standard Si CMOS technology to maintain the same system functionalities. Moreover, a full custom design avoids the use of elements such as a PLL and reduces the power consumption and circuit complexity of the overall system. Now, we will discuss some different microelectronics solutions implemented by standard Si CMOS technology. Referring to Figure 36, the Data Coding architecture is based on simple combinational logic blocks consisting of 2× NOT, 2× NAND and 2× rising edge triggered pulse generators (i.e., the Rising Edge Delay blocks in Figure 36). The schematic circuit of the Rising Edge Delay blocks is reported in Figure 37.

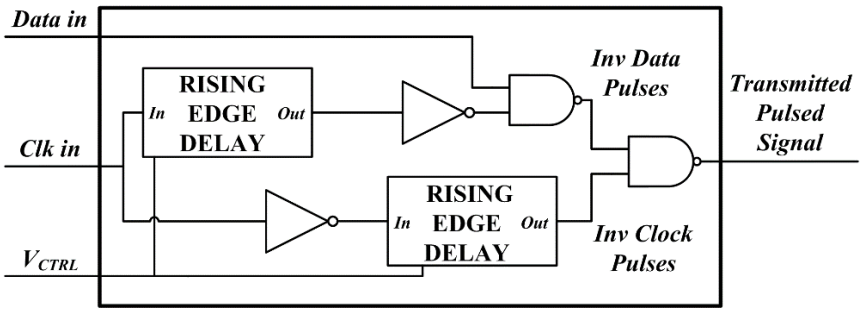
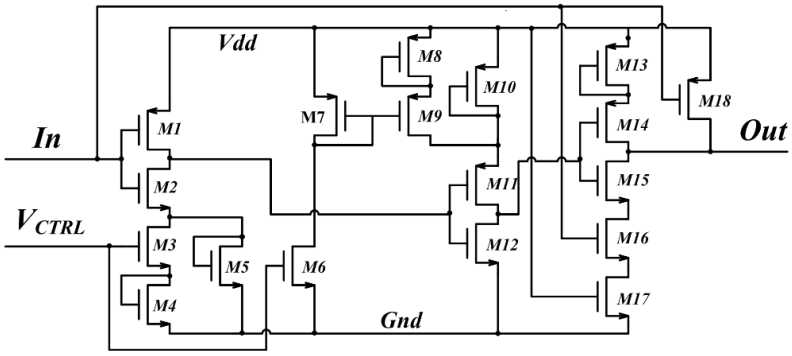


Figure 36 - The architecture at block scheme level of the full-custom DATA CODING block.



Device	W (µm)	L (µm)
M1, M11, M14, M18	15	0.35
M2, M12, M15, M16	6	0.35
M3, M4, M8, M9	24	0.35
M5	6	12
M6	12	0.35
M7	15	100
M10	15	20
M13	15	10
M17	6	1

Figure 37 - Schematic circuit at transistor level of the RISING EDGE DELAY block.

In Figure 37, starting from the Clock input In, the Rising Edge Delay block generates a sequence of voltage pulses with a variable width regulated by the control voltage V_{CTRL}. This control voltage is based on three inverter stages formed by the transistor pairs M1–M2, M11–M12 and M14–M15 and operates as follows: when the voltage V_{CTRL}=0 V, the diode-connected transistor M5 defines the maximum resistance in the pull-down network of the M1–M2 inverter stages. In a similar way, the diode-connected transistor M10 sets the maximum resistance in the pull-up network of the M11–M12 inverter stage. Under these operating conditions, the maximum time delay is achieved. By increasing the value of V_{CTRL}, the transistor M3 and current mirrors M6–M7–M9 progressively turn on so increasing the current flowing through the transistors M4–M8. This design results in an overall reduction of the delay between the rising edges of the input and output signals. The circuit, however, is designed to directly respond to the falling edge of the input Clock signal. This is achieved through the transistor M18 in such a way that only the input rising edge is delayed by the Rising Edge Delay block. In Figure 38, a post-layout simulation of the pulse generator is reported: the red waveform is an input clock set at 50 MHz, the green waveforms are the inverted output of the Rising Edge Delay Block with different values of V_{CTRL}: 1.3 V for the green waveform in the middle and 1 V for the green one at the bottom of then Figure 20. Referring now to the entire digital coding block of Figure 36, the input Clk in follows two different paths to provide voltage pulse trains with a relative phase shift equal to 180° (i.e., equal to the half Clock period). These signals are then combined with the Data-In input data stream through the NAND gates to generate a single output pulse train that contains both the Clock Pulses and the Data Pulses signals.

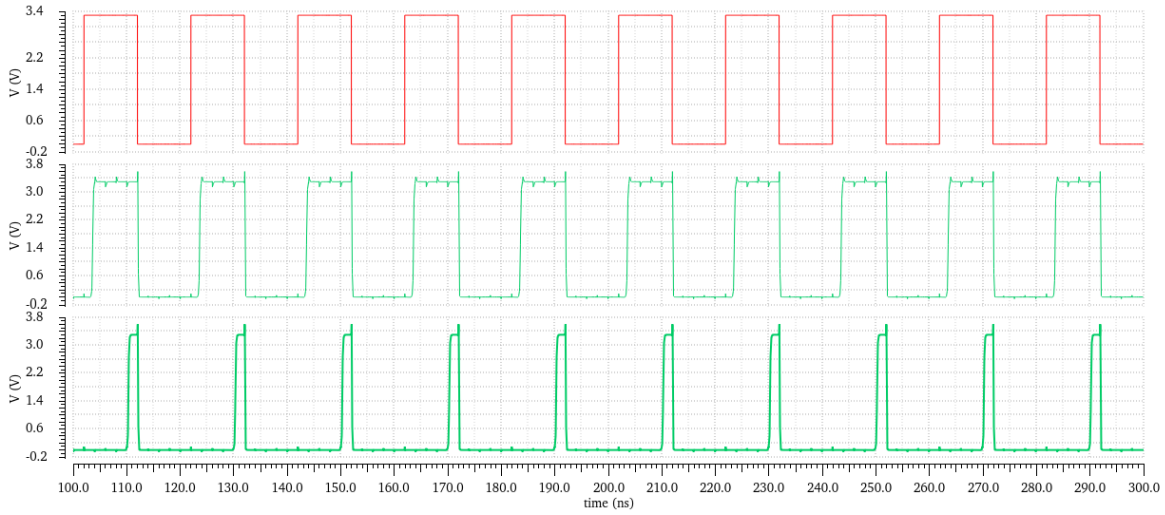


Figure 38 - Post layout simulation of the Rising Edge Delay block.

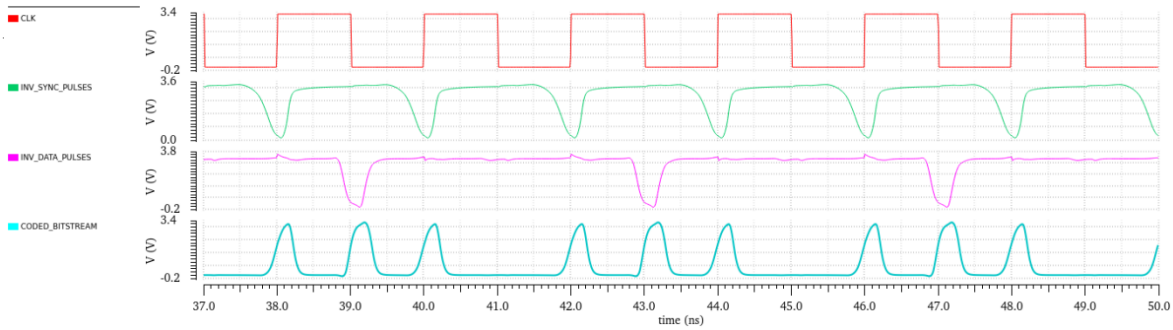


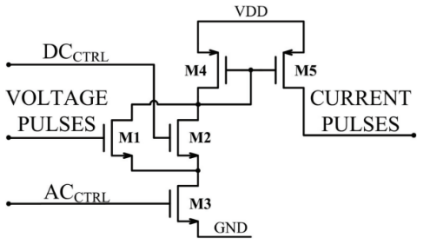
Figure 39 - Post layout simulation of the Data Coding block.

Figure 39 shows a simulation of the Data Coding block. Starting from a Clock at a frequency of 500 MHz (the Red waveform) and from the bitstream to be transmitted equal to a sequence of zero's and one's, the system is able to generate: an inverted copy of the synchronism pulses (the green waveform), an inverted copy of the data pulses (the violet waveform) and the coded bitstream resulting from a NAND operation of the previous two traces (the blue waveform). The system is able to generate sub-nanosecond voltage pulses reducing the time duration of the optical pulses and, subsequently, the electrical power consumption of the overall system.

2.2.2. Design of conditioning circuits for lasers and photodiodes

After the design and the implementation of the laser driver circuits on the PCB, we considered to implement them in an integrated full custom circuit paradigm that is reported in Figure 40. As before discussed, also this circuit is based on a current mirror stage formed by the transistors M4–M5 that convert the Voltage Pulses into CURRENT

PULSES to directly drive the VCSEL Laser. Moreover, this circuit allows for the regulation of both the pulsed current amplitude and the DC current level through the two control voltages DC_{CTRL} and AC_{CTRL} that act on the transistors M2 and M3, respectively.



Device	W (µm)	L (µm)
M1, M3	12	0.35
M2	6	7
M4	18	0.35
M5	240	0.35

Figure 40- Schematic circuit of the laser driver.

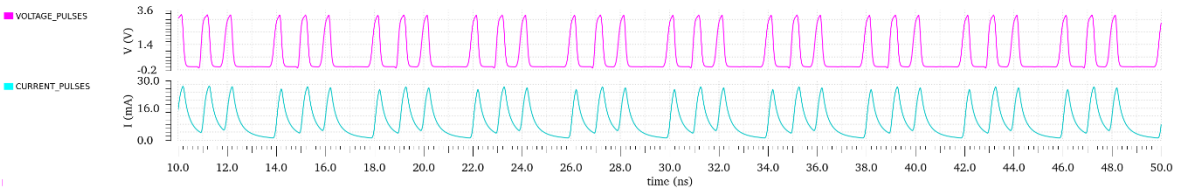
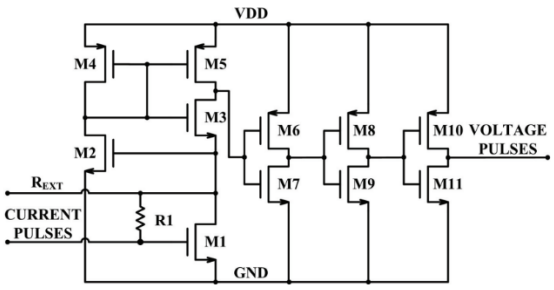


Figure 41 - Simulation result related to the transient response of the laser driver circuit.



Device	W(µm)	L(µm)
M1, M2	500	0.35
M3	60	0.35
M4	100	0.35
M5	85	0.35
M6, M8, M10	18	0.35
M7, M9, M11	6	0.35
R1 = 600Ω	-	

Figure 42 - Schematic of the photodiode interface circuit.

The described solution has been implemented in a commercially available 0.35 µm CMOS technology provided by AMS and operates at 3.3 V supply voltage. The Figure 41 shows a post layout simulation where coded data at 500 Mbps generates a train of current pulses (blue waveform) with a peak value of 30 mA starting from the voltage pulses (violet waveform).

An integrated solution of the TIA-based PD conditioning circuit is shown in Figure 42. This circuit converts the Current Pulsed signals received from the PD generating the corresponding Voltage Pulsed signals. This is accomplished by using a single stage TIA implemented by the transistors M1–M5 with the resistor R1 defining the transimpedance gain. Additional gain is provided through a cascade of three CMOS inverter stages

implemented by the transistor pairs M6– M7, M8–M9 and M10–M11 that generate the output signal Voltage Pulses. Furthermore, the R_{EXT} terminal allows for the overall gain to be precisely adjusted through an optional external resistor (i.e., connected in parallel with R1). Using a 70 µA current pulses as input, the time response of the circuit is shown in Figure 43.

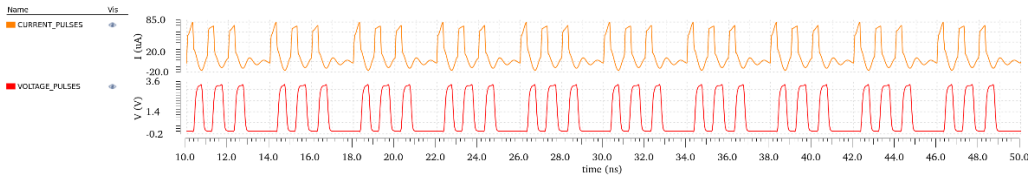
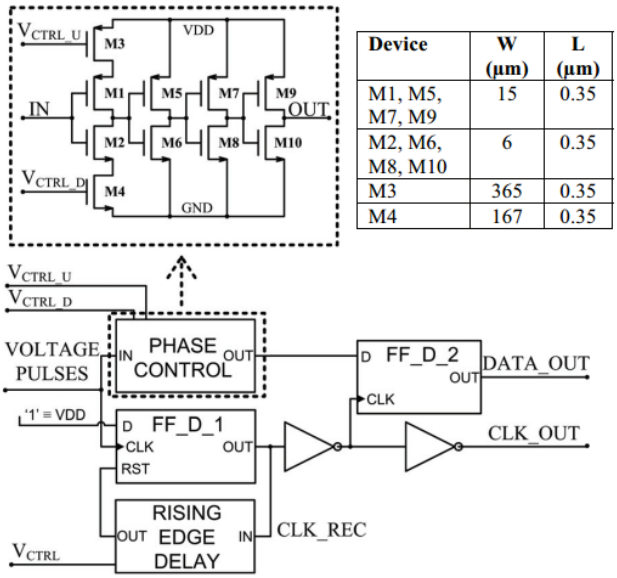


Figure 43 - Simulation result showing the transient time response of the photodiode interface circuit.

2.2.3. Design of a digital architecture for UWB data decoding

The Integrated Circuits Data Decoding system employs the 0.35 µm standard Si CMOS AMS technology and is reported in Figure 44. Similar to the FPGA implementation, the architecture is able to perform the Data and the Clock recovery. The data decoding process is achieved by using 2× D-type FF, 2× inverters, 1× Rising Edge Delay block (equal to that one previously described in Figure 37) and 1× Phase Control block.

The Data Decoding operates as follows: The Received Voltage Pulses drive the Clock input CLK of FFD1 with the data input D fixed to the logic level {1}. In this way, the first incoming Synchronism Pulse sets the output of FFD1 to a high logic level and thus, any further Data Pulse cannot affect the FFD1 output. The FFD1 output signal is then maintained through the Rising Edge Delay block. After this fixed time delay, the Rising Edge Delay triggers the FFD1 asynchronous reset pin RST to toggle its output back to the low logic level {0}. The system is now ready to accept the next Synchronism Pulse. Since there is a fixed phase relationship between the Synchronism Pulses and the Data Pulses signals, it is essential to adjust the pulse delay for different data rates through the Rising Edge Delay block in order to guarantee a delay value between $T/2$ and T, with T the Clock period (i.e., the period between two consecutive Synchronism Pulses of Figure 14). Consequently, the output of FFD1 provides the recovered Clock signal Clk_Out with a duty cycle higher than 50% (i.e., half of a Clock period plus the additional pulse delay). Thus, FFD2 receives the inverted recovered Clock and acquires the data input provided by Data Pulses. In order to avoid a metastable state in FFD2, a PHASE CONTROL has been included to guarantee the FFD2 setup and hold times. Referring to Figure 44, the PHASE



Device	W (µm)	L (µm)
M1, M5, M7, M9	15	0.35
M2, M6, M8, M10	6	0.35
M3	365	0.35
M4	167	0.35

Figure 44 - Circuit schematic of the digital decoding block.

CONTROL block consists of 4× inverter stages implemented by the transistor pairs M1–M2, M5–M6, M7–M8 and M9–M10. The transistors M3–M4 are also driven by the control voltages V_{CTRL_U} and V_{CTRL_D} that allow for the pulse width of the Received Pulsed Signal to be extended. Finally, FFD2 provides the decoded Data Out signal with a stable value corresponding to the rising edges of the recovered Clock signal Clk_Out.

In Figure 45 we report a post layout simulation performed at 500 Mbps. The design and simulations have been performed using Cadence Virtuoso Design Suite and show how the system, starting from a coded signal (the red waveform in the Figure) is able to regenerate a synchronism signal (the violet waveform) and the bitstream (blue waveform). These results demonstrate that the transmitted repeated bit sequence {0,1} is correctly decoded by the receiver and is in synchronisation with the recovered clock signal.

In order to perform an appropriate system analysis, the VCSEL and the PD have been simulated by an RLC-type passive load and a non-ideal current pulse generator including RC parasitic elements, respectively. In Table 2 is reported the estimated electrical power consumption of the complete communication system. It is possible to observe how the power consumption decreases reducing the width of the pulses.

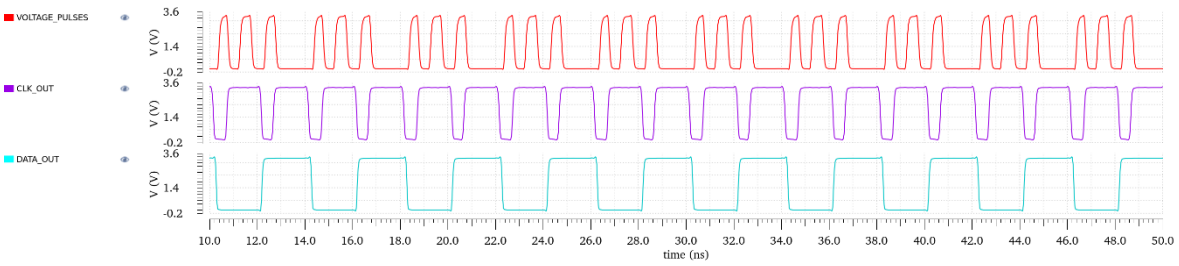


Figure 45 - Simulation result of the Data Decoding block.

Table 2 – Power efficiency of transmitter (TX) and receiver (RX).

Data rate (Mbps)	Pulse width = 300 ps		Pulse width = 500 ps	
	Tx (pJ/bit)	Rx (pJ/bit)	Tx (pJ/bit)	Rx (pJ/bit)
125	85	121	94	121
250	57	67	65	67
500	34	40	41	40

2.2.4. Experimental setup and measurements

For the experimental setup of the integrated circuit version of the designed optical wireless biotelemetry system, the microphotograph of the fabricated ASIC including the pad ring (i.e., ESD protection I/Os and physical bond-pads) is shown in Figure 46. The overall chip (being a pad limited design) measures 1.6x2 mm^2 and has been encapsulated into a JLCC44 (44 pins) ceramic package. The chip has been evaluated through a custom 4-layer designed PCB (Figure 47) that houses the ASIC and allows for SMA connection to external modules and instruments for the test measurements. The complete system is capable to correctly transmit and receive data operating also in a full-duplex mode. It employs VCSEL-850 (Thorlabs) (λ=850 nm, 2.2mA threshold current) and a FDS-025 PD (Thorlabs) (high-speed Si-based PD with 47 ps response time and 250 μm active area diameter), that are the same used in commercial components configuration.

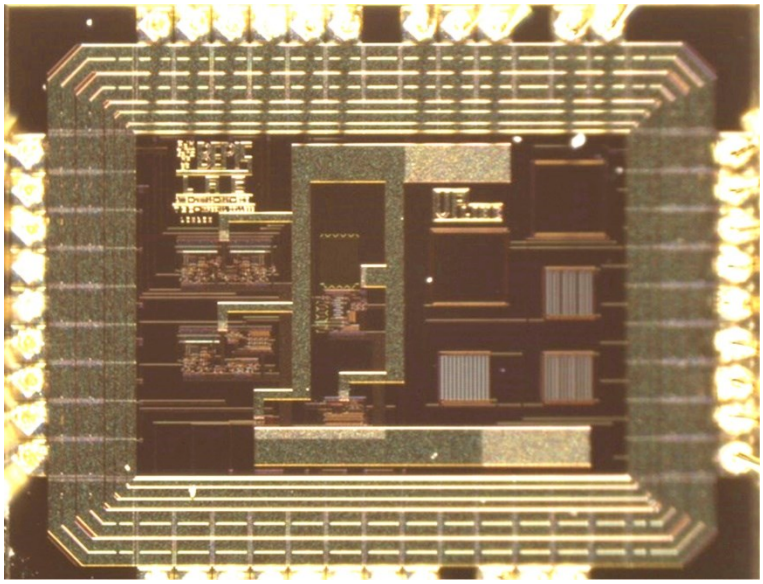


Figure 46- Microphotograph of the fabricated ASIC.

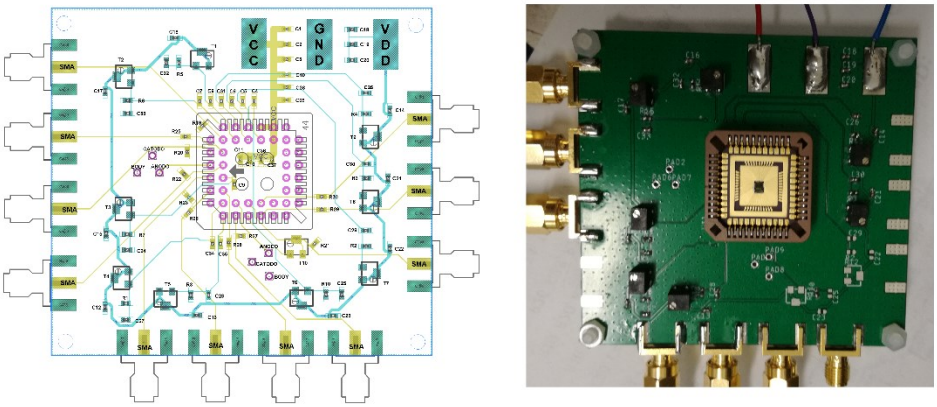


Figure 47 - Layout and photo of the fabricated PCB for the chip experimental test, characterization and measurements.

Also in this case, the system characterization has been performed using a VCSEL-850 (Thorlabs) (λ=850 nm, 2.2mA threshold current) and a FDS-025 PD (Thorlabs) (high-speed Si-based PD with 47 ps response time and 250 μm active area diameter). Additionally, a suitable test-bench for the generation of bitstreams, master clocks and pulse trains, has been implemented on a Xilinx VIRTEX-6 XC6VLX240T FPGA board. A photo of the experimental setup is shown in Figure 48. In particular, according to the scheme reported in Figure 34, two PCBs (shown in Figure 47) have been mounted facing each other so to implement a simultaneous bidirectional link by using two couples of VCSEL and PD. Two XYZ translation stages allowed for the proper optical alignment of the VCSEL and PD along the X- and Y-directions and for the regulation of their relative distance along the Z-direction. Moreover, two 1.5 mm diffusers ED1-C20-MD (Thorlabs) have been inserted between the VCSELs and the PDs to emulate skin/ tissue effects such as light attenuation, diffusion and scattering. Several measurements have been taken using a 6 GHz, 20 GS/s LeCroy WaveMaster 8600A digital oscilloscope so to evaluate the main system parameters, characteristics and time responses under different operating conditions. Concerning the experimental setup of the integrated circuit version of the described optical wireless biotelemetry system, a preliminary experimental measurements are reported below, demonstrating the correctly system working in full-duplex mode. In all the results shown, the coded pulse width is about 1.2 ns with a maximum peak current level driving

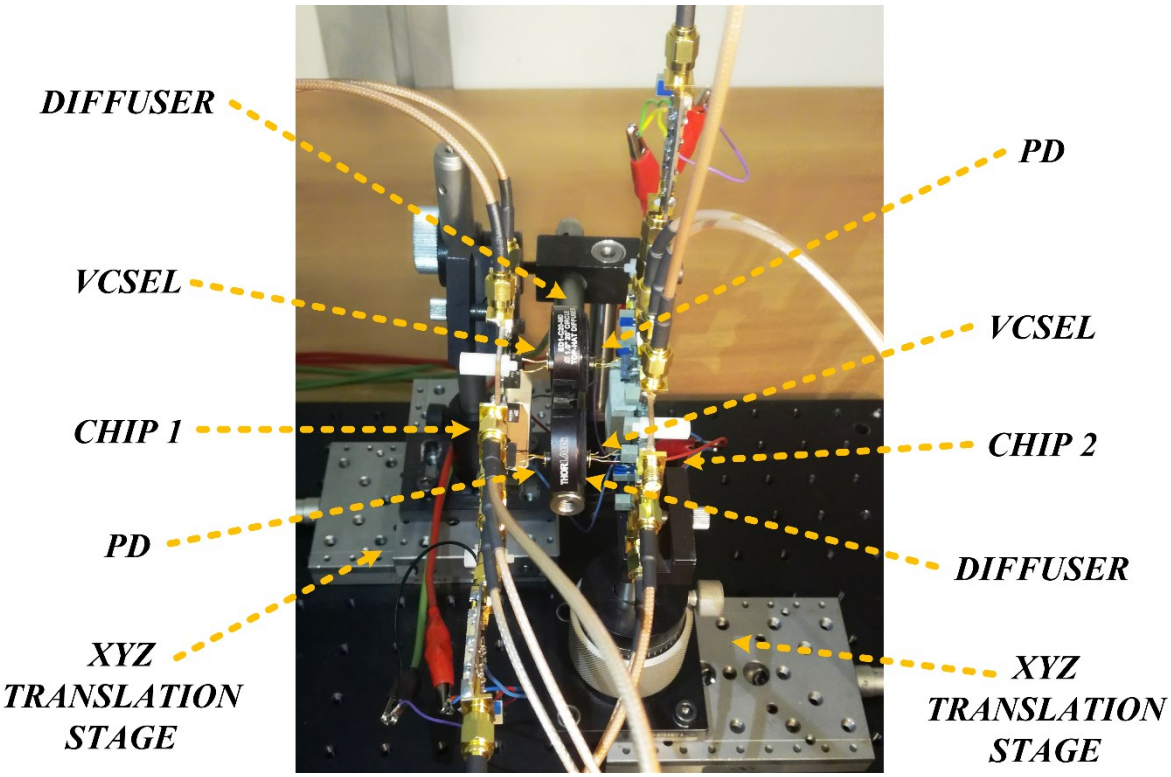


Figure 48 - Experimental setup used for the ASIC characterization.

the VCSEL of approximately 24 mA. The transmitted bit stream used is a repetition of a {0,1} bit sequence to quickly and better evaluate the correctness of the system operation and functionality.

Figure 49 reports the experimental timing diagrams only the uplink channel of the complete system (i.e., a transmitter and a receiver operating on two separate, identical chips) with the main system signals demonstrating the capabilities of the system to operate correctly at 250 Mbps with a minimum power efficiency of about 160 pJ/bit and a maximum BER of 10^{-10}. It is important to observe that the recovered clock signal presents a duty-cycle higher than 50% which, if required, could be simply compensated by a suitable duty-cycle correction circuit [27] that has been optimized and described by the candidate in the appendix D.

Moreover, concerning the results of Figure 50, for both the transmission channels that works simultaneously, bit rate of the uplink channel is 250 Mbps while the downlink channel bit rate is equal to 50 Mbps.

Moreover, in Figure 51 it is shown a comparison of a coded signal generated by the FPGA board (the violet waveform) and the same coded signal employed using the implemented integrated circuits (the yellow waveform).

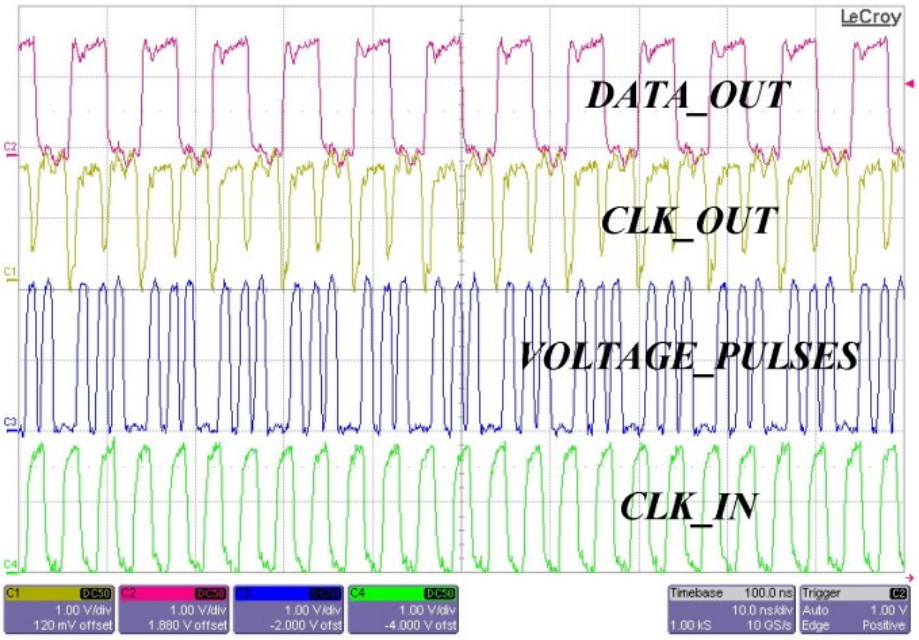


Figure 49 - Experimental measurement: main signals related to a communication channel operating at 250 Mbps and transmitting a repeated {0,1} bitstream.

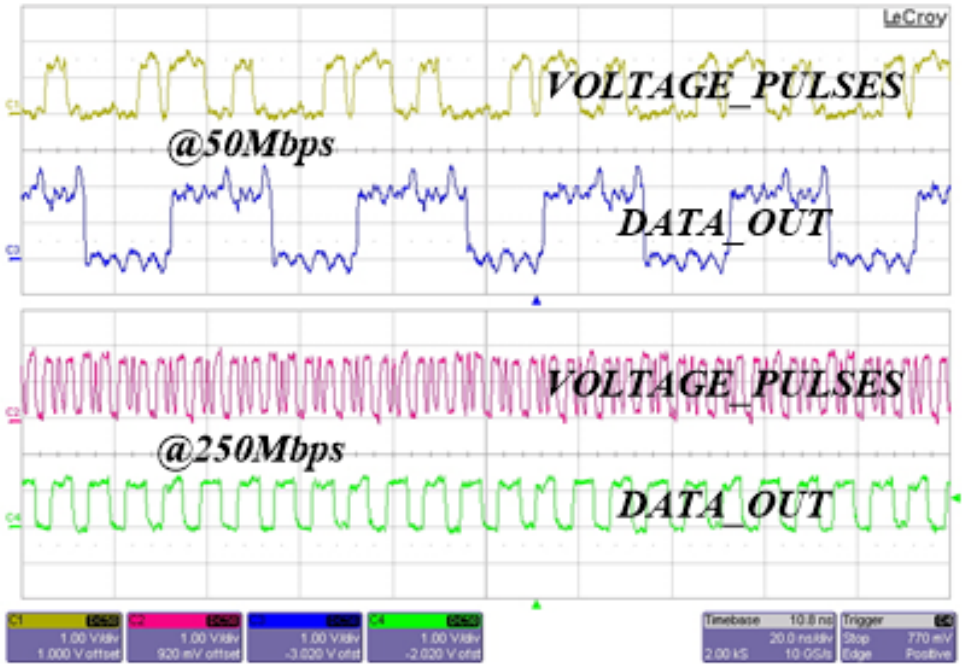


Figure 50 - Measured signals related to a bidirectional communication link operating at 250 Mbps (uplink channel) and 50 Mbps (downlink channel) transmitting a repeated {0,1} bitstream.

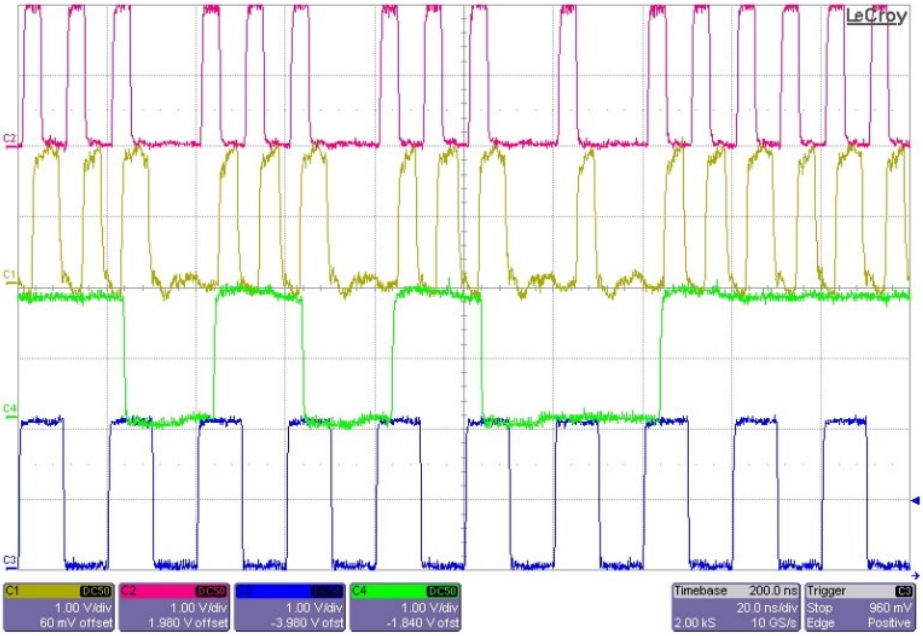


Figure 51 - Comparison between the coded signal generated by the FPGA board and by the developed ASIC.

Table 3 summarizes the power efficiencies of the transmitter and the receiver subsystems working at bit rates equal to 50 Mbps, 125 Mbps and 250 Mbps, a pulse width of 1.2 ns and a pulse peak current of 24 mA. These results have been obtained considering the best optical alignment along X- and Y-directions and a maximum distance of 3 mm between the VCSEL and PD along the Z-direction, including the diffuser that reduces the laser power by a factor 10.

Table 3 - Power Efficiency of the Transmitter (Tx) and Receiver (Rx) subsystems under different operating conditions.

Data rate (Mbps)	**Power efficiency (pJ/bit)**	
	Transmitter (Tx)	***Receiver (Rx)***
50	*174*	*202*
125	*125*	*121*
250	*93*	*67*

2.2.5. Full Custom design of integrated photodiodes

In this sub-paragraph a full custom design of integrated PDs is described. Planar diffused silicon PDs are simply P-N junction diodes (see Figure 52). A P-N junction can be formed by diffusing either a P-type impurity (anode), such as Boron, into a N-type bulk silicon wafer, or a N-type impurity, such as Phosphorous, into a P-type bulk silicon wafer. The diffused area defines the photodiode active area. Silicon is a semiconductor with a band gap energy of 1.12 eV at room temperature. This is the gap between the valence band and the conduction band. At absolute zero temperature the valence band is completely filled and the conduction band is vacant. As the temperature increases, the electrons become excited and escalate from the valence band to the conduction band by thermal energy. The electrons can also be escalated to the conduction band by particles or photons with energies greater than 1.12eV, which corresponds to wavelengths shorter than 1100 nm. The resulting electrons in the conduction band are free to conduct current [28] [29] [30] [31] [32].

Due to concentration gradient, the diffusion of electrons from the N-type region to the P-type region and the diffusion of holes from the P-type region to the N-type region, develops a built-in voltage across the junction. The inter-diffusion of electrons and holes between the N and P regions across the junction results in a region with no free carriers. This is the depletion region. The built-in voltage across the depletion region results in an electric field with maximum at the junction and no field outside of the depletion region. Any applied reverse bias adds to the built-in voltage and results in a wider depletion region. Starting from the simplified electrical model of a PD in Figure 53, the C_J is the

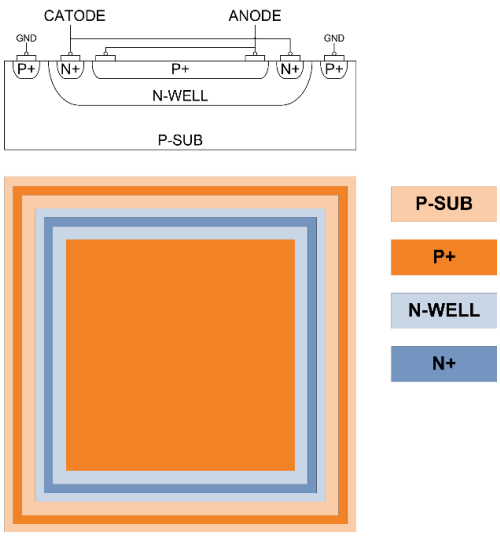


Figure 52 - PD structure.

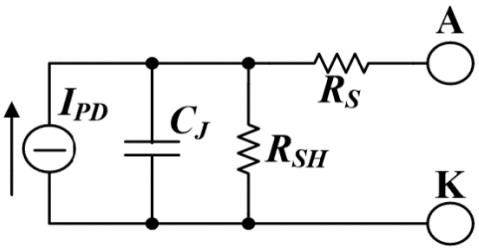


Figure 53 - PD simplified electrical model.

most important parameter in order to evaluate the PD time response for a fast optical data link. The boundaries of the depletion region act as the plates of a parallel plate capacitor (Figure 52). The C_J is directly proportional to the diffused area and inversely proportional to the width of the depletion region. In addition, higher resistivity substrates have lower junction capacitance. Furthermore, the capacitance is dependent on the reverse bias.

When a Si PD is designed using Cadence Virtuoso Environment with a specific technology (in this case TSMC 180 nm library), some process parameters can't be changed (such as dope density/penetration depth). So, it is important to evaluate the C_J as function of the PD geometry.

2.2.5.1. Design, analysis and simulations – TSMC 0.18µm CMOS Technology

For this purpose, we can consider a PNP BJT layout from TSMC 180 nm library. As shown in Figure 54, the layout of the BJT is similar to the PD shown in Figure 52 (except for a metal layer present in the BJT emitter and, obviously, missing in the active area of an integrated PD). In this similitude, the emitter area of the BJT model (equal to W*L) are equivalent to the PD active area. Under these considerations, the electrical model of a PD has been compared with a BJT and Diode library model, as reported in Figure 55.

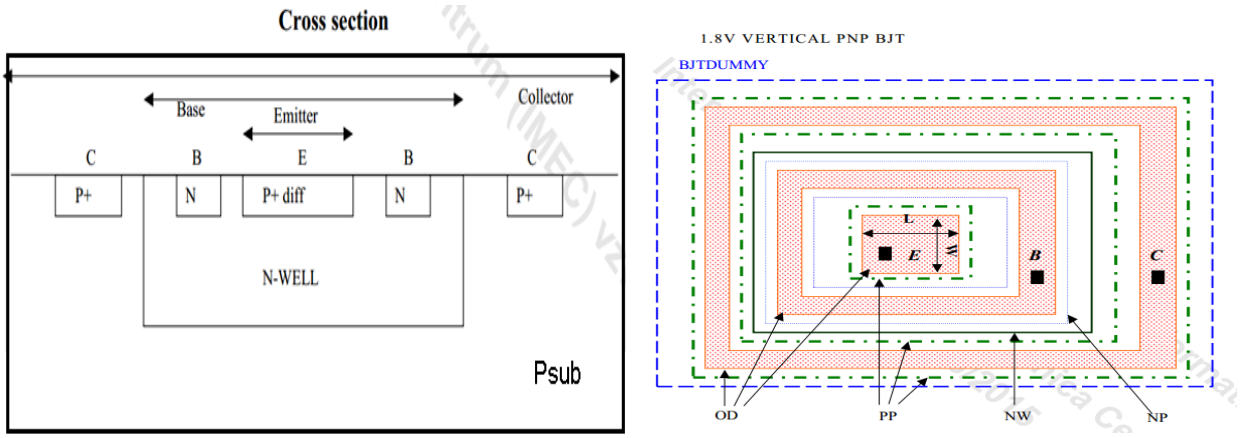


Figure 54 - PNP BJT layout from TSMC 180 nm library.

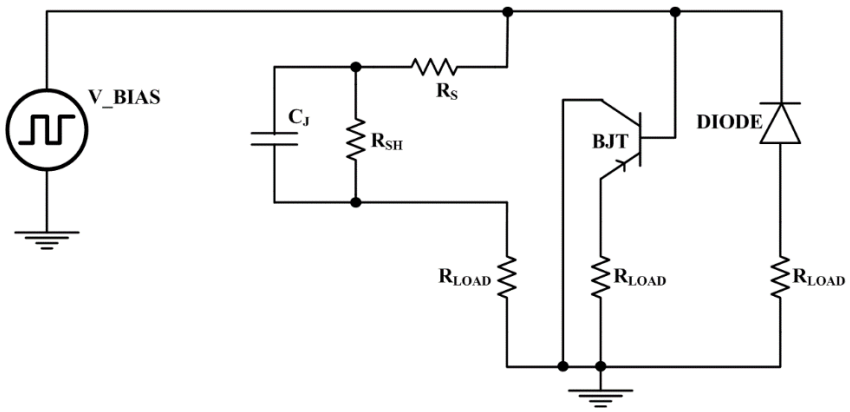


Figure 55 - Comparison between a simplified PD model, a TSMC BJT component and a TSMC Diode component.

The V_{BIAS} signal is a 50 mV square wave at 1 MHz with DC = 0V, R_{LOAD} is equal to 10 kΩ, R_{SH} = 100 MΩ. The C_J-R_{LOAD} derivates the signal, such as C_JBJT-R_{LOAD} or C_J Diode-R_{LOAD}. So, with fixed values of BJT-Diode area, it is possible to change the C_J value of the PD electrical model until the three circuit reach the same results, as shown in Figure 56. The resulting C_J value represents the C_J between Base and Emitter node of the BJT, equal to the C_J integrated PD with the same BJT active area. R_{SH} doesn't affect the results for values greater than 100 MΩ.

In Table 4 is reported the resulting C_J under different BJT configuration. These results are comparable with the C_J values obtained using the ideal model of a PD implemented in Matlab, with an error less than 5%. Under these considerations, the following PDs (from Figure 57 to Figure 62) are been designed:

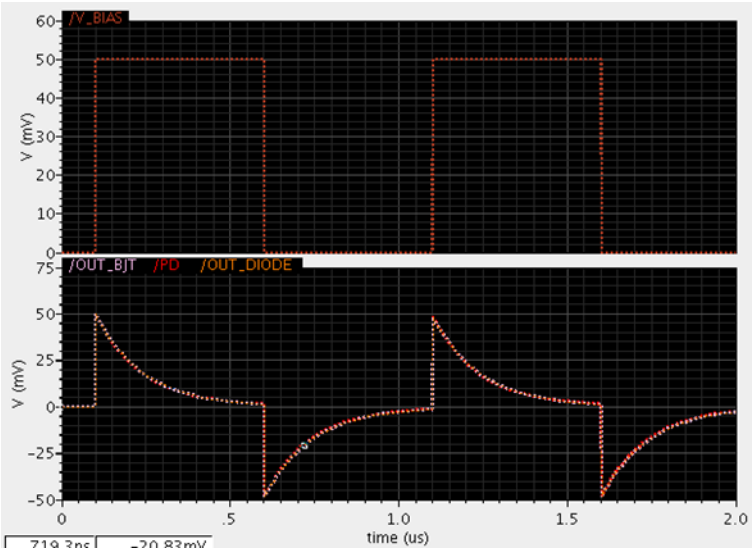


Figure 56 - Comparison between the response of a simplified PD model, a TSMC BJT component and a TSMC Diode component (bottom picture) respect a square wave input (on top).

Table 4 - CJ values for different BJT configuration.

BJT CONFIGURATION	SINGLE BJT 2µm X 2µm	TOTAL EMITTER AREA 4 µm^2	C_J = 4.5 fF
	SINGLE BJT 5µm X 5µm	TOTAL EMITTER AREA 25 µm^2	C_J = 25 fF
	SINGLE BJT 10µm X 10µm	TOTAL EMITTER AREA 100 µm^2	C_J = 80 fF
	PARALLEL OF 4 BJT 5µm X 5µm	TOTAL EMITTER AREA 100 µm^2	C_J = 80 fF
	PARALLEL OF 25 BJT 2µm X 2µm	TOTAL EMITTER AREA 100 µm^2	C_J = 87 fF
	PARALLEL OF 100 BJT 2µm X 2µm	TOTAL EMITTER AREA 400 µm^2	C_J = 360 fF
	PARALLEL OF 100 BJT 10µm X 10µm (i.e., 100µm X 100µm)	TOTAL EMITTER AREA 10000 µm^2	C_J = 8,5 pF
	PARALLEL OF 400 BJT 10µm X 10µm (i.e., 200µm X 200µm)	TOTAL EMITTER AREA 40000 µm^2	C_J = 34 pF
	PARALLEL OF 2500 BJT 10µm X 10µm (i.e., 500µm X 500µm)	TOTAL EMITTER AREA 250000 µm^2	C_J = 210 pF

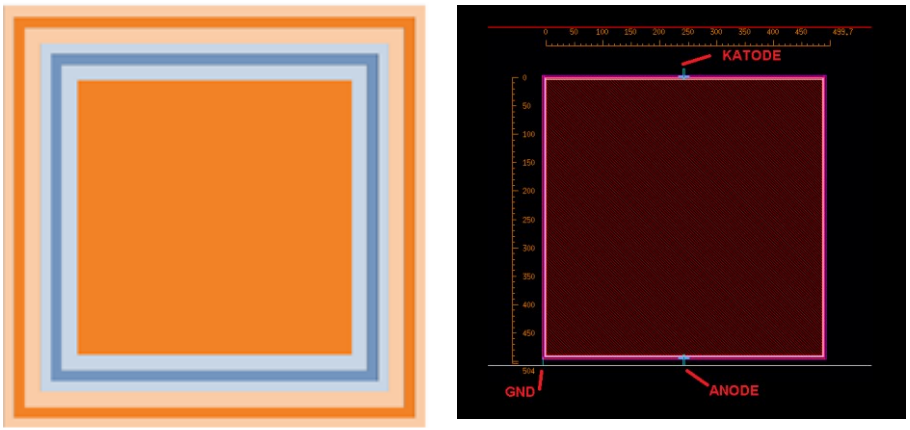


Figure 57 - PD Layout, PNP junction of 500x500 µm2 (0.25 mm2) for optical power transfer applications.

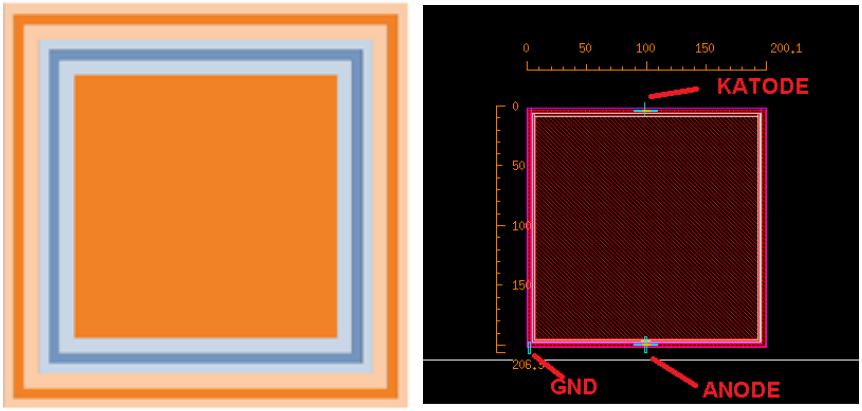


Figura 58 - PD Layout, PNP junction of 200x200 µm2 (0.04 mm2).

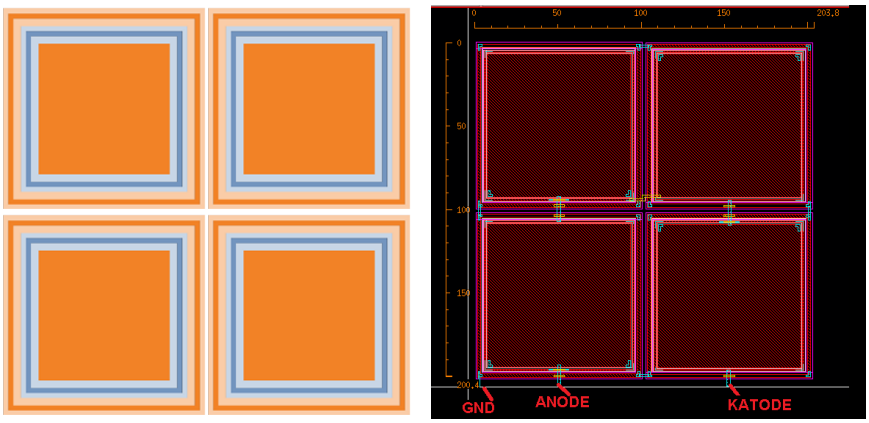


Figure 59 - Layout of four PNP junction of 100x100 µm2 each connected in series (0.04 mm2).

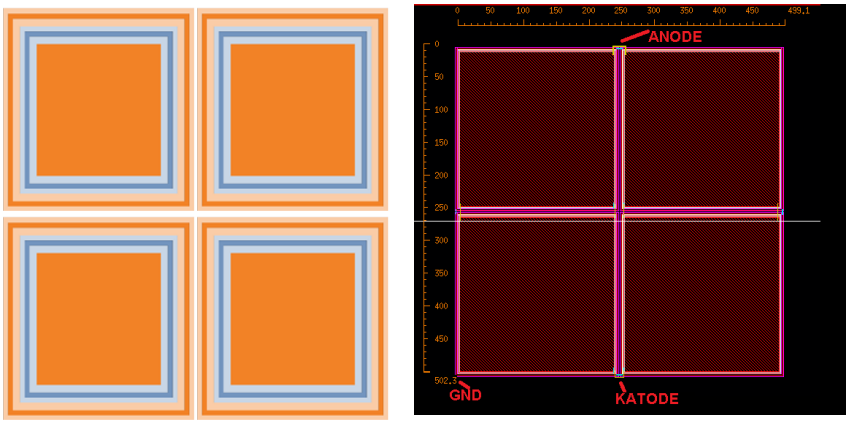


Figure 60 - Layout of four PNP junction of 100x100 µm2 each connected in parallel (0.04 mm2).

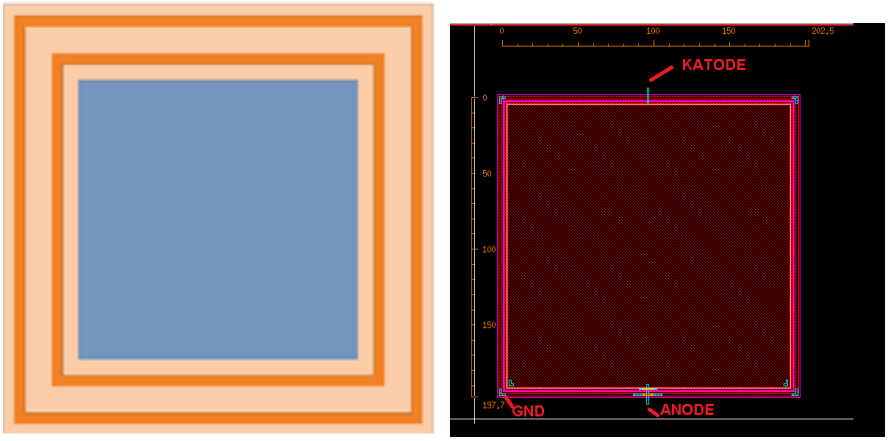


Figure 61 - PD Layout, NP junction of 200x200 µm2 (0.04 mm2).

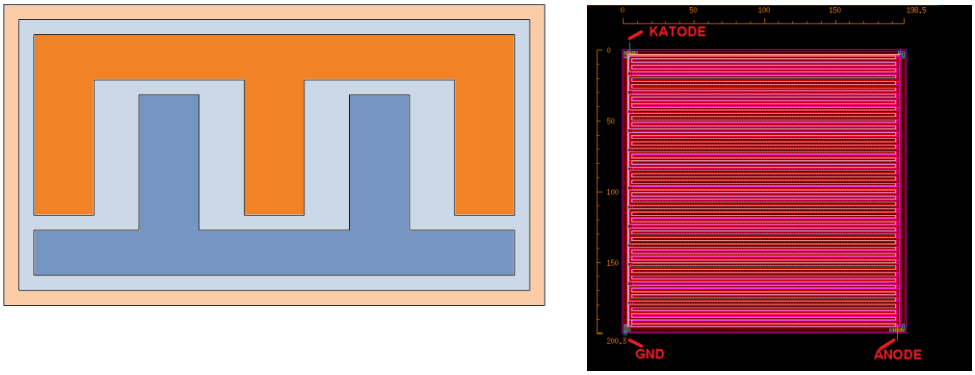


Figure 62 - PD Layout, roost structure PNP junction of 200x200 µm2 (0.04 mm2) [33].

Some of these PDs have been implemented in the chip layout shown in Figure 13B of Appendix B, the chip is actually under fabrication.

2.2.5.2. Design, analysis and measurements – AMS 0.35µm CMOS Technology

In addition, preliminary experimental measurements have been performed using the PDs integrated in the microchip shown in Figure 46 of Chapter 2.2.4. The four PDs topologies are realized using a AMS 0.35 µm technology and are described below. The PD1 is made by 120 NWELL as shown in Figure 63, each NWELL has an area of 3µm x 19µm and all Katode and Anode connections are collected in parallel. The PD2 is described in Figure 64and has a configuration similar to PD1 except for the Anode connections that share the same NWELL of the Katodes. The last two PDs, PD3 and PD4, are simply a replica of PDs in Figure 61 and Figura 58, respectively. These four PDs have been tested assuming an incident optical power around 100 µW generated by a red laser with λ equal to 650 nm. Each PD has been first connected in photovoltaic mode (Figure 65 (a)) and, using a continuous illumination, the open circuit Voltage (V_{OC}) and the short circuits Current (I_{SC}) have been evaluated. Subsequently, the PDs have been connected in photoconductive mode (Figure 65 (b)) and, starting from a 4 kHz pulsed light source generated using a chopper, the peak-to-peak Voltage (V_{P-P}) of each photodiode output has been measured, changing the V_{BIAS} applied. The preliminary experimental results are summarized in Table 5.

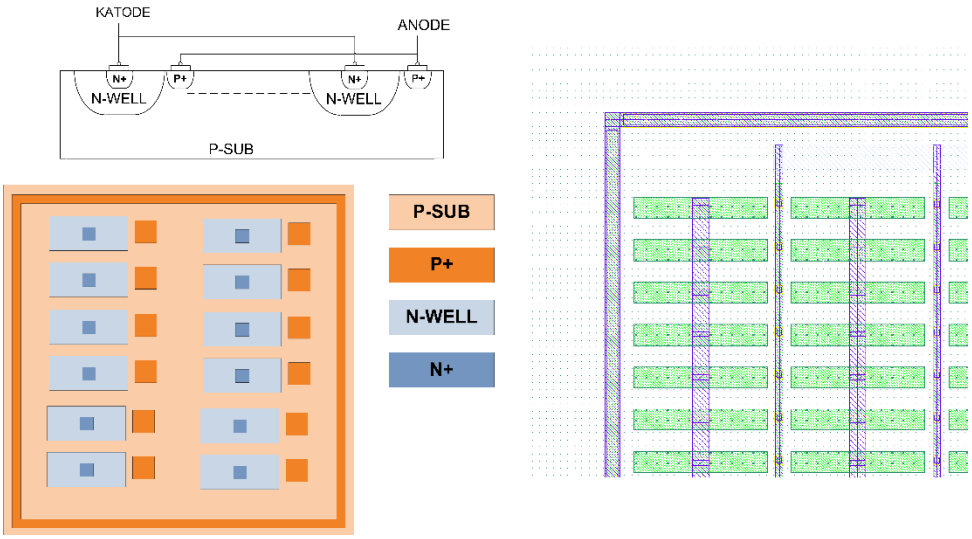


Figure 63 - PD1 Layout.

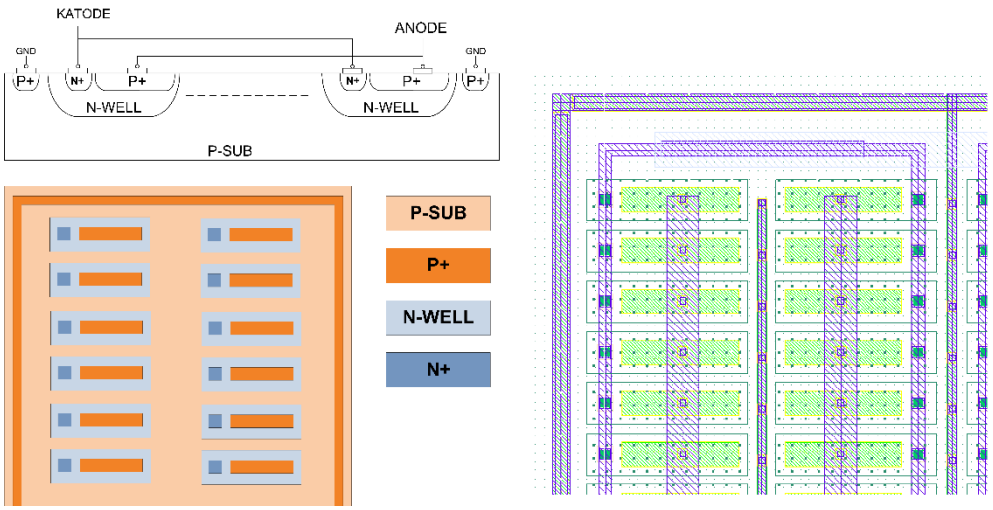


Figure 64 - PD2 Layout.

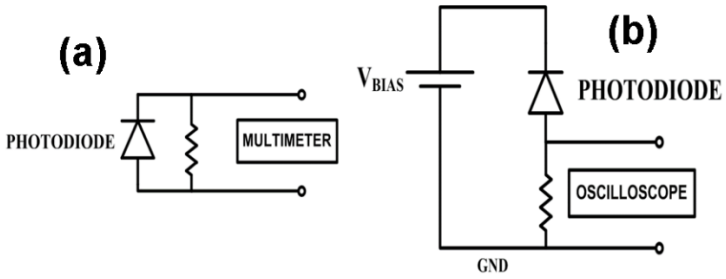


Figure 65 - Experimental setup: (a) PD connected in photovoltaic mode and (b) PD connected in photoconductive mode.

Table 5 - Preliminary experimental results.

	PD1	**PD2**	**PD3**	**PD4**
V_{oc}	474 mV	465 mV	469 mV	491 mV
I_{sc}	4 µA	0.9 µA	1.85 µA	2.08 µA
V_{p-p} at 4 kHz (Vbias=0 V)	0.32 V	0.14 V	0.3 V	0.3 V
V_{p-p} MAX at 4kHz	1.06 V (Vbias=1.5 V)	1.04 V (Vbias=2 V)	0.72 V (Vbias=1 V)	1.08 V (Vbias=2.5 V)

3. OPTICAL DATA LINK - APPLICATIONS

This Chapter reports two applications of the optical data link system discussed in the previous two Chapters. The first application is in the robotic field and makes use of an event-driven serial communication employing an optical fiber [34] [35]. This activity has been developed in collaboration with the iCub Facility of the IIT (Istituto Italiano di Tecnologia) in Genova, Italy. The second application is in the field of prosthetic devices for which has been realized an FPGA-based tactile sensory feedback system. Also in this case the data communication link employs an optical fiber [36] [37]. This activity has been realized in collaboration with the COSMIC Lab, University of Genova, Italy.

3.1. Event-driven serial communication on optical fiber for the humanoid robot iCUB

Nowadays, robots are equipped with an increasing number of different kind of sensors to gather as much as possible information from the external world in order to make decisions or handle some specific job. Processing such a large quantity of data poses hard engineering challenges for optimizing the acquisition of the information, guarantee the system robustness, and, at the same time, provide a large bandwidth electronic and/or optoelectronic devices with a reduced electrical power consumption and latency. In this sense, one possible solution is the use of event-driven sensing whereby the signal coming from the sensors is sampled only when there is a variation of the signal itself. Thus, the sampling rate, the data transfer and processing depend on the dynamics of the stimulus. For example, if we consider a sensor of temperature, for the real robotic applications it is of interest only when and in which part of the robot the temperature has changed. Thus, in this regard, in Ref. [38] has been proposed an asynchronous serial protocol to integrate event-driven sensors on the iCub humanoid platform, including tactile sensors and accelerometers. In this Reference, has been discussed and validated a prototype able to transmit Impulse Based-Asynchronous-Address Event Representation (IB-AS-AER) data over an optical fiber communication link.

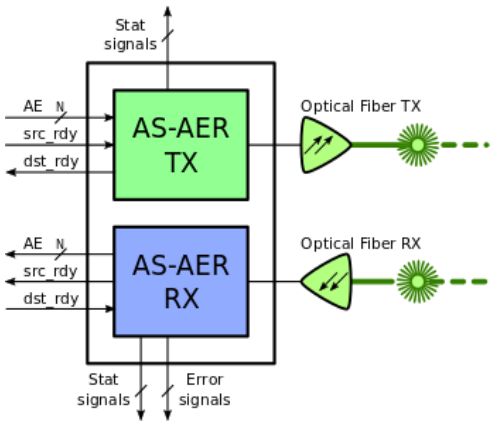


Figure 66 – Overall block diagram of the reference implementation of the transceiver for the developed IB-AS-AER protocol.

Starting our discussion from the general schematic of the system shown in Figure 66, pressure sensors are integrated on the robot fingertips or skin patches, each one interfaced to capacitance-to-digital converters and to a tactile hub, where the pressure value is converted in a suitable event-driven encoding. AER voltage pulses are then converted into current pulses that drive the VCSEL. As discussed, the VCSEL emit a sequence of laser pulses that are the counterpart current one. The generated pulsed laser beam is, then, coupled into an multimode optical fiber that acts as the communication link from the transmitter (i.e., the VCSEL) and the receiver (i.e., the Si photodiode). The receiver converts back the sequence of laser pulses to a sequence of voltage pulses that are, then, acquired in the main processing unit. The contribution to this project is related to the object of this thesis: the realization of the optical communication link able to transmit the sensory signals generated inside the robot body to external devices. In more detail, the optical communication platform is composed by a biasing circuit, based on a current mirror architecture, that converts voltage pulses into current pulses. The current pulses, in turn, drive the VCSEL (VCSEL, OPV314AT by TT Electronics) emitting at λ= 850 nm with a response time lower than 100 ps. The VCSEL is coupled to a 1 m length multi-mode 50/125 mm optical fiber (Duplex, FOPC-F2- M5-DX-FCU-STU-010). Then, in the receiver unit, a high-speed fiber-coupled Si photodiode (DET025AFC/M by Thorlabs), with rise/fall times of about 150 ps, detects the sequence of laser pulses so generating a corresponding sequence of photocurrent pulses. The electronic circuit architectures are similar to those previously described in the Paragraph 2.1.2. Finally, the photodiode is interfaced with a conditioning circuit based on a TIA that converts the sequence of current pulses into a sequence of voltage pulses to be decoded by the receiver electronic circuitry.
In Figure 67 is reported a photo of the experimental set-up implemented to test the overall optical fiber communication link composed by the laser driver, the VCSEL, the optical

fiber, the PD and its signal conditioning circuit. In this regard, a further proper *ad-hoc* test-bench has been developed on a Virtex-6 FPGA board to test and validate the event-driven serial communication protocol on the optical fiber link by performing transmission of data corresponding to 16 bit AER events, with $23^2 \approx 4 \cdot 10^9$ transmissions of events for each conducted test.

Figure 68 shows an example of the main signals, taken from an oscilloscope in the time domain, related to the developed event-based serial communication protocol operating at 100 Mbps. In particular, it reports the signal AS-AER coded by the edge-to-edge intervals approach representing a 16 bit AER event. Simultaneously, the corresponding IB-AS-AER signal is also reported showing the pulse-to-pulse intervals coding technique that provides a train of 2.5 ns voltage pulses always related to a 16 bit AER event. These pulses are then used as the input pulsed signal for the laser driver block of the optical fiber communication link.

Finally, several tests of the overall system, including the optical fiber communication link, have been also performed considering 16 bit AER events, with $2^{32} \approx 4 \cdot 10^9$ transmissions per test at a nominal TX/RX clock equal to 100 MHz (i.e., a raw bit rate of 100 Mbps). Starting from these operating conditions, the TX clock have been spanned in the range 93–107 MHz with different variation steps resulting into a maximum TX/RX clock ratio of ± 7%. Figure 69 reports the achieved results demonstrating that at a bit rate of 100 Mbps, by changing the TX/RX clock ratio of ±2%, the error rate, measured as the number of AER events not correctly received, is equal to zero.

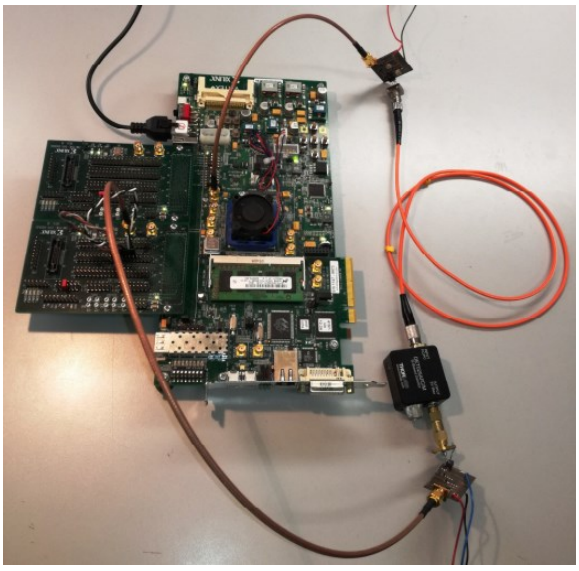


Figure 67 - Photo of the experimental set-up implemented for testing the optical fiber communication link.

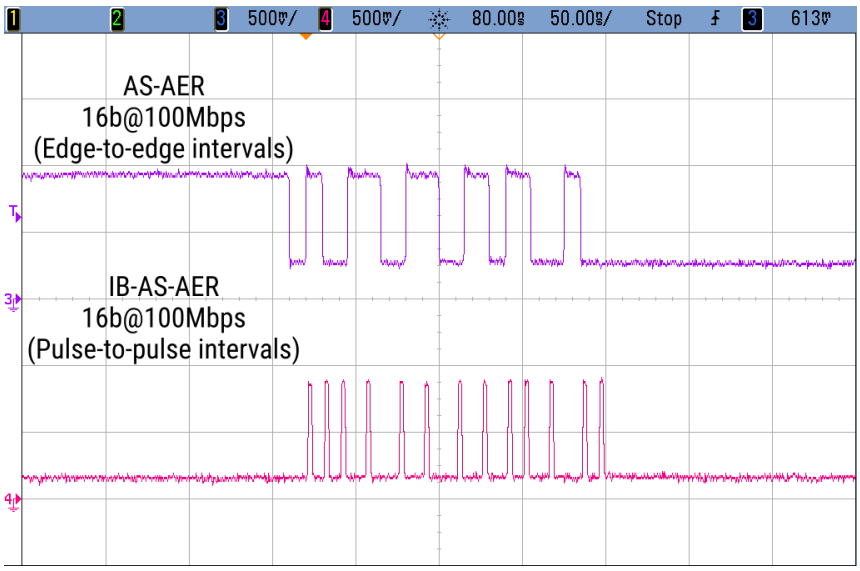


Figure 68- Main signals related to the implemented IB-AS-AER serial protocol operating with 16 bit per event at 100Mbps.

This result relaxes the constraints on the synchronisation of clock sources for transmitter and receiver, as opposed to those solutions requiring a clock precision of the order of 100 ppm (e.g., the standard/common Ethernet applications). The developed reference implementation runs at a raw bit rate of 100 Mbps, leading to a maximum event transfer rate of 2.9 Meps for events of 32 bits. Furthermore, since the serial data have been transmitted by using an optical communication link based on the optical fiber this technical solution highly enhances the system electromagnetic compatibility and signal integrity, reducing interferences and disturbs. At the same time, decreases the power consumption and allows for high data rate transmissions.

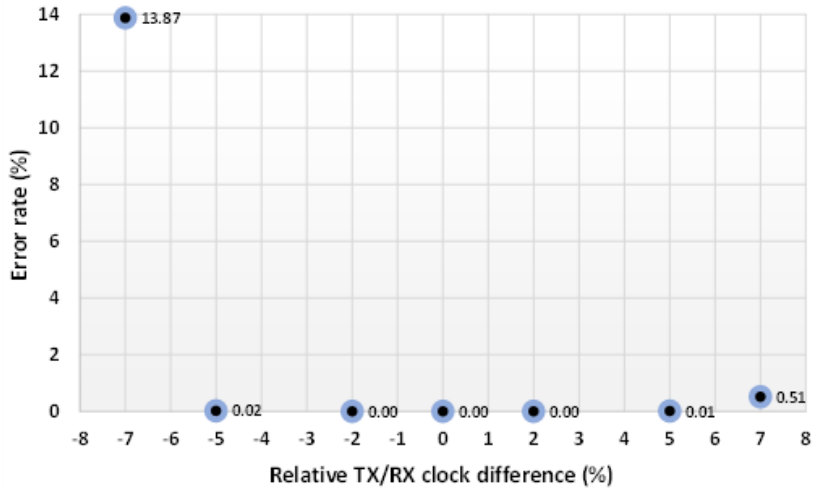


Figure 69 - Error rate as a function of the relative difference between TX and RX clocks.

3.2. Tactile sensory feedback system based on UWB optical link for prosthetics

In Figure 70 it is shown the implementation of the optical communication link, based on optical fiber, for sensory feedback in prosthetic devices. The system consists of an array of tactile sensors placed on the palm of the prosthesis hand. The generated tactile sensor signals are first ADC converted and after digitally processed and optically transmitted by the optoelectronic circuitry present inside the green rectangle. Once received and processed, the transmitted signals are used to activate an electro-cutaneous stimulator in contact with the arm of the patient to restore the sense of touch obtained through the tactile sensors. It worth noting that this represents a first, simple example of application of the optical communication link where the number of data to be transmitted is not so large.

The strategic utility of an optical communication architecture is, also for this specific application and above, more evident if the number and type of the sensors (i.e., temperature, humidity, shape, roughness, etc. sensors) located in the prosthesis increases, the prosthesis from passive becomes active with the use of a number of electrical motors that must be activated to simulate a real human hand. In this case, the very large bandwidth of the employed optoelectronics devices will be able to transport all the signals within a single optical communication link.

Referring to Figure 70, the contribution of this thesis to this project is related to the realization of the transmitter (TX) and receiver (RX) modules, as well as of the optical link. For what concerns the realization of the TX and RX modules, the adopted solution

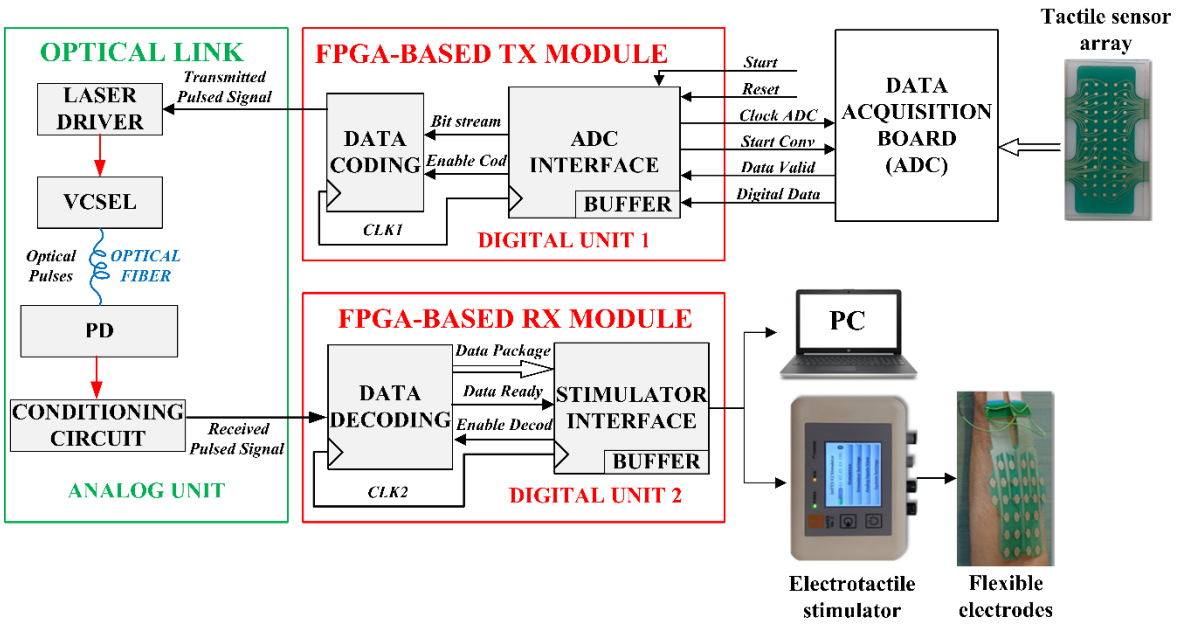


Figure 70 - Overall implementation scheme of a data communication system for prosthetic devices.

employs two different FPGA boards (i.e., Spartan6 and Virtex6 boards by Xilinx). The optical communication link is provided by a VCSEL (OPV314AT by TT Electronics), a Si photodiode (DET025AFC/M by Thorlabs) and a 50/125 µm multi-mode optical fiber. Both the laser beam and the photodiode are directly coupled with the optical fiber by using two lenses with the appropriate numerical apertures to minimize the optical power losses. The photodiode is interfaced with the conditioning circuit shown in Figure 71, based on a TIA, that converts the sequence of the photo-generated current pulses into a sequence of voltage pulses to be decoded by the receiver. Considering the required gain and bandwidth of the photodiode conditional circuit, the TIA uses a cascade of two wideband ERA-2SM+ integrated circuit and reaches a S_{21} of about 30 db as shown in Figure 72.

Referring to Figure 70, after the Start signal has been set to the logic state equal to {1}, the ADC INTERFACE block is enabled to generate a proper Clock ADC signal to retrieve the data from an external data acquisition module (realized by COSMIC Lab of the University of Genova) operating at few kS/s conversion rate (i.e., 2kS/s by employing a DDC232 20bit 32channels ADC by Texas Instruments). Every time the TX MODULE toggles the signal Start Conv, the external ADC simultaneously scans and convert the analogue signals generated by the array of tactile sensors. The converted signals are processed and shifted out to the acquisition module through a serial interface/protocol. Thus, when the

Figure 71 - PD and conditioning circuit.

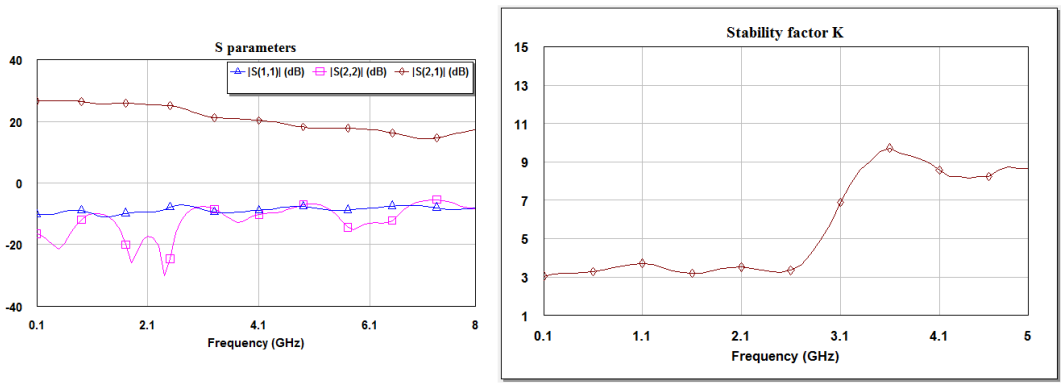


Figure 72 - S parameters and stability factor K of the photodiode conditioning circuit.

acquisition and the conversion are accomplished, the Data Valid pin of the ADC goes low indicating that the data are ready to be stored in the internal global data buffer. Starting from the acquired data, the ADC INTERFACE block generates the serial data package to be transmitted. In this way, according to Figure 73, the serial data package consists of a well-ordered sequence of samples (each one corresponding to the related tactile sensor of the input array) and a header used to detect the beginning of the package.

Subsequently, the serial Data Package is transmitted at a data rate of 100 Mbps using the coding circuits and the architecture solutions described in the previously Chapters. In order to improve the latency of the decoding block, the PLL has been removed for this application.

Once the package is regenerated by the DATA DECODING block, the data can be stored into the global data BUFFER, suitably processed and sent to a stimulator and/or to a PC monitor through a standard Universal Asynchronous Receiver-Transmitter (UART) communication protocol implemented by the UART INTERFACE block or simply evaluated by an oscilloscope. In particular, the data are processed to provide proper control commands to the stimulator device together with the generation of stimuli corresponding to the touch detected by the input tactile sensors.

The control commands carry out all the parameters related to the stimulations to be generated such as the electrostimulation pulse intensity, the frequency and the electrode channel position. These parameters can change according to the type and the force intensity of the touch of the sensing elements (i.e., their physical stimulation). Once the data BUFFER is empty, another Data Package can be acquired, stored and processed. In Figure 74 is reported an example of the measurements performed by employing the implemented system demonstrating that the receiver is able to perform the data and the

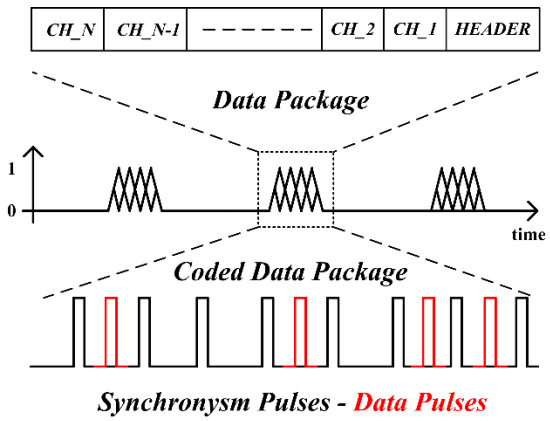


Figure 73 – Structure/composition of the serial data package.

Clock recovery starting from the Received Pulsed Signal. The detection of the package through a HEADER identifies the beginning of the transmitted data acquired from the array of sensors.

In the Figure 75 it is possible to observe how a package is transmitted only if at least an event is detected by the sensors, and the data transmitted is related only to the sensors that has been touched.

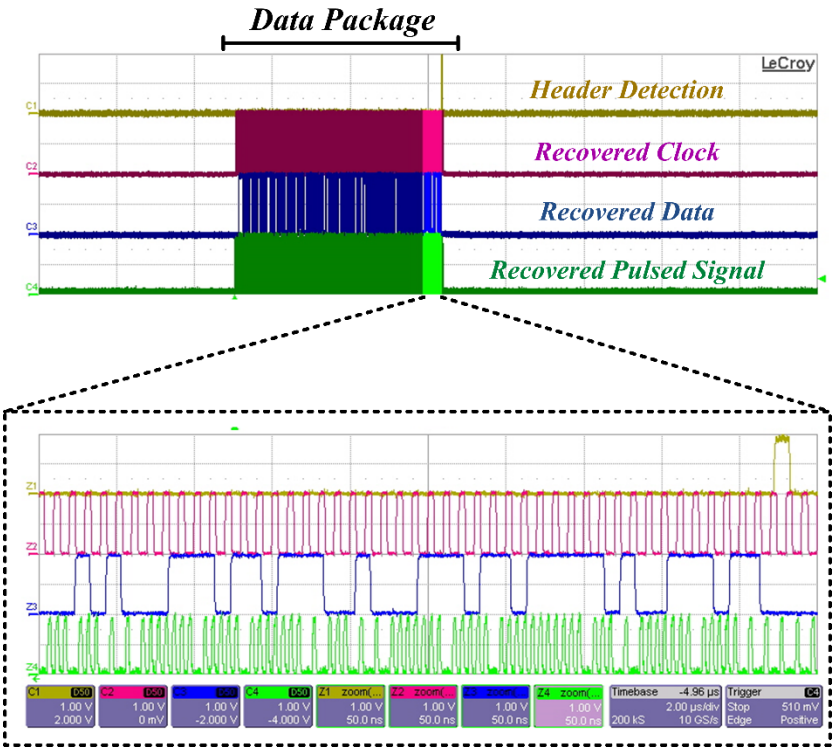


Figure 74 - Experimental measurement: main signals related to the receiver.

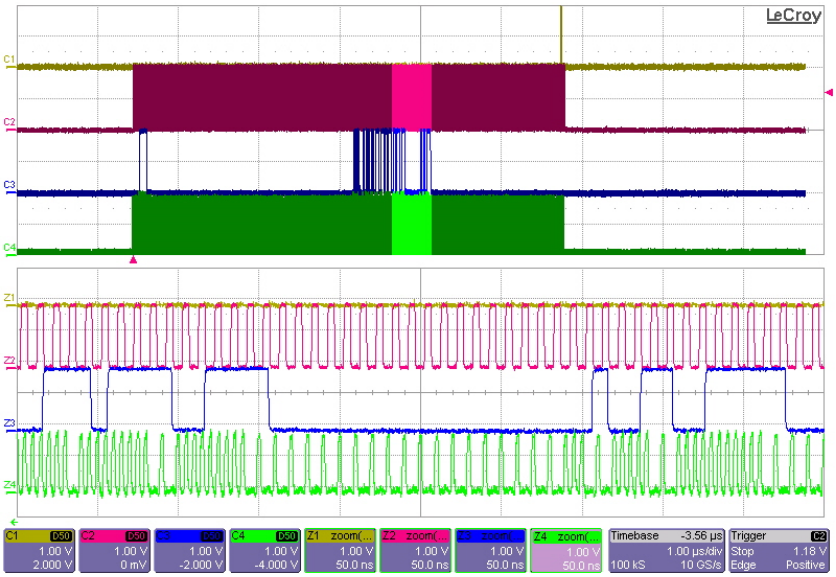


Figure 75 - Experimental measurement: main signals related to the receiver, events detected only by few sensors.

In order to observe in real time the sensors touched displayed on a PC monitor, a GUI in Figure 76 was created by Cosmic Lab using Labview. The GUI is connected to the FPGA using an UART connection with a baud rate of 230400 bps.

A summary of the main overall system specifications, performances and characteristics is reported in Table 6. The achieved results show the correct functionality of the developed system and validate the improvements achieved in the transmission data rate and in the power consumption. These results enable the described solution to be suitably employed with tactile sensor arrays having a higher number of sensors, sampled at higher data sampling rates, that require the transmission of significant amount of data.

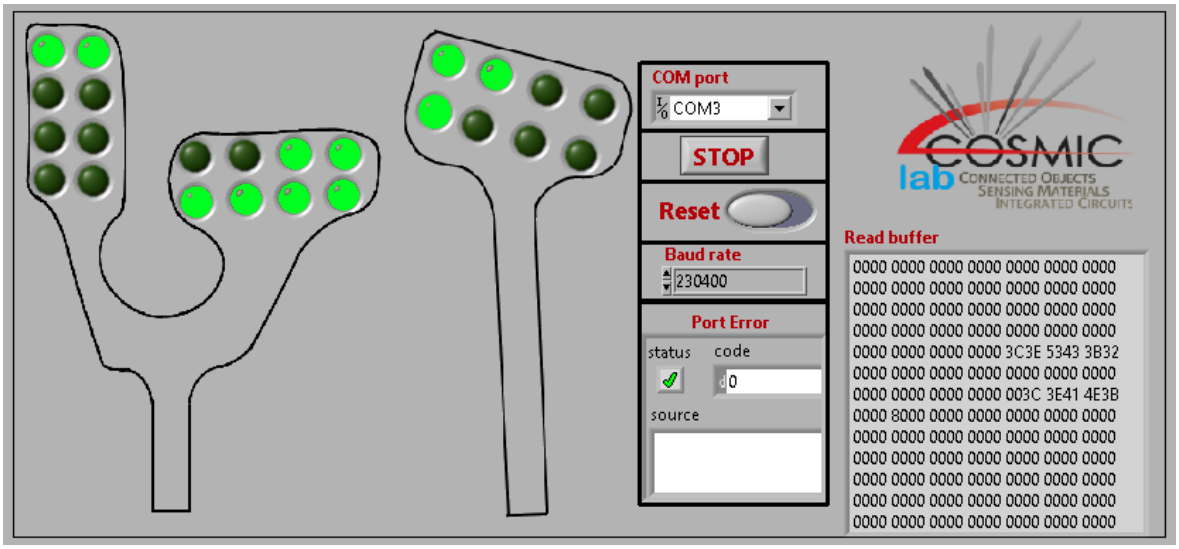


Figure 76 - GUI for graphical data representation.

Table 6 -Developed tactile sensory feedback system: main specifications, performances and characteristics.

Emulated number of tactile sensors	32
Sensor data sampling rate	2 kHz
Optical transmission data rate	100 Mbps
Optical link power consumption	5 mW
Transmission power efficiency	50 pJ/bit
FPGA LUTs for the Tx + Rx	1422 + 1323
FPGA FFs for the Tx + Rx	2230 + 2865

4. IMPROVED SOLUTION FOR WIRELESS OPTICAL DATA LINKS

In this Paragraph it is reported an optoelectronic architecture capable to sum in-phase fast current pulses generated by an array of Si photodiodes with the aim to increase the total effective sensitive area by maintaining the response time and bandwidth unaltered with respect to that one of each single photodiode.

Nowadays, in many demanding applications, optical sensors are gaining importance as probing devices through the use of PD that generate photocurrents proportional to the light intensity impinging on their sensitive area [39]. In particular, for real-time monitoring in industrial and robotic applications, large bandwidth PD are used for time detection of short and ultrashort laser pulses (i.e., pulse duration from one nanosecond down to tens of picoseconds) [40] [41] [42]. This is the case, for example, of the control of chemical and biological reactions and drug delivery achieved by using time resolved optical methods based on the measurement of the light transmittance reflectance and fluorescence [43] [44] [45]. In particular, in the field of new medical systems such as the brain machine interfaces, transcutaneous optical biotelemetry links are obtained by employing semiconductor pulsed lasers and fast Si PDs used in the transmitters and receivers, respectively. These systems are designed to control and actuate external prosthetic devices and need data transfer at high bitrate with a reduced power consumption of the electronic drivers and conditioning circuits [46] [47] [48] [49]. In particular, a VCSEL generates sub-nanosecond pulses in the near infrared regions of the electromagnetic spectrum to minimize the skin/tissue scattering and absorption. The laser pulses are detected by Si PDs with response times of few tens of picoseconds that have very low internal capacitance corresponding to a very small sensitive area. These PD characteristics represent a significant drawback for the optical wireless biotelemetry systems that suffer of optical misalignment between the VCSEL and the PD mainly due to the small generated photocurrent [46] [47] [48] [49]. Since for 50 ps rise time PD have a diameter of the sensitive area equal to about 250 μm [50]. the optical transmitter-to-receiver misalignments less than 125 μm cause a great decrease of the transmitted light intensity through the skin with the subsequent loss of data in the optical telemetric links. In this regards an optoelectronic architecture able to overcome the problem of optical misalignments between the transmitter and the receiver is presented. The designed solution considers an array of fast Si PD with the electronic circuitry designed to sum the pulsed currents generated by each PD through a Kirchhoff node. The resulting single current pulse is amplified by using a transimpedance amplifier. Numerical simulations are performed

with the aim to study the maximum number of PD that can be employed to form an array able to maintain the bandwidth and the rise and fall times of the single PD. The simulations have been performed by using the characteristics of four commercially available fast Si PD starting from the condition that the overall optoelectronic system must provide the condition of low-voltage, low-current operation that is mandatory for the implanted medical systems. Based on the simulation results, a PCB prototype has been implemented including an array of four fast Si PD and the conditioning circuitry employing commercial components in order to characterize the apparatus so validating the optoelectronic architecture. In order to perform the measurements, a laser pulses with a duration at Full-Width-at-Half-Maximum (FWHM) of 800 ps (i.e., the pulse width) operating at 200 MHz repetition rate and a fast Si PD has been used. The measured system total power consumption was found to be less than 100 mW.

4.1. System Design, Analysis and Simulations

The study of the possible electric possible schemes of the array of photodiodes must satisfy both the conditions to add in phase the photocurrents generated by each photodiode and to maintaining unaltered its frequency bandwidth. For biotelemetry applications, the laser pulses have a wavelength falling in the near infrared region of the electromagnetic spectrum. This means that the photon energy is higher than the Si energy gap. For this reason, Si photodiodes are the most common devices used to convert light intensity impinging on their sensitive in electrical current. Moreover, these photodiodes are fully compatible to be integrated in the Si CMOS technology. The simplified equivalent circuit of a Si photodiode is reported in panel a) of Figure 77. Essentially, the photodiode is an ideal current generator in parallel with its internal capacitance C_J and the shunt resistance R_{SH} and in series with the series resistance R_S, where R_L is the load resistance and C_L is the load capacitance.

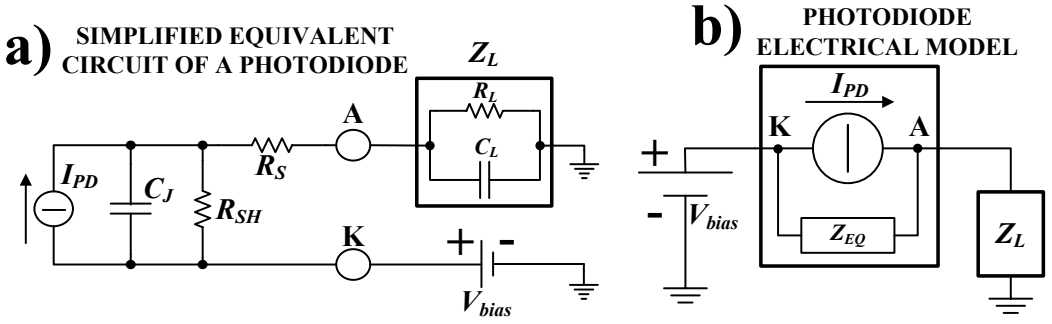


Figure 77 - Panel a): Equivalent circuit of a photodiode where CJ, RSH and RS are the internal capacitance, the shunt resistance and the series resistance, respectively. Panel b): electrical current model of a photodiode where ZEQ and ZL are the equivalent and ex.

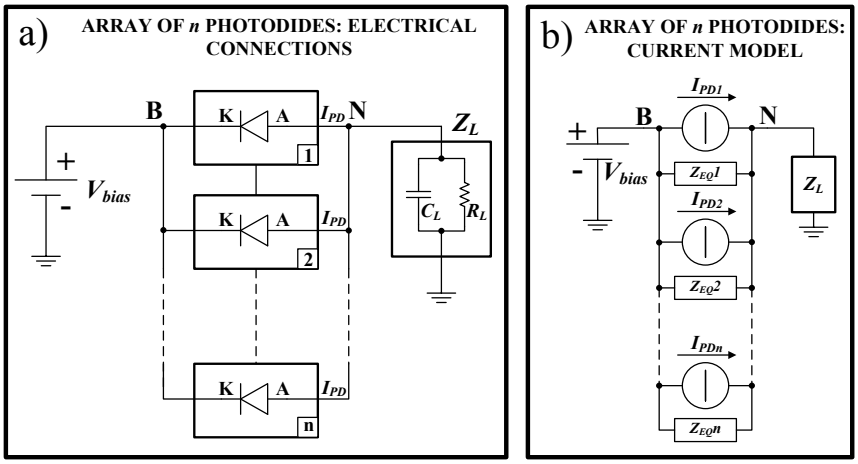


Figure 78 - Panel a): the electric scheme chosen to add the currents IPD generated by N different PD in the Kirchhoff node N: K and A are the PD cathode and anode, respectively; RL are the load resistors. Panel b): the current model of an array of n-photodiodes.

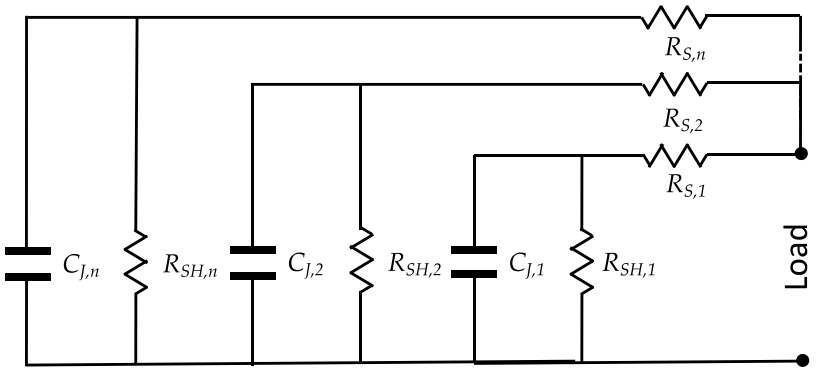


Figure 79 - The equivalent circuit of the array of n PD as seen from the load terminals.

In the following, we calculate the resulting circuit impedance of array of n photodiodes (PDs) with their anodes connected to a Kirchhoff node. The schematic of the electrical connections of the array of n PDs is shown in panel a) of Figure 78.

The equivalent PD array impedance must be calculated respect to the load terminals. Under this condition, the equivalent PD array circuit is shown in Figure 79.

Referring to this Figure 79, first of all, we calculate the resulting impedance Z_1 of the first PD that results equal to:

$$\frac{1}{Z_p} = \frac{1}{R_{SH}} + j\omega C_j \;\rightarrow\; Z_p = \frac{R_{SH}}{1 + j\omega R_{SH} C_j} \;\rightarrow\; Z_1 = \frac{R_{SH} + R_S\left(1 + j\omega R_{SH} C_j\right)}{1 + j\omega R_{SH} C_j} \qquad (1)$$

Assuming the PDs forming the array have the same electrical characteristics, the total impedance of the *n* PDs is simply the inverse of the parallel of *n* impedance all equal to Z_1. Thus, we get:

$$\frac{1}{Z_{TOT}} = \frac{n}{Z_1} = \frac{n\left(1 + j\omega R_{SH} C_j\right)}{R_{SH} + R_S\left(1 + j\omega R_{SH} C_j\right)} \;\rightarrow\; Z_{TOT}(\omega) = \frac{R_{SH} + R_S\left(1 + j\omega R_{SH} C_j\right)}{n\left(1 + j\omega R_{SH} C_j\right)} \qquad (2)$$

If the angular frequency ω goes toward zero (i.e. the DC condition), the capacitances become open circuits and the resulting total impedance is a real quantity equal to:

$$Z_{TOT}(\omega \to 0) = \frac{R_{SH} + R_S}{n} \tag{3}$$

On the other hand, for the angular frequency ω going to infinity (ω→∞), from eq. (2) the resulting impedance has a not defined value. To find the value of Z_{TOT}(ω→∞) we must apply the Hôpital theorem. Calling the numerator and the denominator of eq. (2) as *Num*(Z_{TOT}) and *Den*(Z_{TOT}), respectively, we have:

$$\frac{\partial[Num(Z_{TOT})]}{\partial\omega} = jR_S R_{SH} C_j \quad ; \quad \frac{\partial[Dem(Z_{TOT})]}{\partial\omega} = njR_{SH} C_j$$

The ratio of these two results returns the value of Z_{TOT} for ω→∞. We have:

$$Z_{TOT}(\omega \to \infty) = \frac{jR_S R_{SH} C_j}{njR_{SH} C_j} = \frac{R_S}{n} \tag{4}$$

This result agrees with the fact that when ω→∞, the capacitance of the equivalent circuit of the PD array of Figure 79 becomes short circuits and this condition rules out the presence of all the resistances R_{SH}.

The dependence of the impedance Z_{TOT}(ω) for *n*=5 PD as a function of the frequency $\nu = \omega/2\pi$ of the current generated by the array is reported in the Figure 80. In this Figure is also reported with the red line the behaviour of the impedance of a capacitance equal to $5C_j$ (i.e. $Z(C_j) = 1/(5j\omega C_j)$).

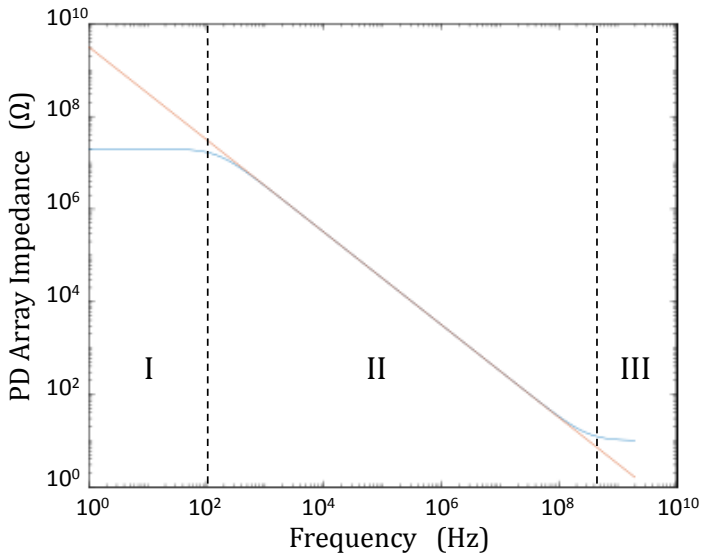


Figure 80 - The behaviour of the total impedance respect to the load terminals as a function of the frequency of the current generated by an array of n=5 PD. Refer to the text for the description of the three regions indicated in the plot.

In Figure 80 are indicated three regions related to the main component that drives the value of the total PD array impedance. In region I the total impedance is controlled by $Z_{TOT}(\omega \rightarrow 0)$ (see eq. (3)); region II is characterised by a pure capacitance impedance $1/j\omega nC_j$ as shown by the red line; in region III the total impedance is governed by $Z_{TOT}(\omega \rightarrow \infty)$, (see eq. (4)).

From the above discussed results, the total impedance Z_{TOT} of eq. (2) suggests that the equivalent circuit of an array of n PDs in the electrical configuration of Figure 78, is the simple circuit reported in Figure 81. For any value of n, in fact, the total impedance of this circuit respect to the load is expressed by the eq. (2).

Numerical simulations were performed by using Cadence Virtuoso Platform with the aim to evaluate how Z_{TOT} influences those two parameters.

Referring to Figure 78, the study of the overall output current from the node N as a function of the number of PD has been conducted by setting: 1) R_S = 50 Ω and R_{SH} = 100 MΩ (i.e., the standard/reference average values for Si PDs); 2) V_{bias} = 3.3 V, C_L = 0.05 pF and R_L = 50 Ω (i.e., the typical values employed to evaluate the effective PD rise and fall times); 3) a current pulse generated by each PD I_{PD} = 10 μA (peak value) with a pulse width (i.e., the duration at FWHM) of 800 ps and a pulse repetition rate of 200 MHz that are the typical operating values for pulsed VCSEL used in optical wireless biotelemetry applications. Moreover, the PD junction capacitance C_J has been changed considering four different models of PDs by Thorlabs having the following main parameters: 1) FDS015 with C_J = 0.65 pF and sensitive area 0.018 mm^2; 2) FDS025 with C_J = 0.94 pF and sensitive area 0.049 mm^2; 3) FGA01 with C_J = 2 pF and sensitive area 0.011 mm^2; 4) FDS010 with C_J = 6 pF and sensitive area 0.8 mm^2. Referring to the operating conditions reported above, Figure 82 reports two examples of the time-domain output currents summed at the Kirchhoff node N of Figure 78, as a function of the number of PDs connected in parallel, for the FDS015 PD (Figure 82a) and for the FDS010 PD (Figure 82b). The results and data achieved from the simulations are summarized in Table 7. More

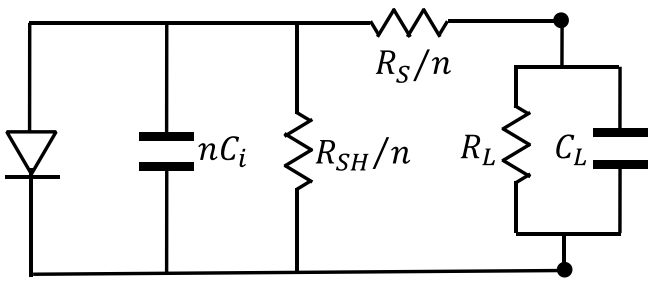


Figure 81 - The equivalent circuit of an array of n PDs connected.

in detail, for each chosen PD, the percentage variations, with respect to their nominal values, of the output peak currents ΔI_{PD} and pulse width ΔFWHM increase as a function of the number of the PD connected in parallel and of their junction capacitance values. For a number of connected PDs greater than that one for which the values of ΔI_{PD} and ΔFWHM (for each chosen kind of PD) in Table I are reported in bold, the overall output peak current I_{PD} and the related pulse width strongly deviate from the nominal values. For example, referring to the results achieved for the FDS025 PD (C_J = 0.94 pF), the values of the output peak current increase almost linearly from 10 μA for a single PD to about 38.9 μA (i.e., ΔI_{PD} = –2.75 %) for 4 PD connected to the Kirchhoff node N. For a greater number of connected PD, the output peak current strongly deviates from linearity reaching a value of about 102.6 μA (i.e., ΔI_{PD} = –35.88 %) for 16 connected PD respect to the nominal value of 160 μA. In addition, also the FWHM of the current pulses remains almost constant up to 4 PDs (i.e., ΔFWHM ≤ +1.18 %) and highly increases reaching a value of about 1.05 ns for 16 PDs (i.e., ΔFWHM = +31.80 %). Resuming, from the results of Figure 82 and Table 7, it is possible to evaluate and extract the maximum number of PDs that can be connected in parallel to maintain unaltered, as much as possible, the effective bandwidth, peak current and pulse width of the single PD for each kind of the considered PD (i.e., for each different value of C_J). In this sense, considering an acceptable maximum deviation of the current peak (ΔI_{PD}) and the pulse width (ΔFWHM) lower than 10 %, in Table I it is highlighted in bold the best values (i.e., the best PD configurations) for each kind of the chosen commercial PD having specific C_J's and sensitive area values. Furthermore, the results of Table I cannot be obtained by simply using single PDs with larger sensitive areas. More specifically, for example, referring to the results achieved with the FDS015 PD, a single PD with 9 times larger sensitive area would have 9 times bigger C_J. Remembering that the C_J is inversely proportional to the square root of V_{bias} [51], in order to maintain unaltered the PD response time and bandwidth it is necessary to increase V_{bias} = 3.3 V up to higher values that could be incompatible for biomedical applications, especially for implanted devices.

These results open the possibility to investigate the possibility to further increase the effective array sensitive area by forming an array of 16 photodiodes by adding four sub-arrays of 2x2 photodiodes as shown in Figure 69.

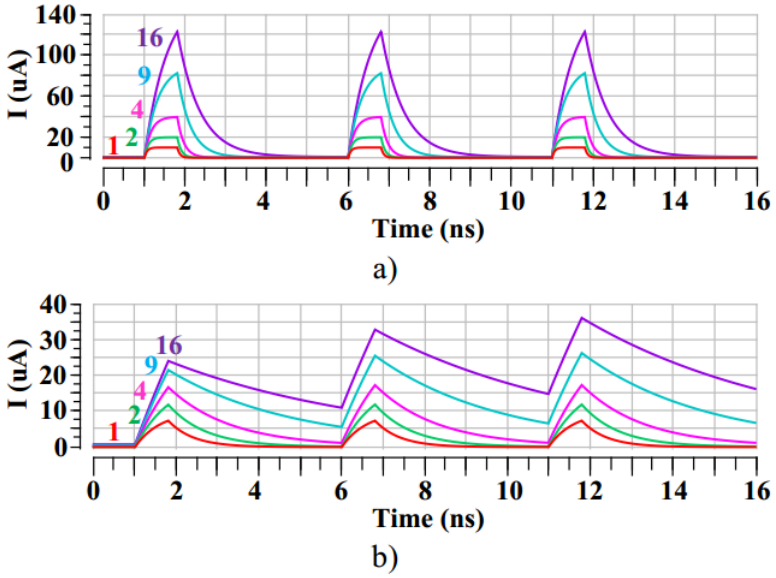


Figure 82 - The output current pulses at the Kirchhoff node N of Figure 1 as a function of the number of the connected PD: a) FDS015 photodiode; b) FDS010 photodiode.

Table 7 - Simulation results for different PD configurations and typologies.

Number of PD in parallel	Nominal pulsed current I_{PD} [µA] (nominal FWHM = 800ps)	PD junction capacitance C_J (reference commercial PD)							
		0.65 pF (FDS015)		0.94 pF (FDS025)		2pF (FGA01)		6pF (FDS010)	
		ΔI_{PD} [%]	$\Delta FWHM$ [%]	ΔI_{PD} [%]	$\Delta FWHM$ [%]	ΔI_{PD} [%]	$\Delta FWHM$ [%]	ΔI_{PD} [%]	$\Delta FWHM$ [%]
1 PD	10	-0.10	+0.12	-0.10	+0.19	-1.30	+0.68	**-25.60**	**+18.07**
2 PDs (2x1 array)	20	-0.15	+0.25	-0.15	+0.25	**-6.35**	**+2.80**	-40.15	+39.19
4 PDs (2x2 array)	40	-0.20	+0.31	**-2.75**	**+1.18**	-19.48	+11.93	-59.55	+91.80
9 PDs (3x3 array)	90	**-7.90**	**+3.66**	-17.53	+10.25	*n.a.*	*n.a.*	*n.a.*	*n.a.*
16 PDs (4x4 array)	160	-22.81	+15.16	-35.88	+31.80	*n.a.*	*n.a.*	*n.a.*	*n.a.*

In order to maintain unaltered the temporal behavior of each sub-array (see the results of Figure 82 above discussed), the output current pulses of the four sub-arrays are suitably decoupled by employing four current buffers before to be added in the Kirchhoff node M as reported in Figure 83a. This avoid to obtain the total output current pulse amplitude and width would result equal to those ones of the 16 photodiodes shown in Figure 82 and Table 7. The output current pulse from node M is amplified by using a TIA. The schematic of the current buffer is reported in Figure 84. This current buffer consists of an architecture based on a self-biased double current mirroring provided by the M1 and M3 transistors that, in addition, allow for a low-impedance input node equal at 186 Ω. The stage composed by the M2 and M4 transistors drains the current I_{INT} from the stage composed by the M5 and M7 transistors. Finally, the M6 and M8 transistors guarantee an impedance output node equal to 3.71 kΩ. The current buffer has been designed in AMS 0.35µm standard CMOS technology and it is able to produce a slew rate equal to 480 µA/ns and a GBW of 3.6 GHz with an average power consumption lower than 20 mW at a current pulse repetition rate of 200 MHz by employing a power supply voltage equal to 3.3V.

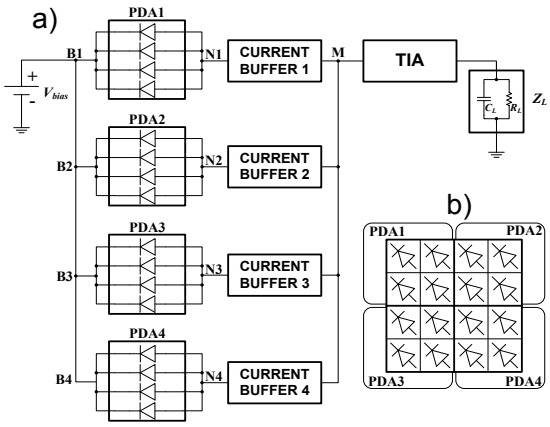


Figure 83 - Panel a): the block scheme for the connection of the 4 sub-arrays PDA1, PDA2, PDA3, PDA4. The current pulse generated by each one of the subarrays is buffered before to be added at the Kirchhoff node M and amplified by a TIA. Panel b): the final array.

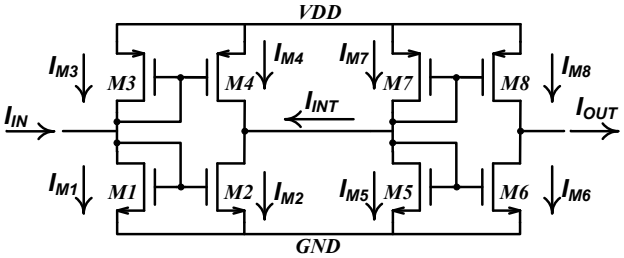


Figure 84 - The schematic of the current buffer employed in Figure 83 designed in the AMS 0.35µm standard CMOS technology.

Table 8 - a) Elements that composing the schematic of the current buffer in Figure 84 and b) Electronics characteristics of the designed current buffer resulting from post layout simulations.

a) Elements of the current buffer		**b) Characteristics of the current buffer**	
MOS	***W(µm) / L(µm)***	***VDD***	*3.3 V*
M1,M3,M6,M8	*20 / 0,35*	***AVERAGE POWER CONSUMPTION***	*19,68 mW*
M2,M4	*30 / 0,35*	R_{IN}	*186 Ω*
M5,M7	*10 / 0,35*	R_{OUT}	*3.71 kΩ*
		SLEW RATE +	*480 µA/ns*
		SLEW RATE -	*476 µA/ns*
		GBW	*3.6 GHz*

More in details, the relationship between the input and output current pulses can be described as:

$$I_{OUT} \cong I_{IN} \frac{g_{m2}}{g_{m1}} \frac{g_{m6}}{g_{m5}} = \alpha I_{IN}$$

Where α is the total gain of the current buffer and g_{mn} the gain of a generic transistor M_n of the schematic shown in Figure 84. Table 8 summarizes the values of the parameters of the elements used for the realization of the current buffer. Note that each element was

provided by the AMS 0.35 µm technology library. In particular, Table 8-b shows the electronic characteristics of the current buffer obtained after the post layout simulations.

The resulting values of the current pulses at the output node M of Figure 83a is amplified by a TIA whose schematic is shown in Figure 85. The TIA is composed by an input differential pair combined with a source-follower stage followed by a cascaded of three CMOS inverter stages. The inverter stages are able to amplify the output pulses up to 3.3 V in order to make the system suitable for optical digital communications [45]. The sizes of the TIA are present in the Table 9-a. The TIA guarantees a slew rate of 17 V/nS, a GBW of 2.24 GHz and an average power consumption lower than 12 mW with input pulses at a repetition rate of 200 MHz by using a supply voltage of 3.3 V as shown in Table 9-b.

As shown from the post layout simulations reported in Figure 86, the peak input current coming from a sub-array of 2x2 PD is equal to 27 µA with a buffer R_{IN} of 186 Ω and it is lower than 38.83 µA obtained without a buffer with a R_L=50Ω as reported in Table 7.

However, the gain α of the buffer is able to guarantee a peak output current of 40 µA with an offset of 68 µA. In this way, referring to the Figure 83a, it is possible to reach a peak

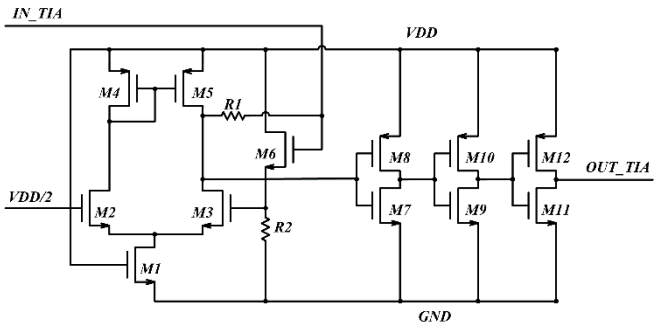


Figure 85 - The schematic of the TIA designed in AMS 0.35µm standard CMOS technology.

Table 9 - a) The sizes of the elements composing the schematic of the TIA shown in Figure 9; b) The electronics characteristics of the TIA resulting from post layout simulations.

a) Elements of the TIA		**b) Characteristics of the TIA**	
MOS	***W(µm) / L(µm)***	**VDD**	3.3 V
M1	*300 / 3.5*	**AVERAGE POWER CONSUMPTION**	11.53 mW
M2, M3	*600 / 0.35*	**SLEW RATE +**	17 V/ns
M4, M5	*15 / 3.5*	**SLEW RATE -**	11 V/ns
M6	*40 / 0.35*	**GBW**	2.24 GHz
M7, M9, M11	*6 / 0.35*		
M8	*21 / 0.35*		
M10	*17 / 0.35*		
M12	*18 / 0.35*		
R1	*550 Ω*		
R2	*710 Ω*		

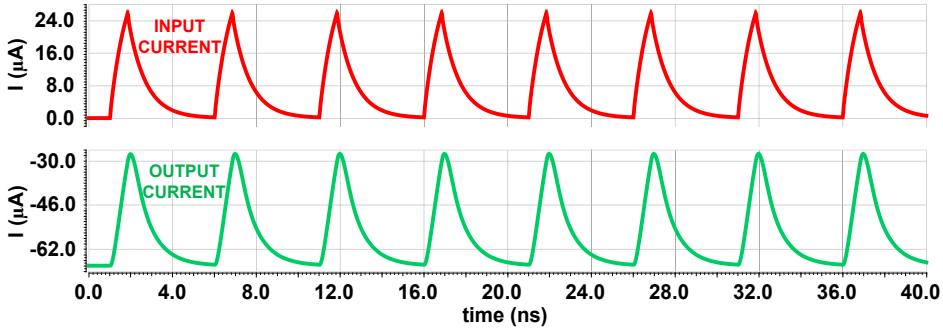


Figure 86 - Output current pulses of the buffer as function of the input current.

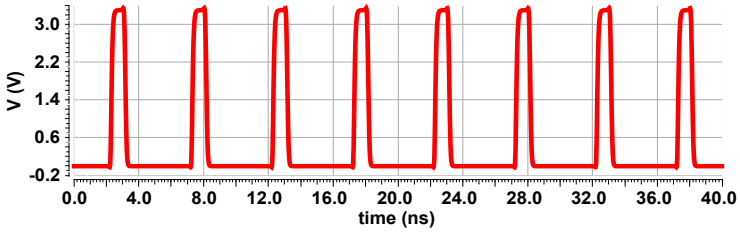


Figure 87 - The voltage pulsed output amplified by the TIA at a repetition rate of 200MHz.

current of 160 µA at the input of the TIA with a current temporal and frequency response equal to those ones of the 16 PD. Figure 87 reports the results of the post layout simulations for the output voltage pulses from TIA under the same initial conditions of Figure 82 for the currents generated by each photodiode sub-array. The temporal and frequency bandwidth remain constant respect to those ones of each photodiode sub-array (i.e., a duration at FWHM of about 800 ps) validating the electronic paradigm used for increasing the effective PD sensitive area by adding the current pulses generated by the 4 sub-arrays.

4.2. System Implementation and Experimental Results

The experimental verification of the developed architecture has been carried out to characterize the properties in bandwidth and temporal response of only a single 2x2 PD array. Commercial off-the-shelf components are used to realize the electronic circuitry. In particular, Si FDS025 PDs by Thorlabs [50], with a rise- and fall-time equal to 47 and 246 ps respectively, have been employed. A quasi-DC characterization has been firstly performed by using the optical configuration shown in the inset of Figure 88. The Continuous Wave (CW) HeNe laser passes through a mechanical chopper to generate a train of laser pulses at a frequency of 77 Hz that is employed also as the reference frequency for a Lock-In Amplifier (LIA) operating in current mode for the measurement of the photocurrent generated by the illuminated PD. The results of the generated output current as a function of the number of the illuminated PD of the 2x2 array is shown in

Figure 88. The increase of the photocurrent is a linear function of the number of the illuminated PD with a ratio between the photocurrent generated by a single PD and that one obtained by 4 PD equal to 3.9. This value is in good agreement with the results obtained by the numerical simulations (see Figure 82). The study of the response of a 2x2 PD array at high repetition rate with pulsed signals has been performed by realizing a TIA fabricated by using high-frequency large bandwidth RF components following the schematic reported in Figure 89. The TIA has been designed and implemented on a PCB prototype employing discrete commercial components (i.e., BFG520 NPN 9GHz wideband bipolar transistor by NXP Semiconductors).

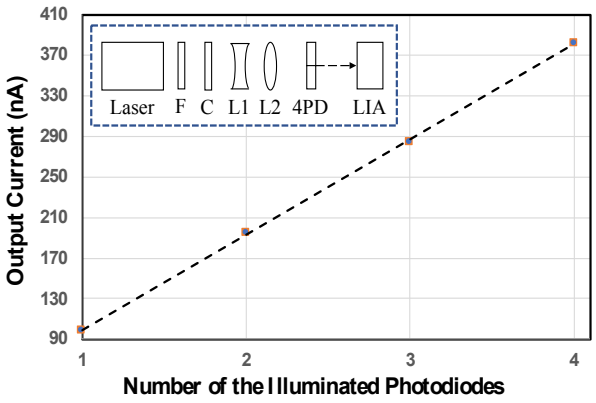


Figure 88 - The output current as a function of the number of the illuminated PD forming the 2x2 array at low frequency rate. In the inset the optical set-up used for the measurements: the laser is a 10 mW output power CW HeNe; F is a neutral density filter to suitably attenuate the laser power; L1 and L2 form a telescopic lens system used to magnify the laser spot for a uniform illumination of all the PD forming the 2x2 array; LIA is the lock-in amplifier.

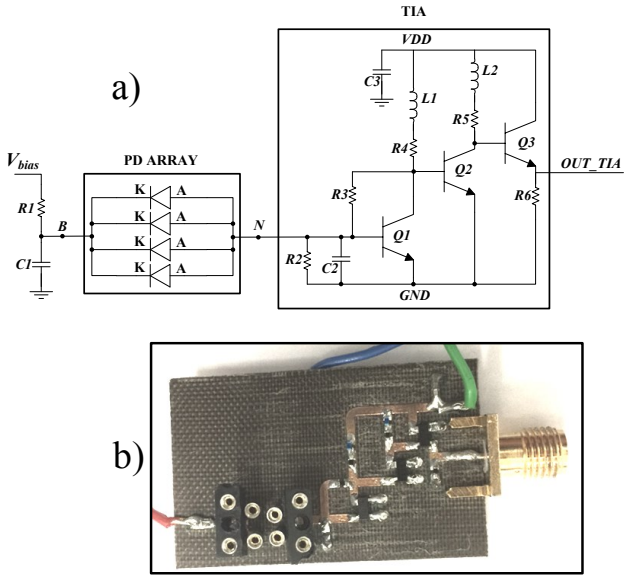


Figure 89 - The TIA schematic realized by using high frequency large bandwidth RF commercial components (a) and its physical realization (b).

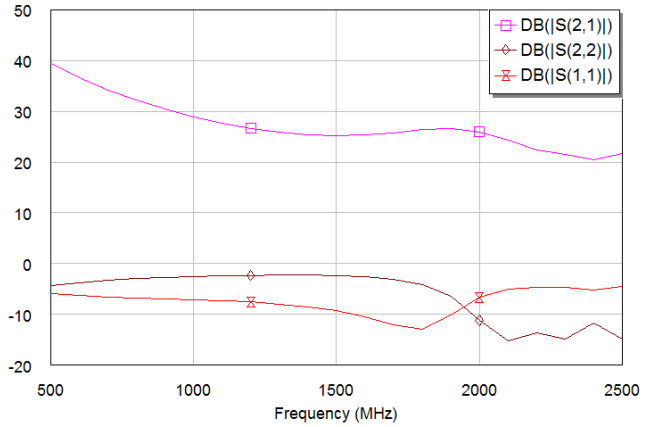


Figure 90 - Evaluation of the S parameters S(2,1), S(2,2) and S(1,1) of the implemented TIA.

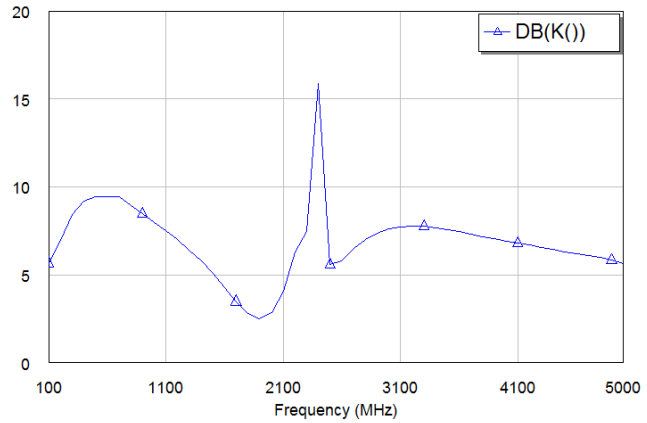


Figure 91 - Stability factor K of the implemented TIA used for the experimental tests.

Referring to the schematic circuit of Figure 89, the input stage is composed by a cascade of two common-emitter configurations (i.e., Q1 and Q2 transistors) followed by a common-collector (Q3) employed as a buffering output stage. Simulations as well as the PCB design on TLX8 substrate were performed using the tool AWR Microwave Office. Figure 90 shows the simulations results indicating a S(2,1) parameter greater than 25 dB in a frequency range from DC to 2 GHz with a good input/output impedance matching. The stability factor K shown in Figure 91 is always high than 1, this ensures the stability of the circuit. By using the implemented TIA to amplify the photocurrents at the exit of the Kirchhoff node M for a single 2x2 PA array (see Figure 83), a series of measurements are performed employing the optical configuration shown in the inset of Figure 92. A VCSEL emitting at λ=850nm is suitably attenuated and magnified for a uniform illumination of the 2x2 PD array. The VCSEL (VCSEL-850 by Thorlabs) is driven by a train of 800 ps current pulses generated by a FPGA board (Xilinx Virtex 6 FPGA) at 200 MHz repetition rate (see Figure 92 panel a). The laser pulses are the optical replica of these current pulses. The TIA amplified output voltage pulses are analyzed by a LeCroy Wavemaster 8600A digital oscilloscope and the results are reported in Figure 92 (panel b) when only one of the four

PD of the 2x2 array is illuminated and (panel c) when the entire 2x2 array is illuminated. The two oscilloscope traces have been recorded using the same voltage sensitivity a choice that makes evident that the ratio between the peak pulses of panel c) and b) is equal to 3.86 in good agreement with both the simulation results of Figure 82 and the quasi-DC measurements of Figure 88. As a final comment, also at 200 MHz repetition rate the resulting output pulse width remains unaltered and equal to about 850 ps. In Figure 93 is shown the experimental results performed at 500 MHz in the same conditions of the previous configuration.

In conclusion, in this Chapter we have presented and experimentally validated a novel optoelectronic architecture capable to sum in-phase fast current pulses generated by an array of four Si photodiodes. The four photocurrents are summed through a Kirchhoff node and the resulting single current pulse is amplified by a transimpedance amplifier. The circuitry is designed to maintain unaltered the rise and fall times as well as the bandwidth of the input pulsed signal with respect to that one coming from each single photodiode. This produces the increase of the total effective sensitive area in comparison with the case of a single photodiode employed in the detection of fast (i.e., sub-nanosecond) laser pulses. As a consequence, the array of photodiodes behaves as a single photodiode producing a current pulse that is 4 time that one of a single photodiode of the array. This result avoids the decrease of the photodiode efficiency due to optical misalignments between the laser and the array of photodiodes that strongly affects the performances of communication systems like transcutaneous wireless optical biotelemetry links. The optoelectronic configuration has been characterized by numerical simulations and the results have been validated also by experiments performed by implementing the circuitry on a PCB prototype with commercial components and using laser pulses of 800 ps at a repetition rate up to 500 MHz. In this sense, it has been demonstrated that the peak value of the obtained current pulses is multiplied by a factor 4, i.e., equal to the number of the photodiodes forming the array.

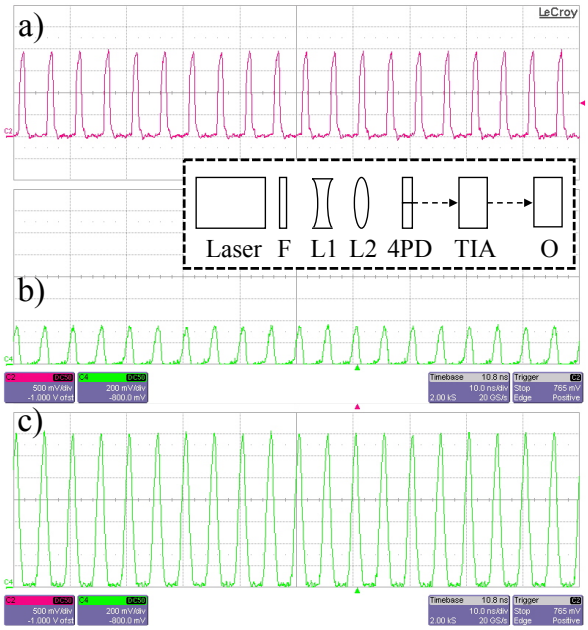


Figure 92 - Panel a): the train of the current pulses generated by the FPGA board at 200 MHz repetition rate that drives the VCSEL; panel b): the pulsed output voltage amplified by the TIA considering a single illuminated PD; panel c): the same as panel b) for 4 illuminated PD of the 2x2 array. In the inset the optical set-up used for the measurements: the laser is a VCSEL generating 800 ps pulses at λ=850 nm; F is a neutral density filter to suitably attenuate the laser power, L1 and L2 are a negative and a positive focal length lens forming a Galilean-type beam expander to magnify the laser beam spot for a uniform illumination of the 2x2 PD array (4PD). The 4PD output pulse current is amplified by TIA and the voltage output pulse are analysed by the LeCroy 8600A digital oscilloscope (O).

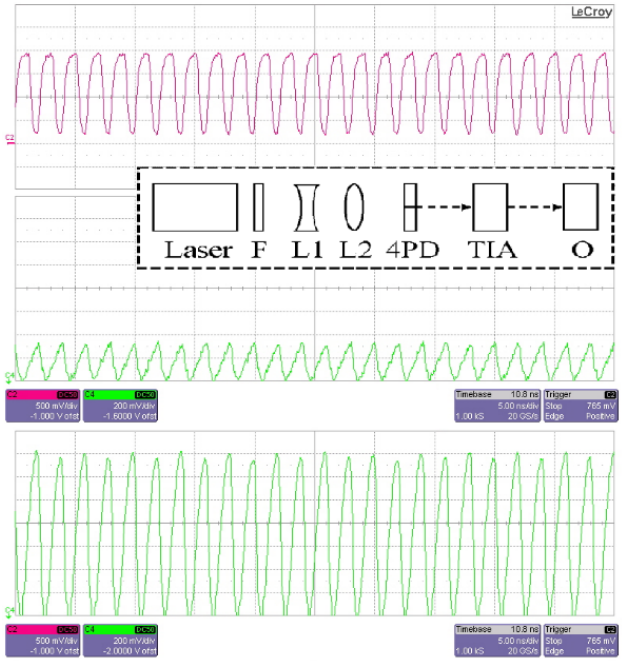


Figure 93 - Experimental results performed at 500MHz in the same conditions of Figure 92.

CONCLUSION

The aim of this Thesis was to introduce the reader to the design and implementation of an UWB optical communication links for biomedical implantable devices and prosthetic applications able to guarantee data transmission rate up to 300 Mbs at low electrical power consumption. Starting from the description of an UWB encoding suitable for the optical transmission by using optoelectronic devices, the thesis reported on the design and the implementation of specific analogue/digital circuitries and data coding and data decoding architectures. All the circuit solutions described have been implemented and developed by using commercial apparatus and components. However, we have demonstrated that the paradigms used for designing the electronic and optoelectronic circuitries allow for a direct integration of all the circuits at transistor level by using standard Si CMOS technologies. In this sense one ASIC devices has been fabricated and a second one, described in appendix, has been designed and analysed. Practical examples of applications have been presented to prove the capability of the optical communication links to be used for the data transmission tactile sensory feedback systems in prosthetic devices, for humanoid-robots or for neural data in implantable biotelemetry systems. The experimental measurements have been presented and discussed for both the solutions (realized with discrete components or integrated in CMOS technology). Moreover, an optoelectronic architecture able to overcome the problem of optical misalignments between the transmitter and the receiver has been presented, such as the design of on-chip PDs. The results indicate that the optical communication links guarantee very high values of electromagnetic compatibility and signal integrity, capabilities to operate in low-voltage low-power regime, transmission data rates up to 300 Mbps, overall power efficiencies of few hundreds of pJ/bit and a BER $< 10^{-10}$. In the end, Analog Front End (AFE) integrated solutions for fluorescence-based pulse oximeter applications are designed and discussed in the Appendix of this Thesis together with further related activities, always concerning biomedical applications.

The achieved system performance is compared to the current state-of-the-art in Table 10. As shown, the present solution achieves the highest bit rate with comparable values of BER, power efficiency and maximum operating distance.

Table 10 State-of-the-art in implantable wireless biotelemetry

Reference	Publication Year	Bitrate [Mbps]	Energy Efficiency [pJ/bit]	BER	Implementation Type	Communication Link Type	Maximum Operating Distance [mm]	Coding Technique
[20]	2019	0.125	50400 (TX)	N.A.	Discrete components	Inductive	50	LSK
[21]	2014	100	21	$< 10^{-7}$	Integrated TX Discrete RX	Optical	2.5	N.R.Z.
[22]	2015	100	290	N.A.	0.35 µm CMOS	Optical	2	N.R.Z.
[23]	2013	135	10	N.A.	0.13µm CMOS	IR-UWB	120	PPM
[24]	2015	67	30	$< 10^{-7}$	Integrated TX Discrete RX	IR-UWB	500	OOK
Solution described in paragraph 2.1	2020	300	37 (estimated)	$< 10^{-10}$	Discrete components	Optical	4.25	S-OOK
Solution described in paragraph 2.2	2019	250	160	$< 10^{-10}$	0.35 µm CMOS	Optical	4	S-OOK

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APPENDIX A: FPGA IMPLEMENTATION OF A TRUE RANDOM NUMBERS GENERATOR

In order to evaluate the BER of the described optical communication system, a TRNG has been implemented. A TRNG can be used in many applications as financial market, bank transactions, avionics communications, and those ones related to the emerging Internet-of-Things (IoT) or Industrial-Internet-of Things (IIoT) where an increasingly high level of network security is needed. In general, the way to accomplish this request is to implement complex software and/or hardware architectures capable to generate sequences of random numbers to providing public and private keys to achieve an effective data cryptography. In this regard, different Pseudo-Random Number Generators (PRNGs) and True-Random Number Generators (TRNGs) paradigms have been designed for the generation of random number sequences to satisfy the randomness characteristics needed for each application. The PRNG solutions are typically developed through specific software codes and called via subroutines [1] even if PRNGs hardware implementations have been also reported with good statistical properties of the generated number sequences [2]. The output of PRNGs is a long periodic and repeatable sequence of numbers approximating the properties of random numbers where each produced number is a function of some of the numbers previously generated. This operation is achieved by using some recursive relations like $X_i = f(x_{i-1}, x_{i-2}, \dots , x_{i-q})$ with $i > q$ and the random properties of the generated number sequence depend on the particular choice of the seed (x1, x2,…, xq). In this regard, the simplest implementation is the use of the Fibonacci generator. Thus, for its particular nature, PRNGs are fast solutions that, however, do not present very high statistical randomness characteristics. For these reasons, these solutions are typically employed for modelling applications and device simulations that make use of the statistical Monte Carlo analysis but are generally inadequate for high level data encryption [3]. On the other hand, TRNGs are based only on hardware architectures and generate random number sequences characterized by an equiprobability in the generation of each symbol (i.e., number, bit, etc.) and the absence of correlation between the last generated symbol and any of the previous ones in order to guarantee the impossibility to determine mathematical and/or statistical connections among the produced symbols. TRNGs are typically realized by using fully-digital circuits, mixed-signal and/or embedded systems with low power consumption and output bit rates suitable for IIoT and Industry 4.0 security and cybersecurity applications [4-10]. For the generation of the random number sequences, TRNGs require an entropic seed that is obtained from physical sources of stochastics noise

intrinsically present in electronic circuits. In this regard, many TRNGs are implemented on Field Programmable Gate Array (FPGA) employing ring oscillators or similar structures as the seed of entropy [11-16]. The FPGA-based TRNGs open the possibility to use a large matrix of Configurable Logic Blocks (CLBs) that can be connected via programmable interconnects so realizing a powerful platform largely used for digital VLSI implementations. In particular, the realization of TRNG architectures requires a large number of Look-Up-Tables (LUTs) with the consequent increase of the system complexity and the overall power consumption. Moreover, the noise source generates a raw bitstream that often needs to be post-processed to improve the randomness properties of the generated numbers. The absence of the post-processing procedure, in fact, does not guarantee the generation of high-quality random number sequences without a further increase of the architectural complexity and/or a reduction of the output bit rate. However, the implementation of the post-processing algorithms requires the use of additional hardware resources and a methodology based on approaches like for example [17]: (i) an XOR reduction operation performed on consecutive generated bits that reduces the output bit rate with the advantage to improve the bias of uncorrelated bits; (ii) a Von Neumann corrector-based comparison performed between a pair of two consecutive generated bits: if the two bits are different, only the first bit is chosen to form the output bitstream while the second one is discarded; if the two bits are the same, the output bitstream is not generated with the disadvantage to produce a no-constant bit rate that must be compensated by using suitable buffer blocks. This appendix reports on the design, realization and characterization of a TRNG architecture implemented on FPGA that employs as seed of entropy both the jitter introduced by a Phase Locked Loop (PLL) and the metastability property of a Flip-Flop (FF). Differently from the use of LUTs, this appendix demonstrates that a reliable TRNG architecture can be obtained by employing only on-board primitives of a Xilinx Ultrascale XCKU040 FPGA. Other few basic logic elements have been utilized only for the initial overall system synchronization and post-processing operation. In this way, this solution largely reduces the required number of CLBs, the architecture complexity and the overall power consumption without affecting the resulting output bit rate. In particular, it is introduced a complete description and theoretical analysis of the main solutions employed as seeds of entropy for the TRNG operation focusing on the jitter and the metastability effects introduced by a PLL and a FF. Moreover, it is presented a detailed comparison of the results achieved by the implemented TRNG with other ones reported in the Literature demonstrating that the architecture employs the smallest number of FPGA hardware resources while providing high output bit rate. Finally, the generated 100Mbps output bit

rate random number sequences pass the National Institute of Standards and Technology (NIST), the Anderson-Darling and the Kolmogorov-Smirnov tests resulting suitable to be employed in security/cybersecurity network systems as well as in IoT and IIoT applications.

I. Analysis of the main seeds of entropy for TRNG implementations

In Figure 1A is shown an ensemble of ring oscillators each one containing an odd number of inverter stages. The outputs of these ring oscillators are used as the input for an XOR operator that returns as output the sum of the jitters introduced by the different employed ring oscillators. Lastly, the XOR output is sampled by a memory element, like an FF, at a frequency fs, thus generating the raw bitstream [19]. In particular, for periodic signals the jitter σ is defined as the time variations (i.e., phase shifts) of a set of transition edges with respect to their ideal values. The different values of the jitter are obtained by ring oscillators, with different lengths, and by different Process-VoltageTemperature (PVT) characteristics of each inverter. However, this kind of solutions implemented on FPGA requires a large number of LUTs with a subsequent increase of the overall system complexity and power consumption. Alternatively, it is possible to consider as the seed of entropy (i.e., the source of randomness) the jitter introduced by a PLL, the RS-Latch uncertainty and/or the metastability property of an FF [20- 23]. In particular, the typical purpose of a PLL block inside an FPGA is to generate a high frequency clock signal starting from an external low-frequency crystal oscillator. The basic scheme of a PLL is shown in Figure 2A. The internal control circuitry continuously adjusts the VCO input so to ensure a specified output frequency and its variation can be considered as a jitter.

An additional noise is also caused by variations of the supply voltage, temperature and/or any further external interferences. More in detail, the input jitter transfer function $H_1(s)$ and the loop oscillator jitter transfer function $H_2(s)$ of a PLL can be expressed as a low-pass and a high-pass filters, respectively. In other words, referring to Figure 2A, the main source

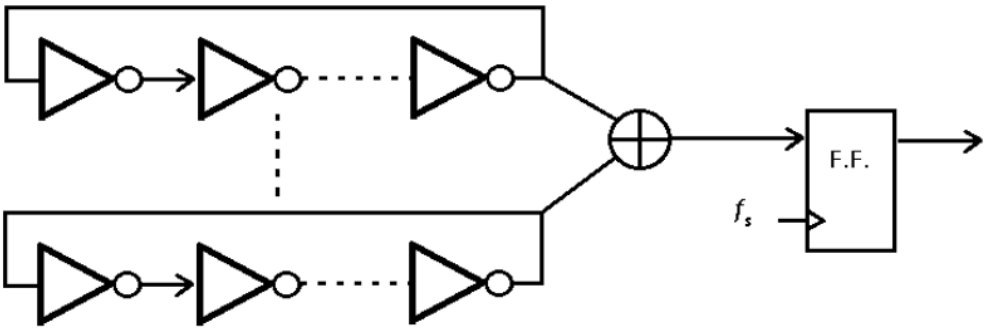

Figure 1A - The sum of jitters coming from ring oscillators achieved through an XOR digital logic gate.

of jitter in a PLL is the VCO block. Therefore, in order to maximize the jitter introduced by a PLL when used as seed of entropy for a TRNG, the jittered signal must be sampled by a clock with suitable values of the phase and frequency parameters [21]. Finally, another important seed of entropy is the metastability introduced by an FF. In general, for a correct data generation and acquisition it is necessary to ensure the Setup time S and the Hold time H of the FF elemental memory cell in which the data must be stored. The S time is defined as the minimum amount of time where the data must be stable before the clock active edge so to be correctly latched. On the contrary, the H time is defined as the minimum amount of time after the clock active edge during which data must be stable. Any violation of these time constraints may cause incorrect data acquisition and the memory cell can fall in a metastable state so that the output data is no predictable. This happens, for instance, when a signal is sampled during its transition edge.

The probability that the output is equal to one can be expressed as follows:

$$P\{Q = 1\} = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} \exp\left(\frac{-u^2}{2}\right) du$$

where x is related to the S/H time window and the difference between the edges of the data and the input clock. Figure 3A shows that there is a deterministic output of the FF (P(Q=1) = 1 or 0) only if the input data signal is delayed by a value greater than H or if it is anticipated by a value greater than S with respect to the rising edge of the clock signal. More in detail, in order to show and demonstrate how the S/H time violations can bring a D-type FF in a metastability state, the performance of this basic memory cell has been analyzed in Cadence Virtuoso environment by performing post-layout simulations of the circuit designed at transistor level in AMS 0.35µm standard CMOS technology whose implemented schematic and layout are shown in Figure 4A. In particular, in order to reach and provide the metastability state of an FF, the S/H time violation is achieved through a fine phase-shift regulation between the FF input signals D and CLK. The sizes of the

transistors are (expressed in terms of W[µm] / L[µm]): Q1 and Q2 = 30/0.35; Q3 and Q11 = 6/0.35; Q4, Q7, and Q10 = 15/0.35; Q5, Q6, Q8 and Q9 = 12/0.35.

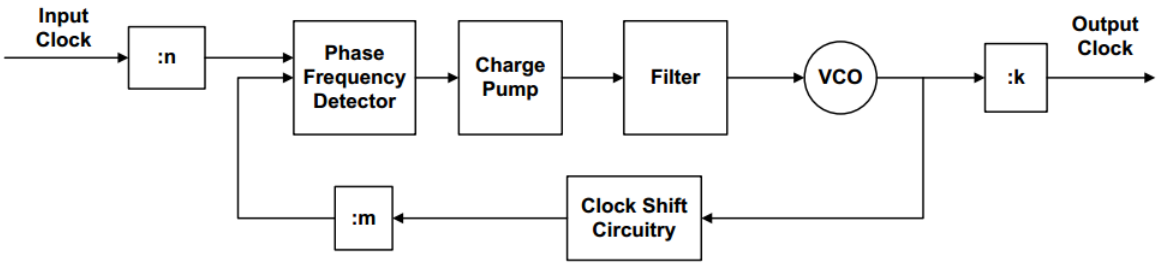

Figure 2A - The block scheme of a generic PLL.

In this regard, a replica of the 250 MHz input clock is used as the FF input D having a relative delay time of about a half period (i.e., 2ns corresponding to the phase opposition between the clock and data signals). In this operating condition, the rising edge of the clock signal is just after the falling edge of the input data and, according to the post-layout simulation results shown in Figure 5A, in static condition the output cannot reach the maximum voltage level (i.e., Vdd = 3.3V) as the results reported in [24]. Consequently, any variation of the supply voltage, temperature and/or input jitter can randomly induce the output Q of the FF in a high or low logic state (i.e., 1 or 0). Metastability can appear as an FF that switches later or does not switch at all. It can present a short pulse at the FF output (so called runt pulse) or causes FF output oscillations and falls in a metastability condition.

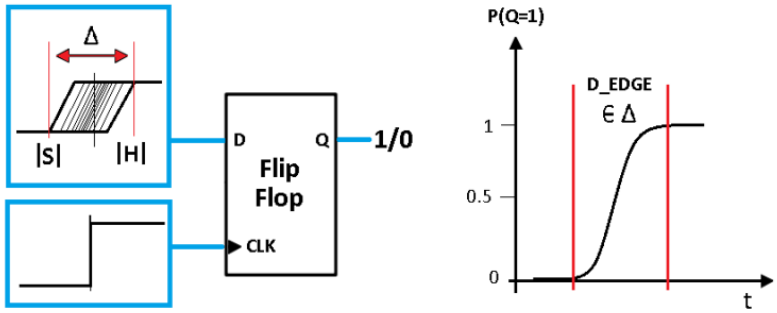

Figure 3A - D-type FF metastability principle: the phase relation between the two FF inputs edges (left); the probability of the output value as a function of the time (right).

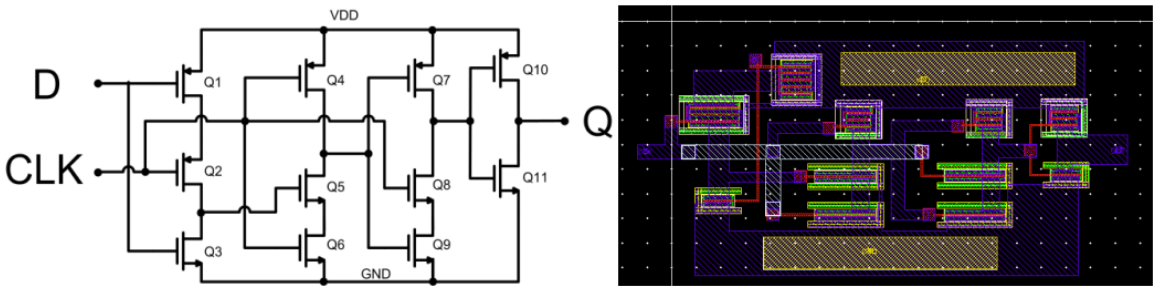

Figure 4A - The D-type FF: schematic circuit at the transistor level (left) and the corresponding designed layout employed for the metastability analysis (right).

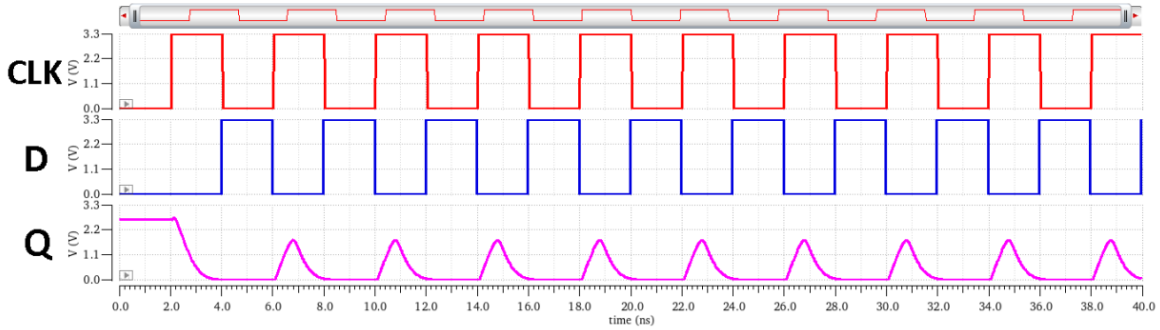

Figure 5A - D-type FF post-layout simulation results showing the metastability effect (CLK is the input clock at 250 MHz of the FF and D is an its replica delayed by a half period used as the FF data input D, Q is the resulting output of the FF).

However, since a precise and accurate (i.e., ideal) synchronization between the edges of data and clock signals is very difficult (i.e., unfeasible) to be reached, the generated output random sequence could present a slight bias with the consequence that the probability of generating a 0 or 1 symbol is not the same. This effect influences the χ^2 evaluation parameter defined as:

$$\chi^2 = \frac{(N_0 - N_1)^2}{N_{TOT}}$$

where N_0 is the number of 0 in a sequence of N_{tot} bits and N_1 the number of 1 in the same sequence. Low values of χ^2indicate that 0 and 1 occur in a generic element of the sequence with the same probability. Generally, in order to achieve this operating condition, a post-processing algorithm must be also implemented as previously outlined.

II. Overall architecture of the designed TRNG

Referring to the considerations reported above, Figure 6A summarizes all the main sources of entropy employed and exploited for the implementation of the TRNG: the jitter of a PLL and of a phase-shifter as well as the metastability state of an FF. The output jitter obtained by a PLL on the generated clock signal is combined with that one generated by a phase shifter that, by providing a data signal (i.e., a shifted replica of the clock), introduces random variations of the relative phase shift between the edges of the data and clock input signals of an FF. Thus, according to Figure 3A, when the edges of the data and clock signals occur exactly at the same time at the two inputs of an FF, the output is not predictable and, ideally, can be at the logic state zero (0) or one (1) with the same probability since no-biased noise is present (i.e., the metastability state). On the other hand, in order to obtain the metastability state of an FF, its S/H time violation must be

operated/exploited by a fine regulation of the relative phase shift between the data and the clock input signals of the FF.

Consequently, in these operating conditions, any variation of the supply voltage, temperature and/or input jitter can induce the random output of the FF in a high (1) or low (0) logic state. The combination of all these considered effects provides a random variation of the probability of the occurrences of the logic state zero (0) or one (1) at the output of the FF so providing an enhancement of the overall entropy of the TRNG architecture. More in detail, Figure 7A shows the overall block scheme implementing the basic operating principle of the designed TRNG architecture: the PLL generates a clock signal for the FF and one replica of this signal, used as data signal for the same FF, is suitably delayed through the phase shift block. In order to achieve a metastability state of the FF, the feedback control block properly regulates the phase shift between the clock and the data signals of the FF: it counts within a time window the occurrences of the logic level zero (0) and one (1) at the output of the FF and gradually increases, through a control signal, the delay introduced by the phase shift block until an acceptable near-to-zero bias of the output raw bitstream is reached (i.e., until the logic levels zero (0) and one (1) have "almost" the same occurrences during the specific operating time, demonstrating that the FF reached the metastability state). Nevertheless, the achieved bias condition at the output raw bitstream can be further improved by a post-processing procedure so providing a final "true" random bitstream.

Moreover, in order to maximize the statistical randomness of the output bitstream of the designed TRNG it is necessary a careful strategy in designing a suitable hardware architecture and its specific implementation (e.g., through a proper place & route processes and/or the use of fine delay elements for the synchronization of the signals, etc.) [25]. In this sense, it is important to consider that typically in an FPGA board the clock signal has a dedicated route with respect to the data signal. For this reason, it is quite difficult that the edges of these signals reach the inputs of an FF at the same time without an additional block that provides to add a suitable time delay. Therefore, in this case, the main purpose

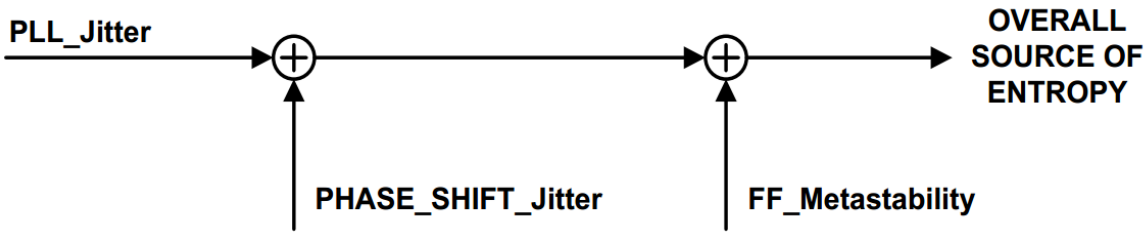

Figure 6A - Main sources of entropy of the implemented FPGA-based TRNG.

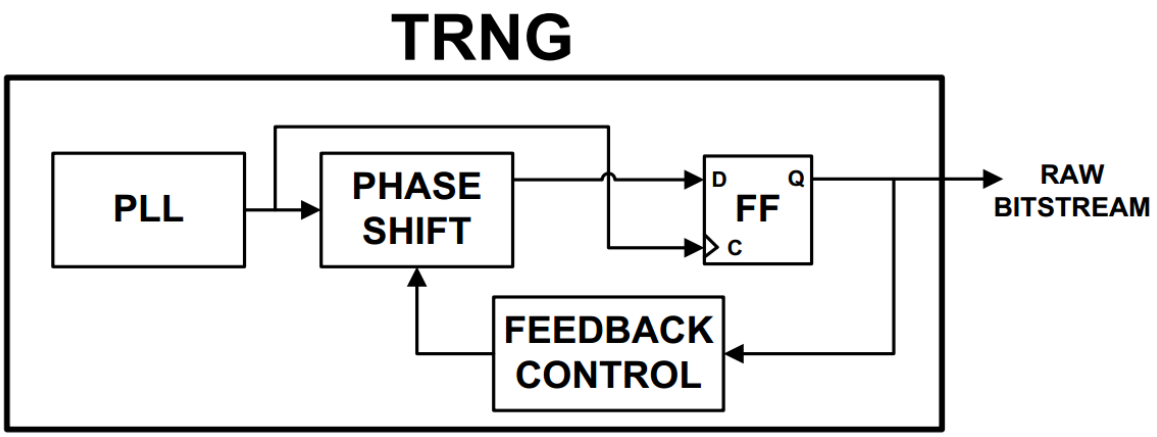

Figure 7A - Block scheme implementing the basic operating principle of the developed FPGA-based TRNG.

of the use of a phase shift block, consisting of a selectable time delay discrete elements, is to compensate for the time delay occurring between the two different paths of the FF clock and data signals. In Figure 8A the overall block scheme of the TRNG architecture implemented on a Xilinx Ultrascale XCKU040 FPGA is reported. The solution utilizes only a PLL and 3 primitive blocks for the generation of the random sequence together with further few logic elements (i.e., 8 D-type FF, 17 LUT and 2 Counters for a total amount of 5 slices and 2 primitives) used only for the initial signals synchronization. The number of primitives utilized for the implementation of this TRNG architecture has been extracted directly from the post Place & Route Report provided by the development environment Vivado2015 used for the FPGA programming.

In particular, an external Low Voltage Differential Signal Clock (EXT_CLK) with an operating frequency of 300MHz and an RMS phase jitter of about 0.7pS is used as the input reference (i.e., an external clock signal) for the PLL block that, in turn, generates two internal 400MHz clock signals with a peak-to-peak period jitter of about 115ps, as analyzed by the Clocking Wizard of Vivado's tools. The PLL has two different outputs: the first one, REF_CLK, is required by the IDELAYCTRL block as reference input (i.e., the reference clock), while the second one is split again in two different paths. One of these paths provides the CLK_D signal that pass through the IDELAYE3 block so to introduce a finite and discrete delay time before reaching the input of the HARD_SYNC DEDICATED SYNCHRONIZERS block composed by a cascade of two D-type FFs (i.e., a 2-state shift register). The FF metastability condition is reached at the first stage (i.e., the first FF) of the HARD_SYNC DEDICATED SYNCHRONIZERS block. On the contrary, the second FF into the same block is used to avoid the propagation of the metastability so obtaining an output with a stable logic state sets to one (1) or zero (0). Thus, the CLK_D signal becomes the data signal to be sampled/acquired by this memory cell (i.e., the

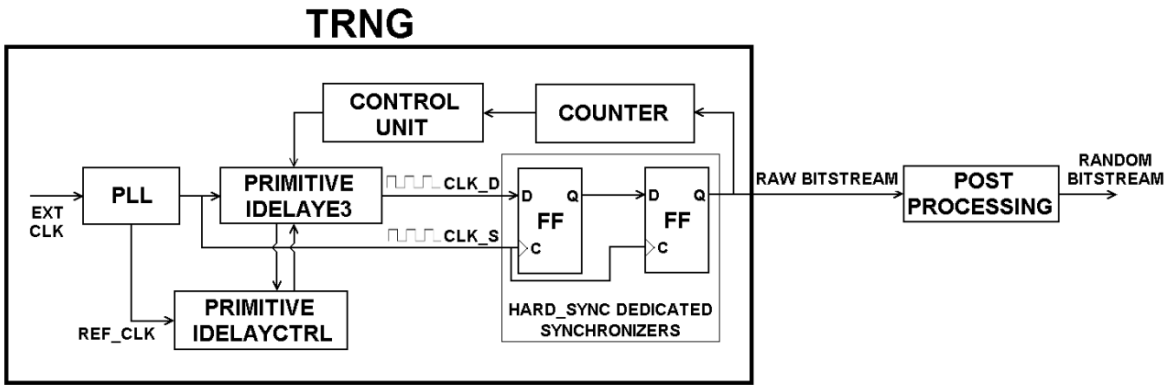

Figure 8A - The overall block scheme of the FPGA implementation of the TRNG architecture.

HARD_SYNC DEDICATED SYNCHRONIZERS block). On the other hand, along the second path, the CLK_S signal is directly connected to the synchronization input of the same HARD_SYNC DEDICATED SYNCHRONIZERS block representing the effective clock signal. The S/H time violation is reached through a fine phase shift regulation between the signals CLK_D and CLK_S. For the synchronization of these two data and clock signals, a fine and stable delay time regulation is needed [25]. In this sense, the IDELAYE3 block is a programmable time delay line located inside the employed FPGA I/O blocks, that provides a maximum of 512 delay taps each one of these introducing a delay time settable from 2.5ps up to 15ps; this primitive does not require any LUT, differently from other kinds of delay line implementations [25]. As a consequence, within a proper time window, the CONTROL UNIT detects the number of generated 1 by a hard-macro COUNTER. Then, using a recursion feedback, the CONTROL UNIT properly adjusts the IDELAYE3 delay line by increasing/decreasing the number of the used taps, until an acceptable near-to-zero bias of the output bitstream is reached. This bias condition is subsequently improved by a post processing procedure. After this initial synchronization, the overall phase delay between CLK_D and CLK_S is about 2.5 ns corresponding to the 400 MHz clock period. In addition, it is important to consider that, also the IDELAYE3 delay line introduces a further random jitter between CLK_D and CLK_S which contributes to the overall randomness of the provided output data [26]. On the other words, the initial synchronization process guarantees the best phase alignment of the two signals CLK_D and CLK_S needed to reach the maximum entropy from the input signal EXT_CLK. Furthermore, the IDELAYCTR primitive block is used to properly achieve and guarantee the needed delay time between the data and the clock signals of the HARD_SYNC DEDICATED SYNCHRONIZERS block. For this purpose, in fact, IDELAYCTR operates a compensation of the delay time drifts due to the supply voltage

and/or operating temperature variations so maintaining at a constant value the required delay time between the two signals CLK_D and CLK_S during the system working time, while the CONTROL UNIT performs a control feedback only during the initial calibration of the system [27]. Finally, a POSTPROCESSING procedure has been also implemented through a further logic block that performs a 4:1 XOR reduction.

III. Experimental results

The implemented TRNG architecture has been tested by employing the experimental set-up reported in Figure 9A and performing the main steps summarized in the flowchart shown in Figure 10A. In particular, according to Figures 7A-8A and referring to Figures 9A-10A, after an initial input signal synchronization, the FF reaches the metastability condition inside the HARD_SYNC DEDICATED SYNCHRONIZERS and the TRNG block generates a raw bitstream at 400Mbps. This is successively processed by the POST PROCESSING block that provides the final output random bitstream at 100Mbps by performing a bit reduction to further decrease the bias of the bitstream. A digital oscilloscope (Lecroy WAVEMASTER 8600A) has been used to show the generated output random bitstream and to evaluate the jitter of the signal CLK_D introduced by del PLL and the IDELAYE3 primitive block inside the TRNG. Moreover, in order to proceed with the quality tests and the randomness evaluations of the generated output data, separate 1Mbit sequences of the final output random bitstream are collected into a data buffer on the FPGA (implemented by using 28 RAM blocks having each one 36Kbit). By means of an UART communication link, one thousands of 1Mbit sequences are sent to a Personal Computer so to provide a graphical representation of the overall acquired random bitstream through the data elaboration in MATLAB2015A environment as well as to perform the statistical analyses by using the NIST suite, the Anderson-Darling and the Kolmogorov-Smirnov tests.

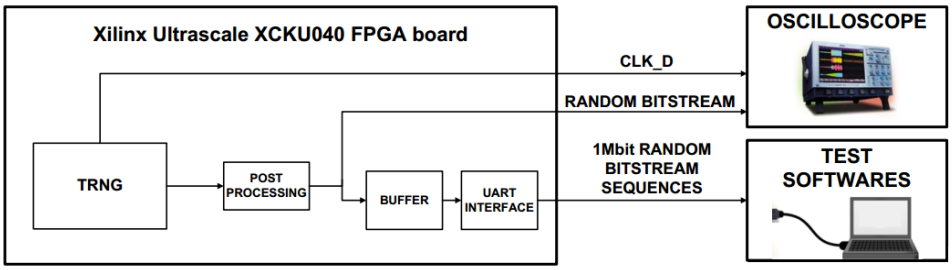

Figure 9A - Experimental set-up.

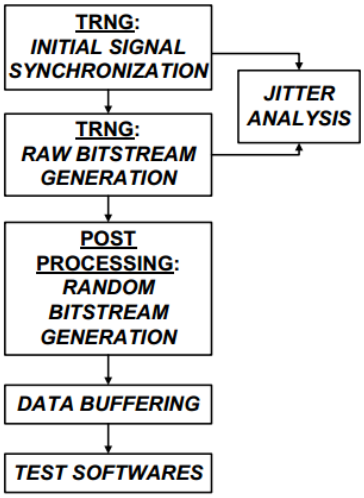

Figure 10A - Experiment flowchart.

More in detail, in order to verify that the bit sequence generated by the developed TRNG is really true random, a deep analysis of its statistical properties must be performed. For this purpose, it is important to highlight that does not exist a specific test able to identify the true random properties of the generated bitstream sequence. In this sense, as a first statistical analysis, the overall jitter of the delayed clock signal CLK_D at 400MHz (i.e., the PLL jitter combined with the IDELAYE3 phase noise) has been experimentally evaluated by measuring a series of 51000 values of its period collected by using a digital oscilloscope (WAVEMASTER 8600A by LeCroy) that provides a time indetermination (e.g., Trigger and Interpolator Jitter) less than 2.5ps. The data of a typical series of these measurements are reported in the histogram of Figure 11A, together with the best fit obtained by assuming a normal distribution for the values of the CLK_D periods, showing a satisfactory statistical quality to be considered as an efficient source of entropy for the TRNG. In particular, the mean value of the period and its standard deviation are equal to 2.49 ns and 0.02 ns, respectively. By performing the χ^2 independence test for a number of degrees of freedom equal to 23, a $\chi^2 = 44.53$ is calculated corresponding to a probability of 0.47% to obtain $\chi^2 > 44.53$. As a consequence, for a significance level of $\alpha = 0.0047$, the null hypothesis can be rejected and, thus, there is no reason to reject the assumption of the normal distribution for the collected data. Furthermore, referring to Figure 8A, it is also important to consider that the CLK_D total jitter results to be the sum of the maximum jitter introduced by the PLL (i.e., 115ps) and of that one given by the IDELAYE3 block. These results combined with the metastability effect of the FF inside the HARD_SYNC DEDICATED SYNCHRONIZERS block, allow increasing the overall randomness of the TRNG output bitstream. In addition to this analysis, it is a common practice to employ several statistical tests to exclude the evidence of a no-random sequences generated by the TRNG. In particular, since human brain is capable to detect periodic repetitions of

geometrical sequences visualized in a picture, a series of visual checks of the generated output bit rate are performed, one on these is reported in Figure 12A.

This image corresponds to a random generation of 1Mbit bitstream converted into a 1000x1000 black and white pixels: the black and white pixels correspond to the occurrences of the symbols 0 and 1, respectively. It is evident from Fig. 12 that the image does not present any evidence of periodic sequences and repetitions. Furthermore, the NIST test suite is commonly used to analyze, through fifteen different algorithms/tests, the distribution of a set of data that can be considered random with a high probability if these tests are successfully passed [28-30].

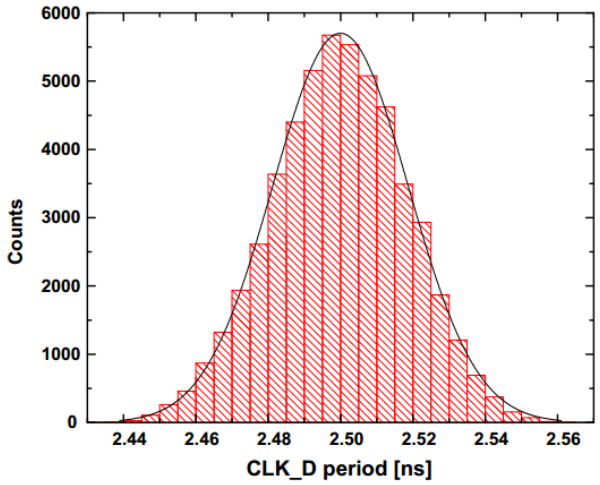

Figure 11A - Histogram of the statistical distribution of a series of 50000 values of the CLK_D periods and the best fit curve assuming a normal distribution of the collected data.

In this sense, 1000 bitstream sequences of 1Mbit generated by the implemented TRNG have been analyzed by the NIST suite and have passed successfully all the tests. The achieved results are reported in Table I where the values of χ^2 indicate the uniformity of the distribution of the p-values in each test (i.e., the probability that a perfect

random number generator is able to generate a sequence less random than the tested sequence or, equivalently, the p-values summarize the strength of the evidence against the null hypothesis) and the proportion is the ratio between the number of the sequences that have passed the test and the total number of the analyzed sequences.

Figure 12A - The image of 1Mbit bitstream generated by the designed TRNG converted into a 1000x1000 pixels for a preliminary visual check of its randomness property.

Additionally, in Figure 13A is graphically shown the distribution of the ordered p-values obtained from each sub-test achieved by performing both the Anderson-Darling (AD) and the Kolmogorov-Smirnov (KS) tests that include also the NIST test. When a good generator is tested and verified, the points should not be distributed too far from the "ideal" black line. The satisfactory statistical parameters reported in Figure 13A together with those ones summarized in Table IA demonstrate that the sequences generated by the proposed TRNG can be considered the results of a "true" random generation.

TABLE IA - Results of the NIST test performed on 1000 random sequences of 1Mbit bitstreams.

Type of NIST test	χ^2	**Proportion**
Frequency	0.8832	0.996
Block Frequency	0.3505	0.994
Cumulative Sums	0.1223	0.993
Runs	0.9155	0.994
Longest run of Ones	0.6591	0.987
Rank	0.4750	0.997
DFT (Spectral)	0.5544	0.992
Non-overlapping Template Matching	0.2133	0.998
Overlapping Template Matching	0.7399	0.986
Maurer's "Universal Statistical"	0.7792	0.997
Approximate Entropy	0.6949	0.991
Random Excursions	0.8165	0.994
Random Excursions Variant	0.6993	0.996
Serial	0.2149	0.985
Linear Complexity	0.8343	0.992

Finally, Table IIA summarizes the main characteristics of the developed TRNG compared to those ones obtained by using other hardware-based solutions reported in the Literature. The presented TRNG architecture is competitive in terms of the high output bitrate and requires the smallest number of necessary hardware resources. The subsequent reduced overall power consumption and system complexity making it suitable also for a VLSI implementation as full-custom integrated circuit designed at transistor level in a standard CMOS technology. This achievement can be considered the direct consequence of the use of the PLL jitter and the FF metastability as the main sources of entropy for the random number sequence generation. Moreover, it is also important to consider that it is possible to implement the employed solution also by using other FPGA boards/families since primitives similar to those ones employed in the developed TRNG architecture are also provided by other commercial FPGA boards (e.g., Xilinx Virtex6 and Spartan6). Nevertheless, it is always necessary the presence of the phase shift block to allow for a fine regulation of the introduced time delay between the FF input signals so to reach/guarantee its metastability state. On the contrary, a possible worse resolution of the delay regulation of the phase shift block (e.g., 80ps for the Xilinx Virtex6 instead of 2.5-15ps for the employed FPGA) will require a stronger post processing of the raw bitstream with a consequent reduction of the final output bitrate.

The achieved results make the implemented architecture suitable for different network security/cybersecurity applications in the fields of IIoT and Industry 4.0.

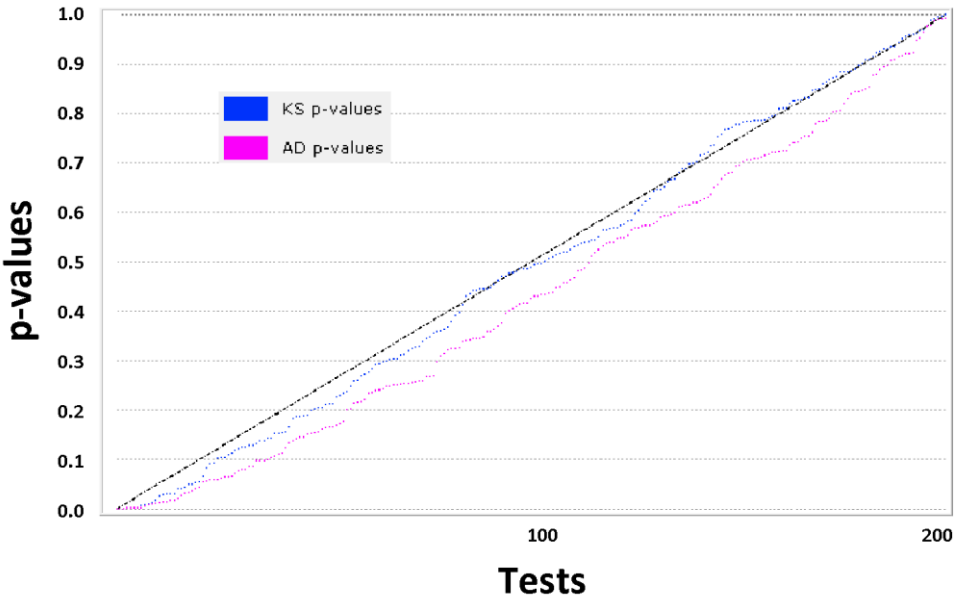

Figure 13A - Results of the Anderson-Darling and Kolmogorov-Smirnov tests.

TABLE IIA - Comparison of the main characteristics of different TRNG solutions.

Reference	Main entropy source	Device	Hardware resources	Throughput	Post-processing
[13]	Metastability	Altera Cyclone III	511 LUTs	133 Mbps	Yes
[12]	Metastability	Altera Cyclone IV	298 LUTs	150 Mbps	Yes
[14]	Ring oscillator	Xilinx XC5VLX50T	147 LUTs	100 Mbps	Yes
[23]	Metastability	Xilinx XC6SLX16	1 DCM; 24 DFFs; 36 LUTs	12.6 Mbps	Yes
[8]	D-Latch	Xilinx XC6VLX240T	224 Slices	50 Mbps	Yes
[20]	RS-Latch	Xilinx XC4VFX20	580 Slices	12.5 Mbps	No
[11]	Chaotic ring oscillator	Xilinx XC6SLX16	256 LUTs	125 Mbps	No
[25]	Metastability	Xilinx XC5LX50T	128 LUTs	2 Mbps	Yes
[21]	PLL jitter	Altera Stratix	120 LE	>1 Mbps	Yes
Developed Solution	***Metastability / Jitter***	***Xilinx XCKU040***	***1 PLL; 3 Primitives***	***100 Mbps***	***Yes***

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APPENDIX B: ANALOGUE FRONT-END CIRCUITS FOR BIOMEDICAL APPLICATIONS

The blood oxygen saturation is percentage of oxygen in the blood. It is defined as fraction of oxygenated hemoglobin to the total hemoglobin present in the blood. The human body maintains a very precise level of oxygen in the blood stream. The normal range is between 95 and 100. The pulse oximeter is the device which is used to measure the heart rate and arterial oxygen saturation. Pulse oximeters are also used to help with the early detection of COVID-19 infections, which may cause initially unnoticeable low arterial oxygen saturation and hypoxia. The New York Times reported that "health officials are divided on whether home monitoring with a pulse oximeter should be recommended on a widespread basis during Covid-19. Studies of reliability show mixed results, and there's little guidance on how to choose one. But many doctors are advising patients to get one, making it the go-to gadget of the pandemic." [1]. Typically, the measurement is based on the photoplethysmogram signal acquired. The reflective pulse oximeter has LEDs and photodiode adjacent to their sides. The light emitted from the LED is reflected back into the photodiode. Based on the intensity level changes the estimation of the parameters is done.

In Figure 1B, an improvement of the reflective pulse oximeter is the fluorescence-based method that allows the use of comfortable dry electrodes without the need for heating. This method uses a thin film consisting of platinum porphyrin (Pt-porphyrin). When the film is exposed to blue light, it emits red light, the intensity and lifetime of which are inversely proportional to the concentration of O_2 around the film. The fluorescence of the thin film is typically measured in terms of its lifetime (i.e. fall time) where τ_0 is the lifetime of the film fluorescence without the quencher (oxygen), and τ is the lifetime of the fluorescence with the quencher, as reported in Figure 2B [2].

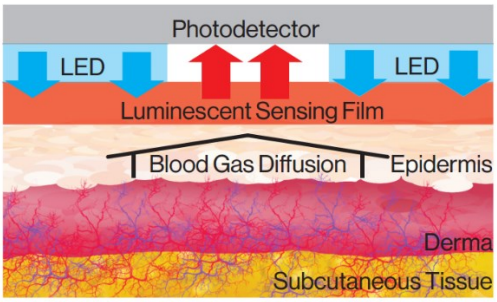

Figure 1B - Fluorescence-based transcutaneous oxygen sensing technique.

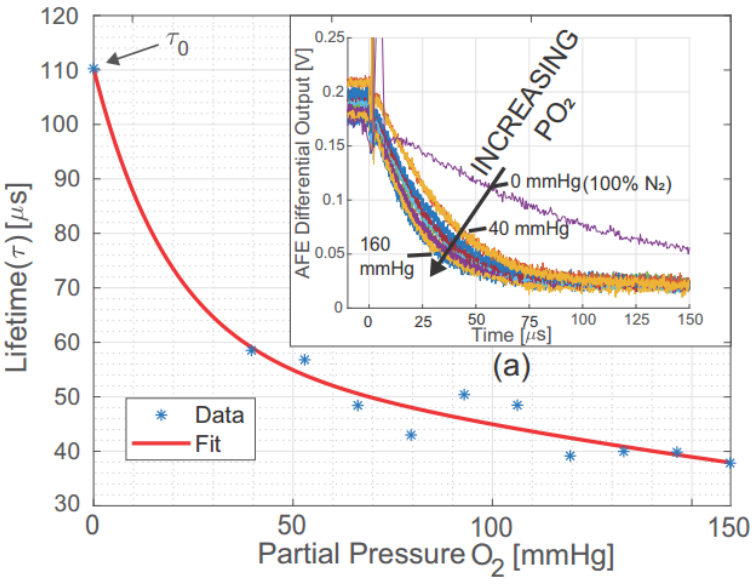

Figure 2B - Fluorescent lifetime vs PO_2.

For this purpose, an Analog Front-End (AFE) for wearable photoplethysmography acquisition systems must ensure low-power, high-gain, and low-noise.

Usually, these solutions use a TIA as conditioning circuit for the photodiode, however in this chapter also others approaches of data acquisition are proposed, as reported in Figure 3B. All the circuits have been realized using Cadence Virtuoso Platform with a TSMC 180 nm library and the resulting microchip is under production. The first solution employs a TIA with tunable gain, this solution can adapt the circuit gain to the light source transmitted optical power and has characteristics comparable with the state-of-the-art similar application. The second solution converts a variation of the photocurrent generated by the PD to a square wave frequency modulation. The last solution employed is based on the variation of the Junction capacitance C_J of the PD as function of the incident light. This variation changes the frequency of the output square wave signal. The last two solutions generate outputs that don't require ad ADC for the data elaboration and can be processed easily by digital blocks. Moreover, in order to validate the proof of concepts of the last two solution, experimental measurements have been performed using commercial components.

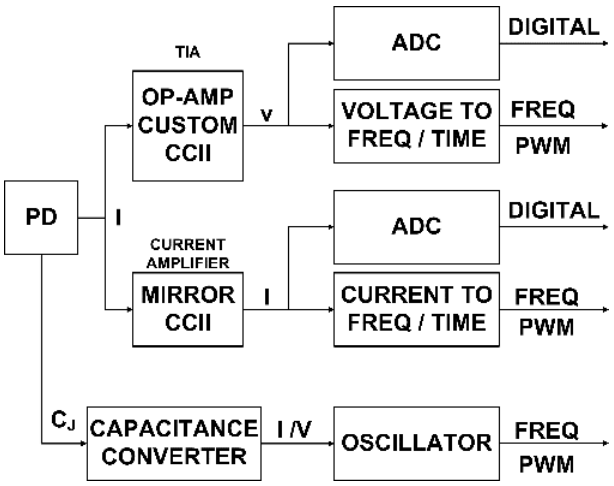

Figure 3B – Possible different solutions of AFEs for photodiodes.

I. Transimpedance amplifier

The first AFE proposed in Figure 4B is a transimpedance amplifier with a tunable gain. The tunable current amplifier is based on a current mirror scheme composed of the transistors M1-M2-M4 and M5 or M7 or M9 according to the digital signals V1, V2 and V3 that select the desired gain, while the analogue input signal V_{ctrlAN} of M3 is used for a more accurate tuning. The capacitances C1 and C2 are required for the stability of the system. The transistor size is reported in Table 1B.

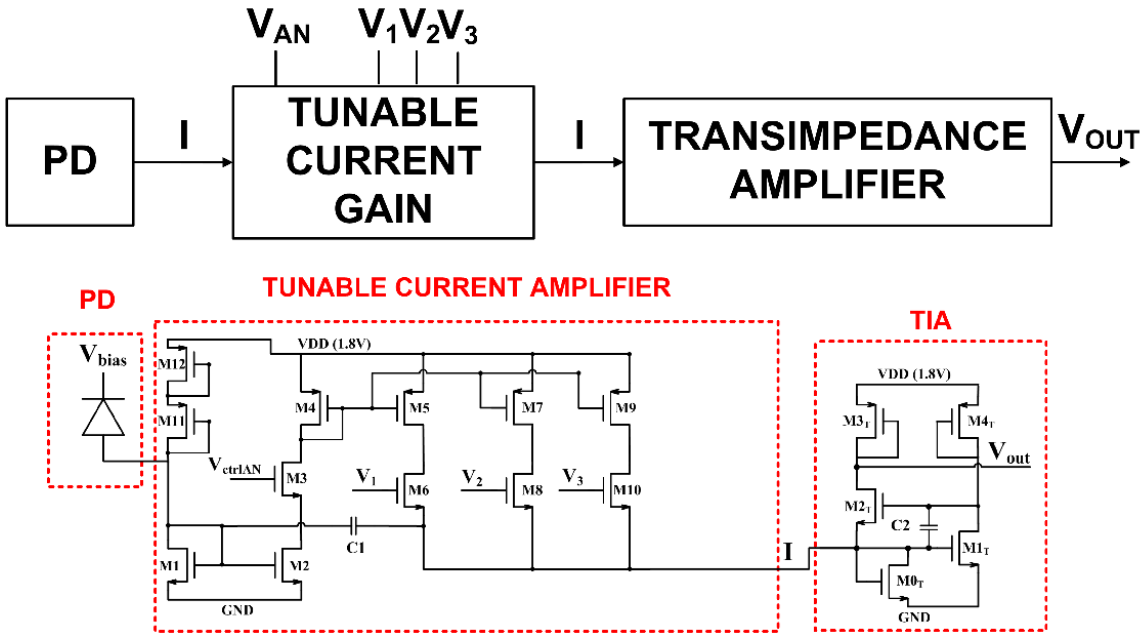

Figure 4B - Block scheme and schematic circuit, at transistor level, of the designed TIA.

Table 1B – Transistor sizes of the designed TIA circuit.

TRANSISTOR	W/L (µm / µm)
M1, M2	1/0.18
M3	2/0.18
M4, M5	0.22/0.36
M6, M8, M10	0.22/0.72
M7	1/0.36
M9	3.5/0.18
$M0_T$	1/1.8
$M1_T$, $M4_T$	1/0.36
$M2_T$	3/0.18
$M3_T$	1/4

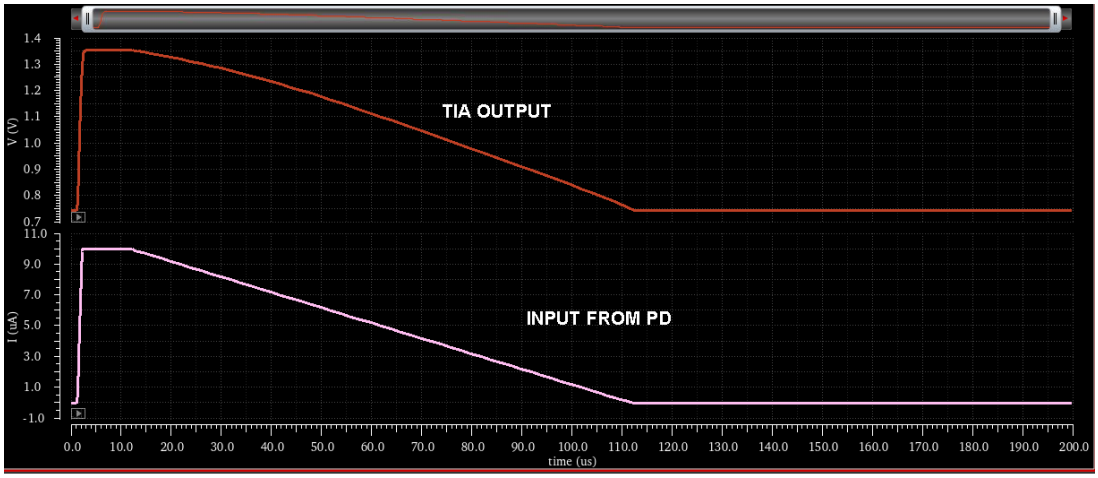

Figure 5B – Example of the transient time simulation results of the TIA.

In order to emulate the film fluorescence lifetime, the simulated input current coming from the PD is a current signal with a pulse-width of 10 µs, a rise time of 1 µs and a fall time of 100 µs, as shown in Figure 5B. In the same figure is possible to observe the TIA output transient simulation considering an input pulse amplitude of 10 µA (V1 = 1.8 V, V2=V3=GND, setup used for an input range of 10-1 µA, average power consumption equal to 55.7 µW). Similar simulation results are obtained considering an input pulse amplitude of 2 µA (V2 = 1.8 V, V1=V3=GND, setup used for an input range of 2-0.2 µA, average power consumption equal to 50.7 µW) and an input pulse amplitude of 400 nA (V3 = 1.8 V, V1=V2=GND, setup used for an input range of 400-40 nA, average power consumption equal to 49.2 µW). The Figure 6B reports a comparison between post schematic transient simulation and post layout transient simulation of the output TIA. The layout of the circuit requires an area on chip of 2070 μm^2.

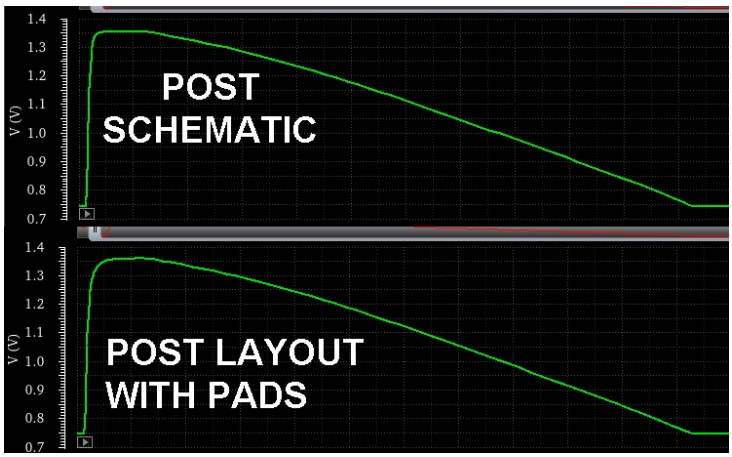

Figure 6B - Comparison between post schematic and post layout transient time simulations of the designed TIA.

II. Current-to-frequency converter

The circuit proposed in Figure 7B and Table 2B converts a variation of the photocurrent generated by the PD to a square wave frequency modulation. The pair of transistors Q11-Q14, Q12-Q15 and Q13-Q16 form a three-stage inverter ring oscillator. The frequency of the output oscillation depends to the current that flow through the pull-up and pull-down nets of the first inverter (Q11-Q14). This current is proportional to the photocurrent generated by the PD thanks to the pair of current mirrors Q1- Q8/Q9/Q10 and Q2 – Q17/Q18/Q19. Also in this case, it is possible regulate the current gain of the mirrors through the digital signal V1, V2 and V3. At last, the transistors Q3-Q4 are used to regulate the minimum frequency of the output square wave and the Duty Cycle.

In Figure 8B a transient simulation of the current-frequency converter considering an input pulse amplitude of 10 µA (V2=1.8 V, V1=V3=GND, average power consumption equal to 44 µW). Similar results are obtained considering an input pulse amplitude of 100 µA (V1=1.8 V, V2=V3=GND, average power consumption equal to 93 µW), and an input pulse amplitude of 1 µA (V3=1.8 V, V2=V1=GND average power consumption equal to 42 µW). In all these cases the maximum output frequency is about 4 MHz.

A Corner Analysis has been performed considering a temperature range of -25° / 75° and a power supply equal to +/- 10% of the standard value (1.8 V). The Layout of the circuit is of 4680 μm^2.

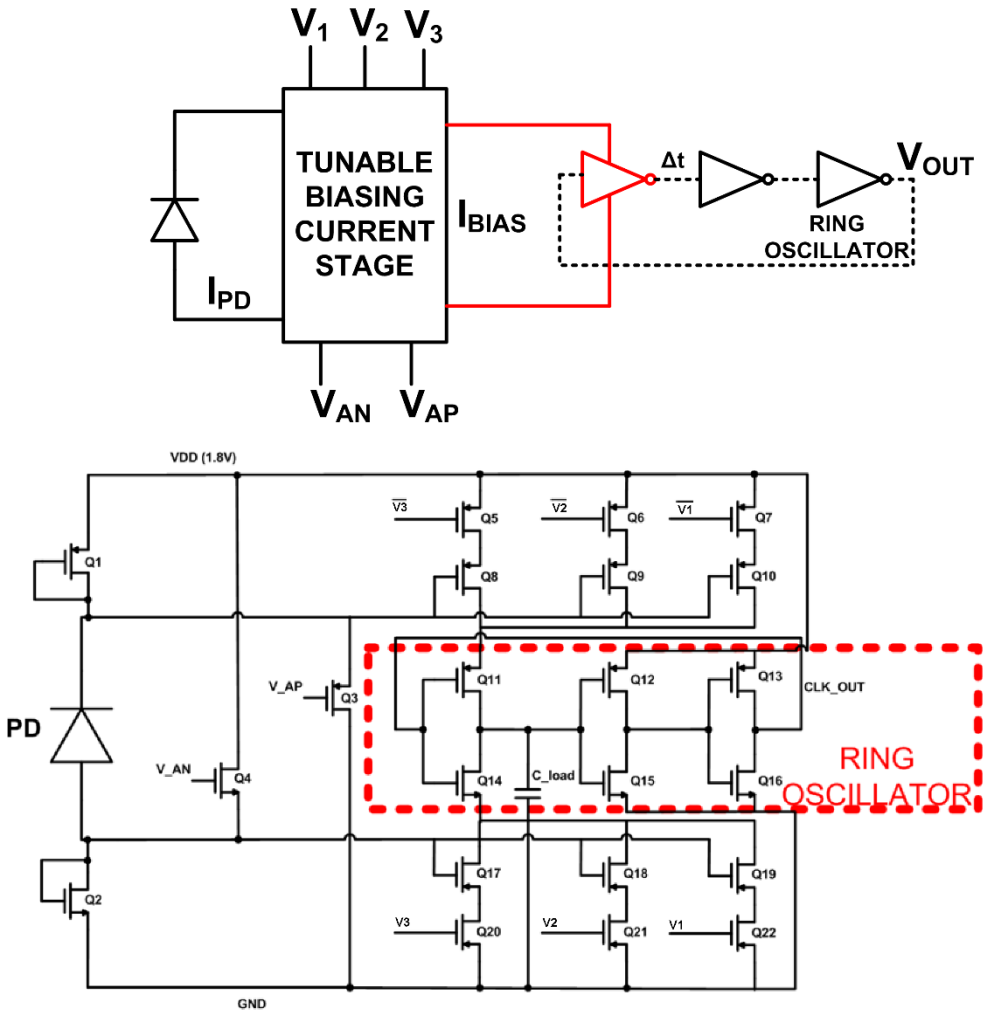

Figure 7B - Block scheme and schematic circuit of the current-to-frequency converter circuit.

Table 2B – Transistor sizes of the designed current-to-frequency converter circuit.

Transistor	W/L (µm/ µm)
Q1, Q2	17.5/0.18
Q3, Q4	12.5/0.18
Q5	6/0.18
Q6	15/0.18
Q7	20/0.18
Q8, Q9, Q10, Q17 ,Q18, Q19	10/0.18
Q11	18/4
Q12, Q13	18/7
Q14	6/4
Q15, Q16	6/7
Q20	3/0.18
Q21	11.5/0.18
Q22	17.5/0.18
C_LOAD	0.2 pF

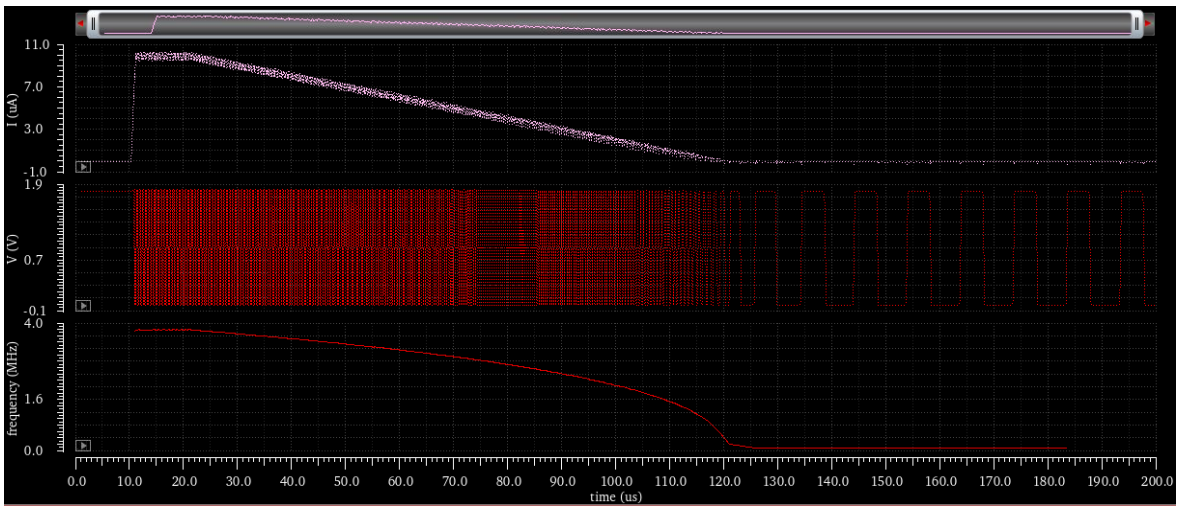

Figure 8B – Example of the transient time simulation result of the current-to-frequency converter.

In order to validate the proof of concepts of the current to frequency converter, the circuit has been also simulated with Cadence Pspice and implemented using a CD4007 commercial components by Texas Instruments (a CMOS Duale complementary pair plus inverter). The experimental measurements of the circuit have been achieved using a BPW34 photodiode. The system presents a slight nonlinearity, as reported in Figure 9B(a). Anyway, it is always possible to regulate the laser power bias and range in order to work in the linear zone of the circuit (Figure 9B(b)).

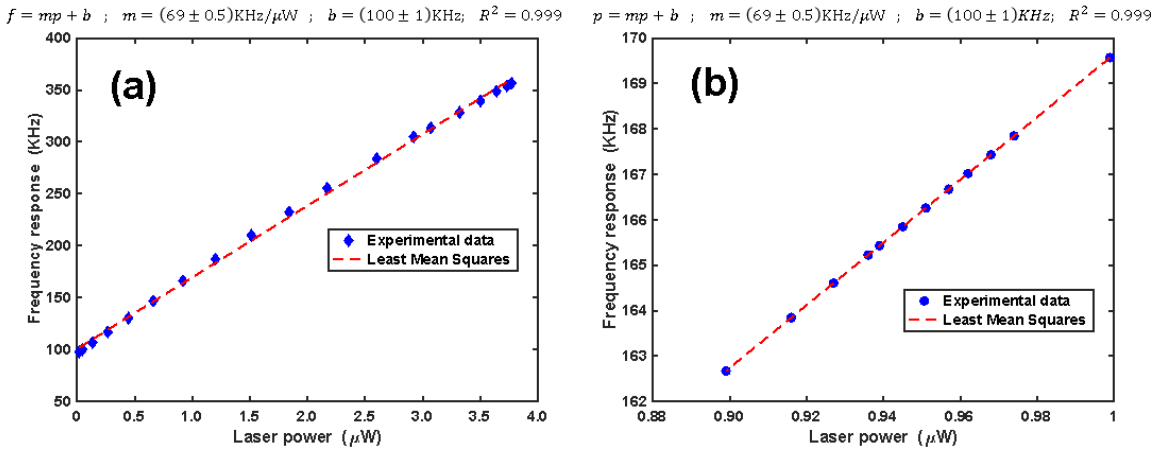

Figure 9B - Experimental results of the current-to-frequency converter implemented with discrete components.

III. Capacitance-to-frequency converter

The last readout circuit proposed for photoplethysmography applications is shown in Figure 10B. The Junction Capacitance (C_J) of a photodiode change as function of the Depletion width W defided as:

$$C_J = \frac{\varepsilon_{Si}\varepsilon_0 A}{W_d} \qquad W_d = \sqrt{[2\varepsilon_{Si}\varepsilon_0(V_{bi} - V_A)(N_A + N_D)/(q\, N_A N_D)]}$$

Anyway, this function is approximated and does not consider that the incident light introduces a small change of the C_J. The proposed circuit can read the variation of C_J and convert it in a square wave frequency modulation. The circuit is composed by two Second Generation Current Conveyor (CCII). The CCII on the left is used as derivator, more in detail the current that comes from the node X reaches an high-pass filter composed by C_J and R1 deriving the signal. The derived signal comes into Y node of the CCII on the right and has a slope proportional to the instantaneous value of C_J. The CCII on the right works as hysteresis comparator and, thanks to a feedback with the derivator, generates an output square wave with a frequency inversely proportional to the C_J value. Approximately, the period of the output oscillation can be evaluated using the following formula.

$$T = 4 * C_J * R1 * ln\left\{\frac{[(R1*R4)-(R1*R2)]}{(R1*R2)}\right\} \qquad (1)$$

The sizes of the transistors and the parameters of the integrated CCII are presented in the Table 3B and Table 4B, respectively.

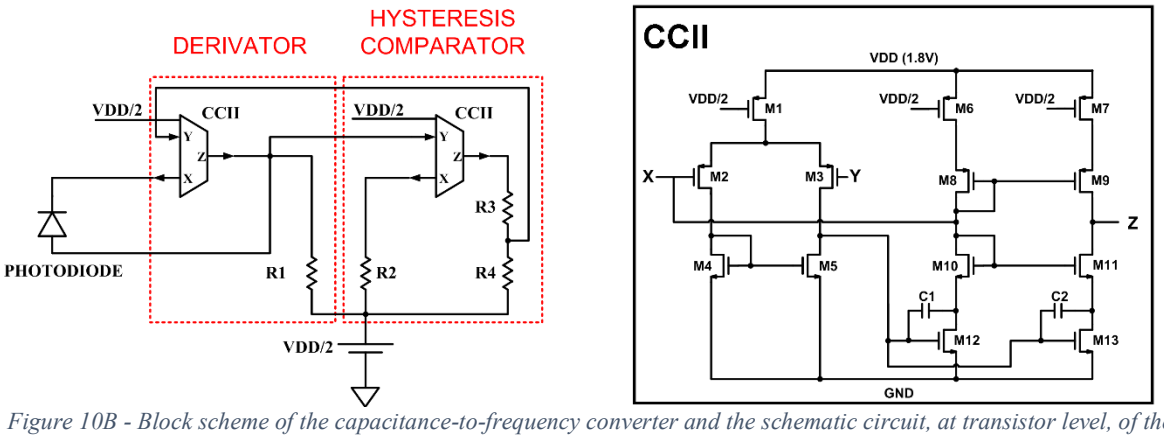

Figure 10B - Block scheme of the capacitance-to-frequency converter and the schematic circuit, at transistor level, of the designed CCII.

Table 3B – Transistor sizes of the designed capacitance-to-frequency converter.

Transistor	W/L (µm/ µm)
M1, M4, M5	2/2
M2, M3	80/2
M6, M7	20/2
M8	150/0.18
M9	150/0.18
M10	50/0.18
M11	50/0.18
M12, M13	80/0.36
C1, C2	0.2 pF
R1	32 kΩ
R2	300 Ω
R3	9 kΩ
R4	1 kΩ

Table 4B – Parameters of the designed capacitance-to-frequency converter.

Parameter	Value
Supply voltage	0-1.8 V
Overall Power consumption	427 µW
Z node Resistance of CCII	1.15MΩ
X node Resistance of CCII	46Ω
Voltage Gain of CCII	0.989
Current Gain of CCII	0.9999

In Figure 11B, a transient simulations of the circuit output (on right) and its frequency (on left) for different C_J are shown. The simulation results are: a square wave with (a) a frequency of 1.45 MHz for a C_J equal to 1 pF, (b) a frequency of 1.01 MHz for a C_J equal to 2 pF and (c) a frequency of 581 kHz for a C_J equal to 5 pF. In the frequency response, it is possible to observe also a slight variation of the frequency, according with a current pulse of 10 µA. After simulation performances with Cadence Pspice, the circuit has been implemented using commercial components. In particular, the CCII has been implemented using an AD844 by Analog Devices. Subsequently, experimental measurements have been performed. In Figure 12B (a) is shown the frequency response versus laser power variation considering a sensitivity and resolution obtained for a variation of the laser power from 29 nW to 19.2 µW. Instead, in Figure 12B (b) is shown the frequency for a variation of the polarizer angle equal to 2°. The Layout of the CJ to frequency converter is presented in Figure 13B for an area of 8525 μm^2.

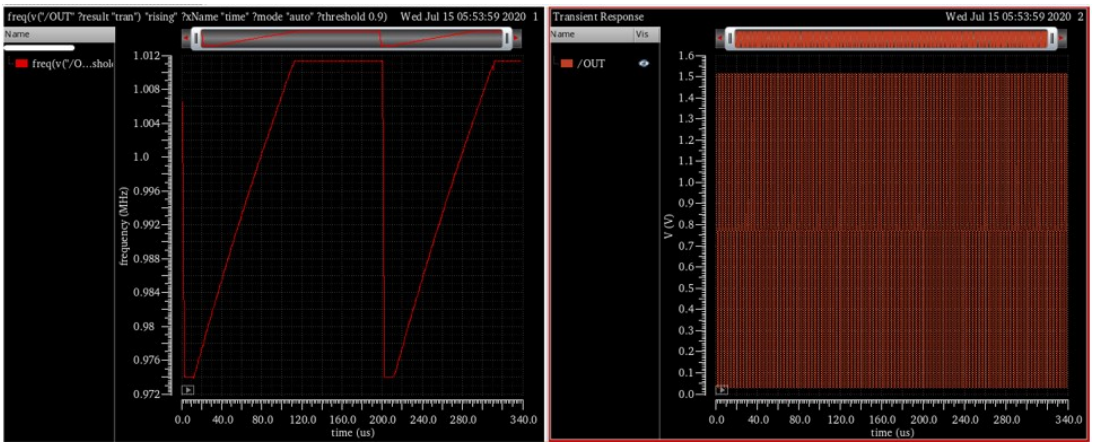

Figure 11B – Example of the transient time simulation of the capacitance-to-frequency converter.

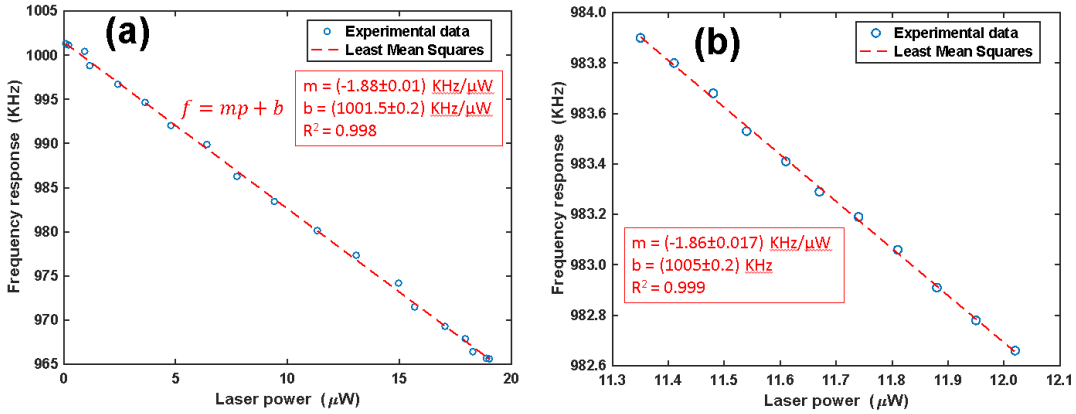

Figure 12B - Experimental response of the C_J to frequency converter implemented with discrete components.

Finally, the Figure 13B reports the final layout complete by padframe. The three proposed AFE are presented in the bottom-right corner of the layout. The remaining area is occupied by integrated PDs (the areas with massive diffusion, in red) and by a wireless optical power transfer system (in the center of the chip) that are described in the subsequent appendices.

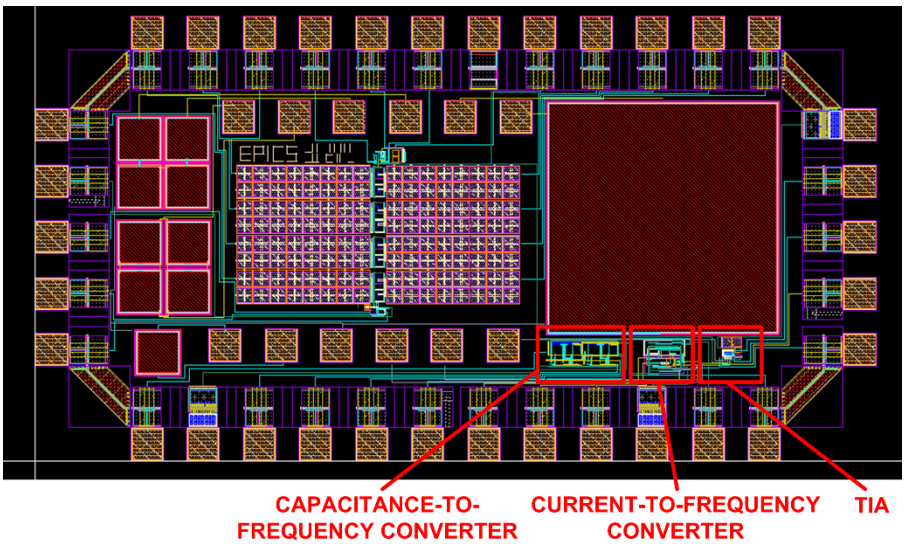

Figure 13B – Complete layout design of the optical biotelemetry system including the chip padframe.

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[2] I. Costanzo, et al «An Integrated Readout Circuit for a Transcutaneous Oxygen Sensing Wearable Device,» IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, USA, April 2020.

APPENDIX C: OPTICAL WIRELESS POWER TRANSFER

Wearable or implantable low-power electronics devices such as active contact lenses or intraocular pressure sensors, require an exceedingly small-form factor and cannot tolerate surface mounted components or standard batteries. Photovoltaic (PV) energy can be harvested with miniature photodiodes or flexible thin-film PV cells to eliminate the need of batteries [1]. However, the voltage that can be drawn from an on-chip solar cell is a value not exceeding 0.55 V. Thus, in order to obtain a higher voltage values, it is possible to connect two solar cells on a common Si substrate in series. Even though this low voltage level is acceptable and possibly beneficial for low power digital operations, it is lower and more less stable than the supply voltage required for analog subsections of the chip (usually at least 1 V regulated). Therefore, a regulated dc–dc step-up converter is needed. As shown in the Appendix C**,** the reflective pulse oximeter already uses laser or LEDs for the excitation of the film. So, one of these light sources can be used to transfer power to an PD in order to powering the integrated electronics.

I. System design

The proposed wireless optical power transfer system is shown in Figure 1C and is composed by an oscillator, a driver and a charge pump.

The ring oscillator block in Figure 2C(a) is composed by a three-stage ring oscillator and is powered with a voltage provided by the PD. So, the output oscillation amplitude and frequency depend on the PD output voltage, the frequency can also be changed acting on internal capacitors. The driver block in Figure2C(b) decouples the oscillator and the charge pump block providing two square wave signals with a phase difference of 180 degree each other. In Figure 2C(c) is shown the charge pump block that is composed by four cross coupled charge pump blocks. The purpose of this block is to improve the output voltage provided to the load in order to reach at last 2V. In this way, as example, the load can be replaced with a LDO voltage regulator that can provide to the integrated circuitry a stable power supply of 1.8V. The circuit was implemented using Cadence Virtuoso environment and the inverter sizes are reported in Table 1C.

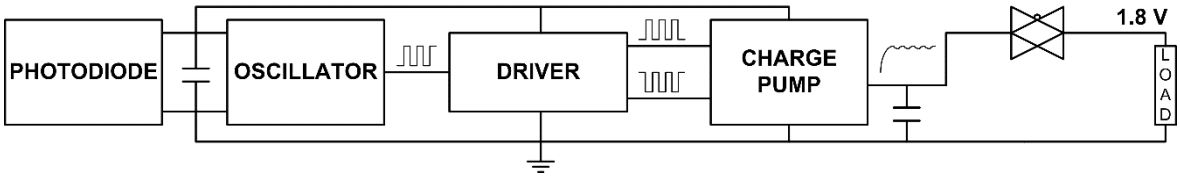

Figure 1C – Block scheme of the proposed optical wireless power transfer system.

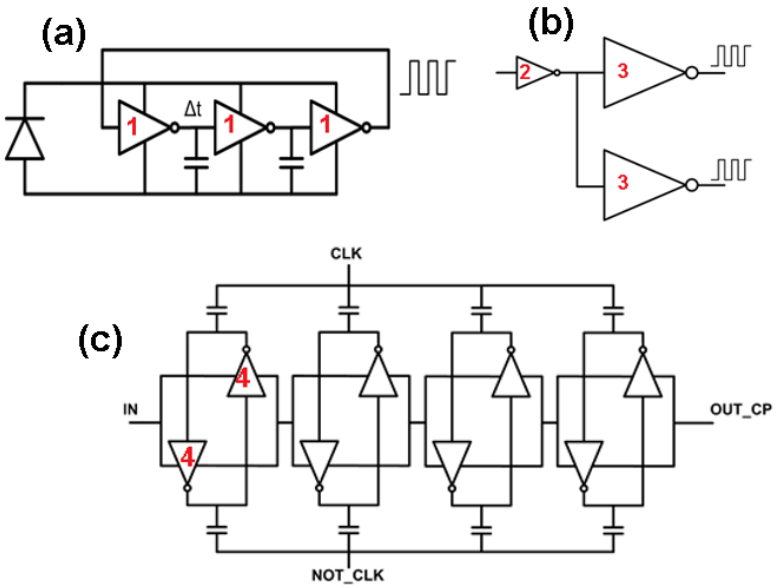

Figure 2C – Internal blocks of the system.

Table 1C – Transistor sizes of the inverter circuits.

INVERTER	PMOS W/L (µm/ µm)	NMOS W/L (µm/ µm)
1	0.44/1	0.44/5
2	0.22/0.18	0.22/0.36
3	4/0.18	8/0.18
4	150/0.18	150/0.18
PASS GATE	100/0.18	100/0.18

II. Simulation Results

Starting from an input voltage of 0.5V, the output of the charge pump reaches the value of 2.45V considering an open circuit load, as shown in the post layout transient simulation of Figure 3C.

Considering instead an input of 0.7 V, the output reaches a value of 3.4 V. In the same conditions, using a load of 0.1 pF in parallel with 1.5 MΩ, the oscillation frequency is 205 kHz and the output is equal to 2.65 V / 1.8 uA with an efficiency (evaluated as the ration between the output power and the input power of the system) PCE (η) = 0.65.

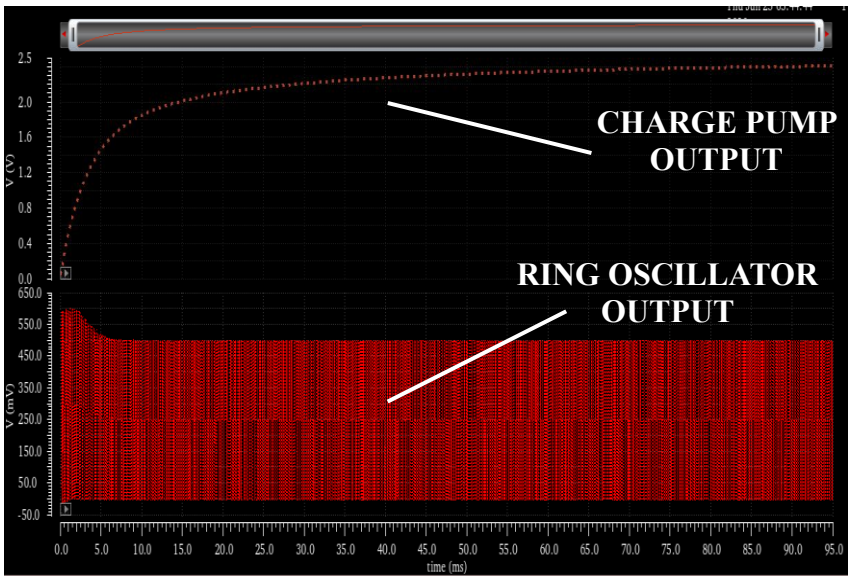

Figure 3C – Post layout simulation of the charge pump (open circuits).

Since the reflective pulse oximeter, as others kind of biosensing system, requires a short time measurement, it is possible to supply the load only when needed and accumulate charge coming from the charge-pump in the intervals between a measurement and the subsequent.

In this way, it is possible to work in discrete mode providing a proper current to the load during the measuring time, as shown in Figure 4C.

When a load of 2.5 nF in parallel with 4kΩ is not connected to the optical power transfer system, the capacitor at the output of the charge pump reaches a voltage of 2.65 V. When the load is connected, the system capacitor provides 2.4V average voltage (always more than 2 V needed for an LDO to generate a stable 1.8 V) and 600 uA for about 5 us. When the load is disconnected, 500 us are required to recharge the capacitor. Obviously, the charge/discharge time depends to the power provided by the PD and by the values of the capacitors of the charge pumps. Moreover, corner analysis of the system as been performed considering a temperature range of -25° / 75° and a PD voltage in a range of 0.5 to 0.7 V. In Figure 5C the layout of the proposed system is reported, each stage of the charge pump is designed with 16 capacitors of 1.79 pF each in parallel for a total area of 0.216 mm2, the system is implemented in the layout shown in Figure 13B of Appendix B. Anyway, it is possible to add external capacitances in order to adapt the DC-DC converter to the characteristics of the system that must be powered. In the end, a comparison with the state-of-the-art similar solutions is reported in Table 2C.

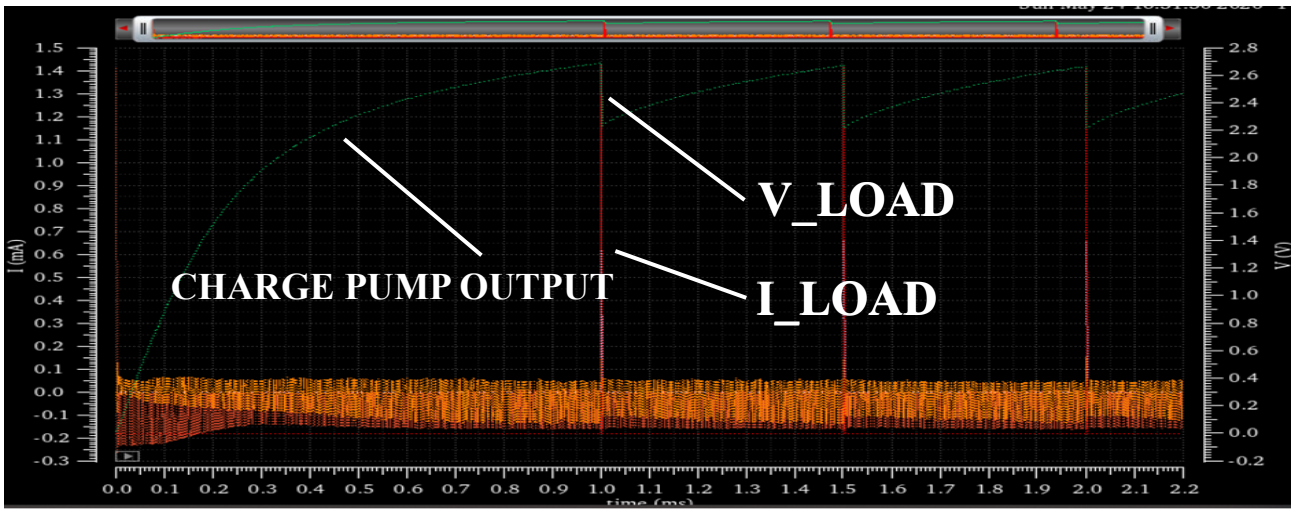

Figure 4C – Post layout simulation of the overall circuit in discrete time operating mode.

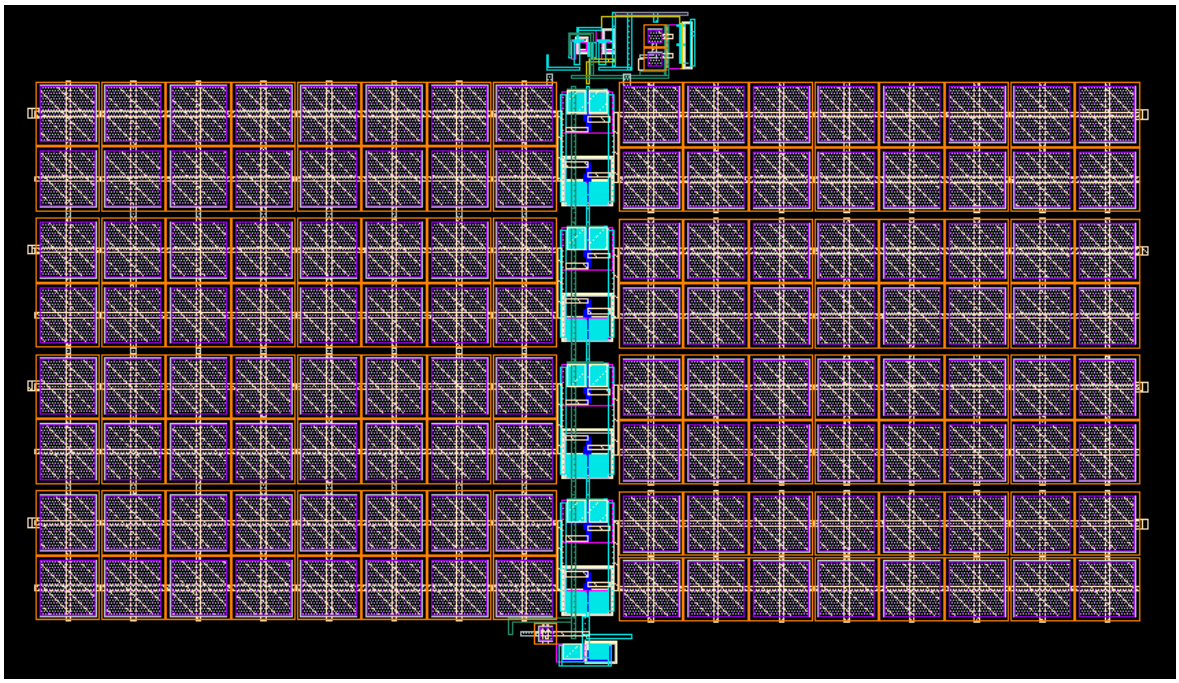

Figure 5C – Layout of the optical power transfer system.

Table 2C - comparison with the state-of-the-art.

	[2] 2015	[1] 2011	[3] 2011	[4] 2010	[5] 2016	[6] 2010	[7] 2014	Developed system (Continuous)	Developed system (Discrete)
Source	N.A.	1.21 mm^2 photodiode	N.A.	Ideal Voltage Source	solar (external)	solar (external)	1 mm^2 photodiode integrated	Internal/external	Internal/external
Process	0,13 µm CMOS	0,13 µm CMOS	65 nm CMOS	65 nm CMOS	0,18 µm	65 nm CMOS	0,18 µm CMOS	0,18 µm TSMC	0,18 µm TSMC
No. of stages	3 stage	3 stage	10 stage	3 stage	N.A.	N.A.	2-stage cross-coupled	4-stage cross-coupled	4-stage cross-coupled
Clock Frequency (f)	250 kHz	800 kHz	20 MHz	10 MHz	17-23 MHz	20 MHz	714 kHz	205 kHz	205 kHz
Vin (V)	0,18/0,45	0,35	0,12	0,18	≈ 0,4	≈ 0,3	0,5	0,7 (0,55 min)	0,7 (0,55 min)
Vout (V)	0,5	1,4	0,77	0,5	1	1	0,8	2,65V	2.466
Iout (µA)	21	3	3,9	8,75	600-1100	190-681	1,6	1,77	615
Efficiency (%)	34/72,5	58	38,8	N.A.	70	N.A.	51,7 (dark current) 39,6 (illumination)	65	35
Pumping Capacitors	6x10 nF (off-chip)	6x25 pF (on-chip)	6x28,6 pF (on-chip)	2x0,4 pF + 6x12,3 pF (on-chip)	N.A.	N.A.	4 x 20 pF	8*28,64(on-chip)	8*28,64(on-chip)

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APPENDIX D: CLOCK DUTY-CYCLE CORRECTION IN INTEGRATED DIGITAL SYSTEMS

As in the optical data link system described in this Thesis, the accuracy of the clock duty-cycle is one of the main important issues in many different applications both for digital and industrial systems such as frequency multipliers/dividers and synthesizers, multiphase clock generators, power converters. In particular, these solutions require a clock signal with a 50% duty-cycle so to guarantee the optimal operating conditions and better performances [1-7]. Generally, clock generators and references (i.e., frequency dividers, quadrature oscillators, etc.) provide clock signals having 50% duty-cycle. However, some solutions, such as crystal-based oscillators, could generate signals with variable duty-cycle typically ranging between 40% and 60%. Consequently, in these cases the clock variation must be suitably compensated by means of a Duty-Cycle Corrector (DCC) circuit whose basic functionality is to provide an output clock signal with 50% duty-cycle at the same frequency of the incoming periodic input signal. The DCCs are mainly employed in high-performances integrated digital system applications such as in Synchronous and Double Data Rate Dynamic Random Access Memories (DDR DRAMs) as well as in high speed I/O data links that are particularly sensible to a clock duty-cycle different from 50% [8-12]. In the Literature, several DCC solutions have been already proposed based on different approaches. In particular, one of the more conventional technique is based on Phase-Locked Loop (PLL) or Delay-Locked Loop (DLL) that suffer from circuit complexity, high power consumption, phase noise degradation, delay mismatch and large silicon area [13-22]. In this appendix it is proposed a new fully-analogue DCC circuit based on a closed-loop architecture operating a continuous time 50% duty-cycle regulation of the output clock signal. The presented solution performs low-pass filtering operations to reveal the mean values of the input and the output clock signals to estimate their duty-cycles proportional to the extracted DC signal levels. Starting from these signals, a suitable feedback provides a control voltage to generate and regulate two levels of currents that properly charge and discharge (asymmetrically) a load capacitor so adjusting to 50% the duty-cycle of the output clock signal. The proposed DCC topology has been designed in AMS 0.35μm standard CMOS integrated technology, powered at 3.3V single supply voltage with a low power consumption and very small silicon area. The circuit solution, employing a very reduced number of components (i.e., 16 transistors, 1 capacitor and few offchip components).

I. Circuit Design

The developed DCC architecture, whose overall schematic circuit is reported in Figure 1D, is capable to perform a continuous-time 50% duty-cycle regulation of the output clock signal CLK_OUT starting from the incoming input clock signal CLK_IN having a whatever/unknown duty-cycle value.

More in detail, the integrable core of the circuit is composed by only 16 transistors (Q1-Q16) and 1 capacitor (C_load) together with an external feedback sub-system constituted by two passive low-pass filters (R1-C1 and R2-C2) and two differential blocks and two differential amplifiers based on Operational Amplifier (OA) in four-resistors configuration (OA_1 with R3÷R6 and OA_2 with R7÷R10). The input signal clock CLK_IN with a certain duty-cycle allows, through the transistor Q8 and Q9, to charge and discharge the load capacitor C_load with controlled constant current levels provided by the transistors

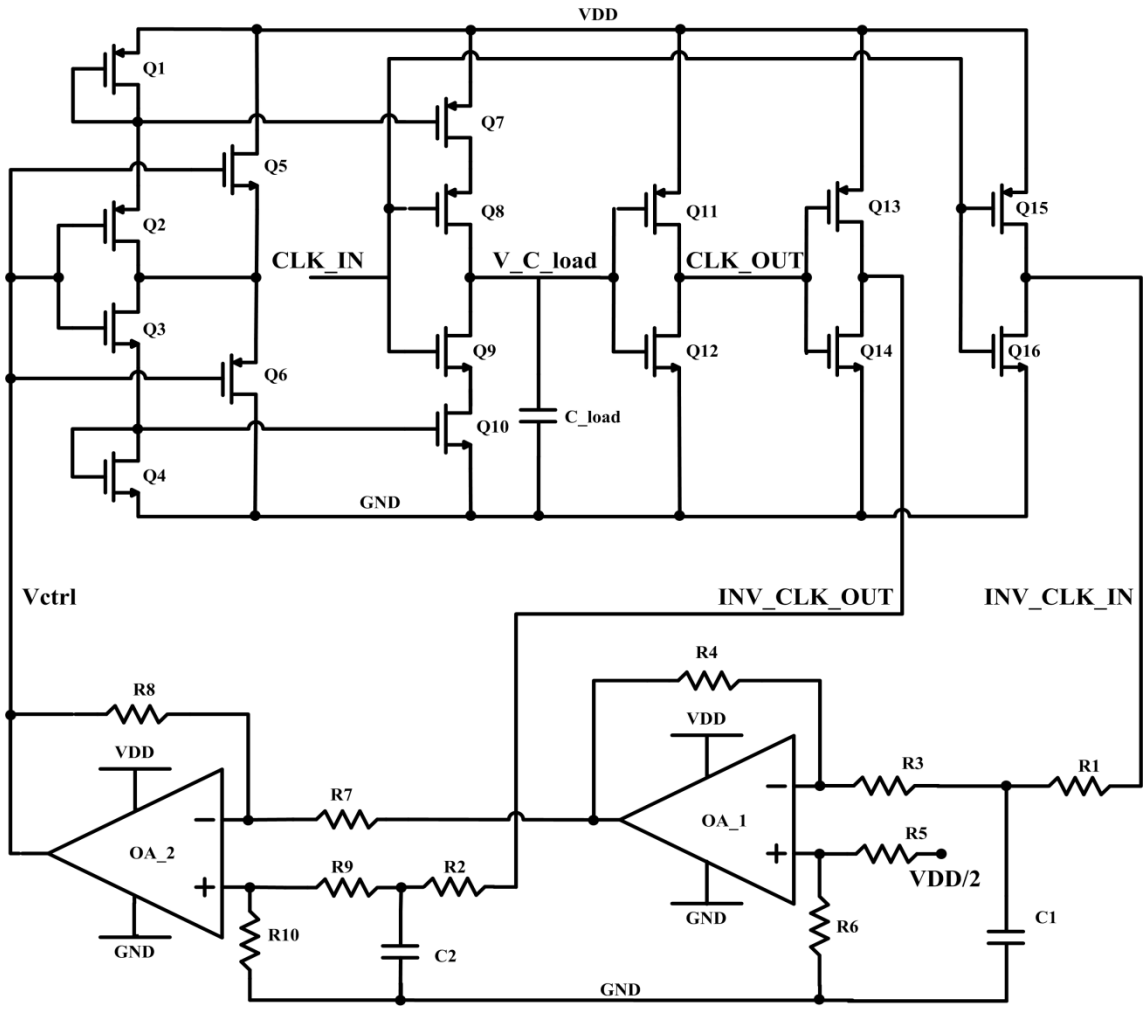

Figure 1D - Schematic circuit of the DCC architecture.

Q7 and Q10. In this way, the voltage level at the V_C_load node (i.e., the voltage of the capacitor C_load) results to be a ramp signal with rising and falling slopes depend on the value of the capacitor C_load as well as on the charging (through Q7 and Q8) and discharging (through Q9 and Q10) current levels. The next stage, formed by the transistors Q11-Q12 implements a standard CMOS inverter (i.e., a Push-Pull stage) and provides an output square waveform representing the output clock signal CLK_OUT having a 50% duty-cycle. In order to perform a suitable correction of the input clock duty-cycle, both the CLK_OUT and CLK_IN signals are buffered through the two further standard CMOS inverter stages (i.e., Push-Pull stages, Q13-Q14 and Q15-Q16, respectively) that provide the two signals INV_BUFF_CLK_OUT and INV_BUFF_CLK_IN. Both these signals are processed through two passive low-pass filters, implemented by R1-C1 and R2-C2 discrete components, allowing to extract their mean values (i.e., the DC levels) proportional to their duty-cycles, according to the following relationship:

$$\text{Signal duty-cycle [\%]} = (\text{DC mean value} / \text{VDD}) * 100 \quad (1)$$

Then, the first differential amplifier (OA_1 with R3÷R6) operates a subtraction between the output of the R1-C1 filter and the reference voltage level equal to VDD/2 (i.e., the half of the supply voltage VDD corresponding to a mean value of a clock signal having a 50% duty-cycle). The output signal provided by this stage, whose amplitude depends on the duty-cycle value of the input clock signal CLK_IN, is then subtracted to the output signal of the R2-C2 filter through the second differential amplifier (OA_2 with R7÷R10). Finally, starting from these operations with the signals related to the estimated duty-cycle values of the CLK_IN and CLK_OUT signals, OA_2 provides a suitable feedback voltage Vctrl controlling the transistors Q1-Q6.

This last stage generates and regulates two levels of currents that properly charge and discharge (asymmetrically) the load capacitor C_load so adjusting to 50% the duty-cycle of the output clock signal CLK_OUT. In particular, the transistors Q2-Q3 and Q5-Q6 are two in-parallel stages that, as a function of the input voltage level Vctrl, allow to generate a current passing through the diode-connected transistor Q4 higher than that one flowing into the diode-connected transistor Q1 (for high values of Vctrl that “enables” Q3 and Q5 and “disables” Q2 and Q6), and vice versa (for low values of Vctrl that “disables” Q3 and Q5 and “enables” Q2 and Q6). These two current levels, flowing into the transistors Q1 and Q4 and varying in an opposite way, are mirrored by the transistors Q7 and Q10,

respectively, that suitably charge and discharge the load capacitor C_load so properly correcting the duty-cycle of the input clock signal CLK_IN.

Table 1D – Circuit transistor sizes.

Transistor	Sizes (W[µm] / L[µm])
Q1, Q7	367 / 0.35
Q2	560 / 0.35
Q3, Q5	60 / 0.35
Q4, Q10	165 / 0.35
Q6	210 / 0.35
Q8, Q11, Q13, Q15	18 / 0.35
Q9, Q12, Q14, Q16	6 / 0.35

The developed DCC has been implemented, simulated and analyzed in CADENCE environment by designing the overall circuit at transistor level in C35B4C3 AMS 0.35µm standard CMOS integrated technology. In particular, the chosen transistor sizes are reported in Table 1D, the integrated capacitor C_load = 0.1pF, the OA_1 and OA_2 have been implemented employing standard analog cells of the AMS technology library, while all the other passive components have been considered external (i.e., off-chip) devices whose values are reported in the following: C1=C2=10 nF, R1=R2=10 kΩ and R3=R4=R5=R6=R7=R8=R9=R10=100 kΩ. The circuit is powered at a VDD = 3.3V single supply voltage and shows a power consumption of about 7mW at the operating frequency equal to 2GHz (i.e., 3.5mW/GHz). The total silicon area is about 0.033mm2 corresponding to only the 16 CMOS transistors Q1-Q16, the load capacitor C_load and the two OAs OA_1 and OA_2.

II. Circuit Analysis and Simulations

The performed simulations of the developed DCC have demonstrated that the circuit is capable to correct the duty-cycle of the input clock signal CLK_IN varying from 30% to 70%, with an operating frequency ranging from 200kHz to 2GHz (i.e., 4 frequency decades), providing a 50% duty-cycle output clock signal CLK_OUT with an error always lower than ±1.5%.

An example of the timing diagram is reported in Figure 2D showing the duty cycle of the signal CLK_OUT (Figure 2D (a)) and the signal Vctrl (Figure 2D (b)) for an input clock signal CLK_IN at 1MHz with a duty-cycle equal to 70%, 50% and 30% (i.e., a clock period of 1µs with a pulse width ranging from 300ns to 700ns). As reported, the feedback

control signal Vctrl starts from an initial value equal to 1.65V (i.e., VDD/2) and, after a transient time, reaches the level that guarantees a corrected duty-cycle CLK_OUT equal to 50%.

An example of the timing diagram is reported in Figure 3D showing the main signals of the DCC circuit for an input clock signal (red waveform) CLK_IN at 2MHz with a duty-cycle equal to 30% and 70% (i.e., a clock period of 500ns with a pulse width equal to 150ns (panel a) and 350ns (panel b)), the Vctrl signal (bottom waveform) and the CLK_OUT signal (blue waveform). As reported, the feedback control signal Vctrl starts from an initial value equal to 1.65V (i.e., VDD/2) and, after a transient time of about 80□s (i.e., the DCC response-time mainly due to the low-pass filters R1-C1 and R2-C2 in the feedback sub-system) for both the cases, reaches the level equal to 0.95V (panel a) and 2.35V (panel b) allowing the output clock signal CLK_OUT achieving a corrected duty-cycle equal to 50%.

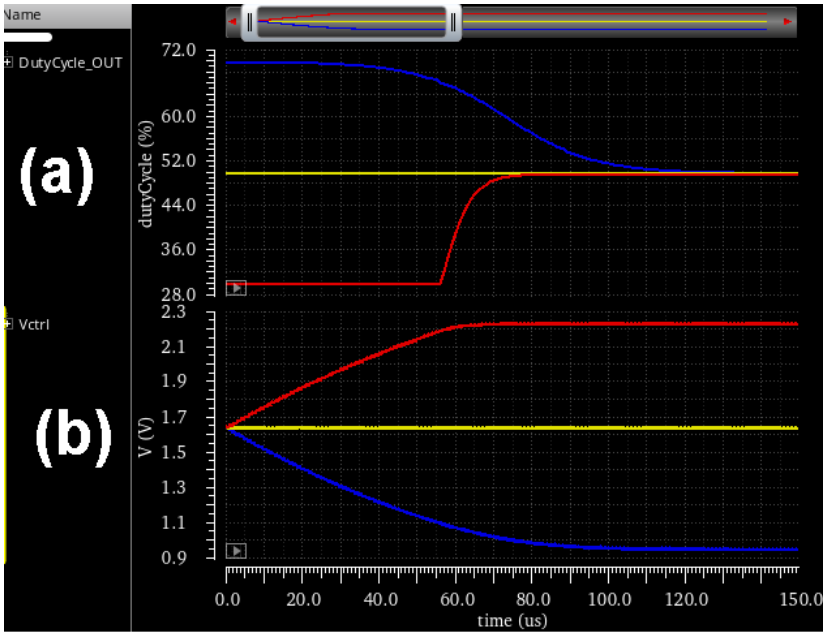

Figure 2D - Simulation results: example of the CLK_OUT Duty-Cycle (a) and Vctrl(b) for an input clock signal CLK_IN at 1MHz with a duty-cycle ranging from 30% to 70%..

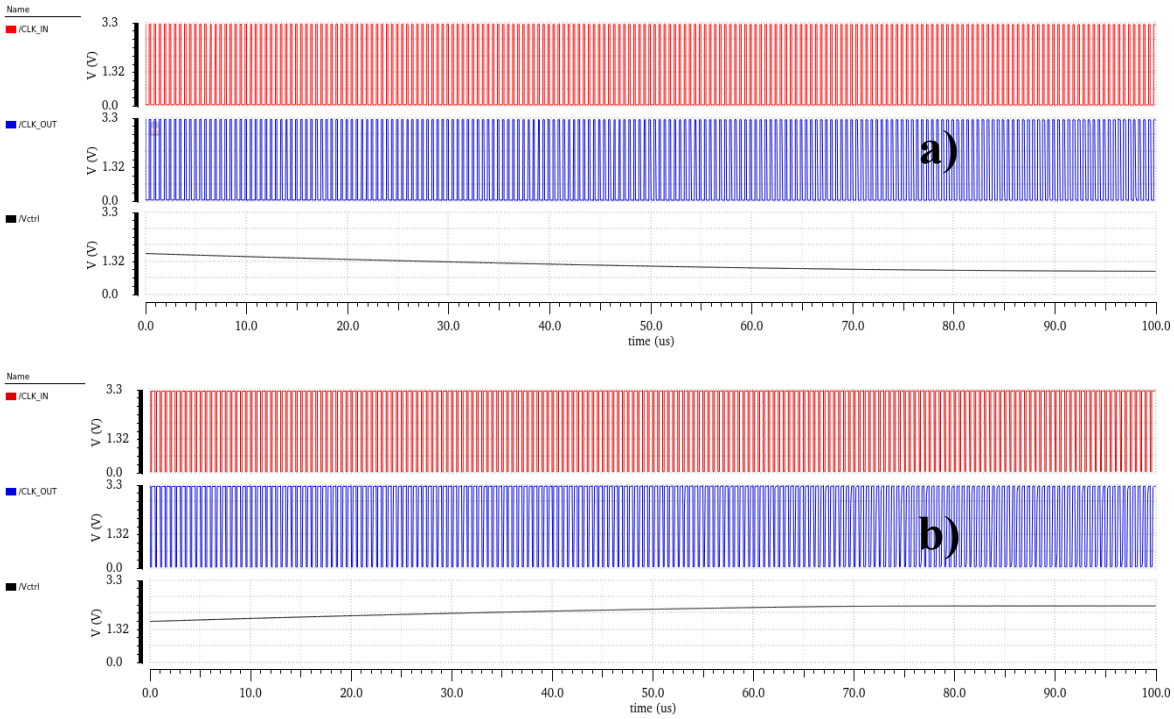

Figure 3D - Post-layout simulations: timing diagram of the DCC main signals for an input clock signal CLK_IN at 2MHz with a duty-cycle equal to: a) 30%, b) 70%.

The performed simulations have demonstrated the DCC capability to correct the input clock signal duty-cycle varying from 30% to 70% with an error lower than ±1.5% for operating frequencies ranging from 200kHz to 2GHz. Finally, in Table 2D the main DCC circuit characteristics and performances are summarized and compared with those ones of other similar solutions reported in the Literature. In particular, the proposed solution shows very good features especially in terms of high operating frequency range, low power consumption and reduced silicon area together with a satisfactory input duty-cycle range and output duty-cycle error.

Table 2D – Comparison with similar solutions.

PARAMETER	***REFERENCE - YEAR***								
	[19] - 2016	***[28] - 2017***	***[21] - 2007***	***[29] - 2016***	***[22] - 2011***	***[25] - 2007***	***[26] - 2012***	***[27] - 2008***	***Developed Solution***
Circuit typology	Digital	Analogue	Digital	Analogue	Digital	Analogue	Digital	Analogue	Analogue
Integrated technology	CMOS 65nm	CMOS 65nm	CMOS 180nm	CMOS 130nm	CMOS 54nm	CMOS 350nm	CMOS 130nm	CMOS 180nm	CMOS 350nm
Supply voltage	1.2V	1V	1.8V	n.a.	1.8V	3.3V	1.2V	1.8V	3.3V
Operating frequency range	120MHz ÷ 2GHz	2.4GHz ÷ 2.9GHz	40MHz ÷ 550MHz	100MHz ÷ 3.5GHz	100MHz ÷ 1GHz	3MHz ÷ 660MHz	310MHz ÷ 1GHz	1MHz ÷ 1.3GHz	200kHz ÷ 2GHz
Input duty-cycle range	20÷80%	30÷70%	20÷80%	30÷70%	44÷63%	30÷70%	40÷60%	30÷70%	30÷70%
Output duty-cycle error	< ±0.6%	< ±1%	< ±2%	< ±1%	< ±2%	< ±1.5%	< ±1%	n.a.	< ±1.5%
Power consumption (mW/GHz)	6.6mW@2GHz (3.3)	0.17mW@2.9GHz (0.06)	12.6mW@0.55GHz (22.9)	20mW@1GHz (20)	29.5mW@1GHz (29.5)	1.1mW@550MHz (2)	3.2mW@1GHz (3.2)	4.8mW@1.3GHz (3.7)	7mW@2GHz (3.5)
Typical application	SDRAM	High-speed serial interface	DLL	Wide frequency range transceiver, high-speed digital link, memory	DLL/DRAM	General purpose	DRAM	General purpose	General purpose
Silicon area	0.059mm^2	0.00048mm^2	0.2mm^2	0.011mm^2	0.11mm^2	0.06mm^2	0.048mm^2	0.057mm^2	0.033mm^2

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APPENDIX E: TUNABLE-GAIN DUAL-CHANNEL DUAL-PHASE LOCK-IN AMPLIFIER FOR LASER TRANSMISSION SPECTROSCOPY

This appendix reports on the design, fabrication and characterization of a double channel, tunable gain Lock-in Amplifier (LIA) operating with voltage input pulses provided by two Si photodiodes that measure the power variations of 10 ns laser pulses at 10 Hz repetition rate Q-Switched Nd:YAG tunable laser equipped with an optical parametric oscillator and second and third harmonic generation crystals. This laser is used to perform Laser Transmission Spectroscopy (LTS) measurement to evaluate both the concentration and dimension of nanoparticles for biomedical and biophysics applications. Nowadays, the challenge is to investigate the role of nanoparticles in activating biological processes when their concentrations are less than 10^9 particles/ml and/or their size ranges from few tens to few hundreds of nanometers. LTS is a powerful technique to investigate these topics of research and is based on the measurement of the transmittance through the sample containing the nanoparticles (i.e., the signal channel) against that one through a sample with no nanoparticles (i.e., the reference channel). When the nanoparticles size and/or concentration are small, also the light scattering process that influences the transmittance is small: the value of the signal channel approaches that one of the reference channel. Thus, in this case, it is of paramount importance to develop methods to perform measurements with very low indetermination. The designed double channel, tunable gain LIA is a solution to this problem since it allows to implement a new variable gain LTS method. Before performing the LTS measurements of the samples of interest, a calibration curve is accomplished for each wavelength of the laser beam passing through the signal and reference channels both in absence of nanoparticles. Under these conditions, the LIA gain is varied to achieve a ratio between the light power passing through the two channels as much as possible close to 1. This avoids any experimental artifact due to the optical components that drive the laser beam along the two signal and reference channels. Once verified that the calibration curve remains unaltered in time, the variable gain method LT can be used to determine the wavelength dependent extinction coefficient of NIST standard polystyrene particles suspension. Respect to the method of the double ratio conventionally used for these measurements the variable gain technique decreases the extinction coefficient relative error up to a factor 8. As outlined before, since the LTS technique allows to determine the size and the concentration of colloidal suspensions of paramount importance for biological and medical applications [1-4], in the following we will discuss in some details the LTS principle of operation and the contribution of the designed,

fabricated characterized double channel, double gain Lock-In Amplifier to improve the LTS measurements.

I. LTS Methodology

LTS measures the wavelength dependent transmission coefficient T of a suspension of particles diluted in aqueous medium. Once T is achieved, the related extinction coefficient α can be calculated by the following relation:

$$\alpha(\lambda, r) = -\frac{\ln [T(\lambda,r)]}{z} \quad (1)$$

where z is the sample and reference optical path and r is the radius of the nanoparticles. The resulting extinction coefficients are analyzed and inverted by means of a square root-based algorithm [5] to return the particle size and concentration via computing the known wavelength-size dependent properties of the nanoparticles under study, i.e., their Mie scattering cross-section σ(λ,r) [6,7]. Figure 1E reports the experimental setup for the LTS measurements of the transmittance $T(\lambda,r)$ of the laser beam passing through the sample channel containing the particles (SC) and the reference channel (RC) with only the suspending medium.

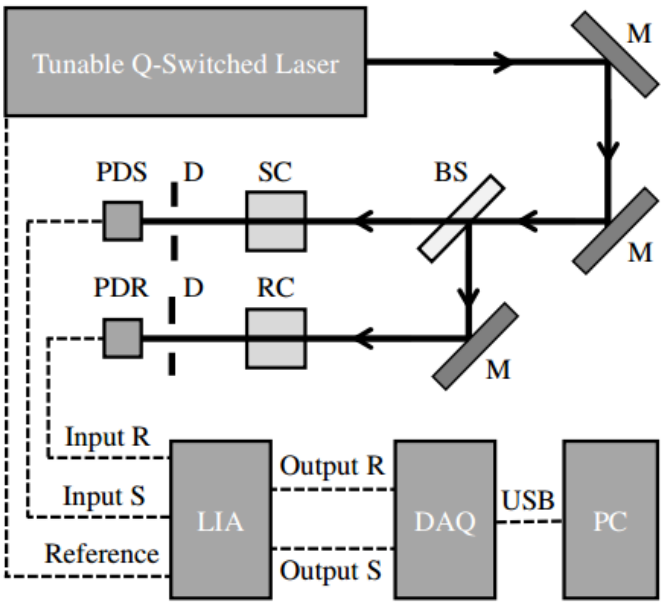

Figure 1E - The LTS experimental setup: the tunable laser is a Q-Switched Nd:YAG equipped with an optical parametric oscillator and second and third harmonic generation crystals allowing for the wavelength tuning from 400-2600nm; M are total reflection mirrors; BS is a polka-dot 50/50 beam splitter; SC and RC are the sample and the reference cuvettes, respectively; D are variable diaphragms; PDS and PDR are Si photodiodes detecting the laser beam power passing through SC and RC, respectively. LIA is a tunable gain double channel Lock-In Amplifier, DAQ is a Data Acquisition board and PC is a Personal Computer.

The setup measures simultaneously the two transmission coefficients and calculate the ratio between them. As above discussed, the method used to cancel out the contributions of the optics and detector efficiencies that constitute the two optical paths containing SC and RC is to calculate a double ratio of the transmitted laser intensity by interchanging the position of SC and RC (i.e., by performing a 180° rotation of SC and RC) [1]. The development of a tunable gain LIA allows to propose a new measurement method based on balancing the transmitted laser intensity passing through the SC and RC channels in a calibration procedure carried out with the two samples that do not contain the particles under investigation. The aim of the calibration procedure consists in collecting the values of the LIA gain for each laser wavelength in order to provide a ratio equal to about 1 between the transmitted laser intensities detected by the photodiodes PDS and PDR. The achieved values of the LIA gain are used in the LTS measurements with SC containing now the particles under study to determine the extinction coefficient $\alpha(\lambda,r)$ simply from the ratio between the SC and RC transmitted laser intensities.

The standard measurement procedure for LTS is based on the double ratio method [8]. Referring to Figure 1E, the use of this method implies that the characterization of the nanoparticles contained in SC (i.e., the determination of their size and concentration) is achieved by performing two distinct LTS measurements: in the first one the cuvette positions are, for example, as shown in Figure 1E. The resulting transmission coefficient is $T_1(\lambda,r) = S_1(\lambda,r)/R_1(\lambda)$ where, as before defined, λ and r are the laser wavelength and the radius of the nanoparticles, respectively. Here, $S_1(\lambda,r)$ is the PDS voltage signal proportional to the laser beam intensity passing through the sample channel and $R_1(\lambda)$ the PDR voltage signal proportional to the laser beam intensity passing through the reference channel that is independent from r since it contains only the liquid solution. For the second LTS measurement, the position of SC and RC in the optical channels are interchanged so obtaining a second transmission coefficient $T_2(\lambda,r) = S_2(\lambda)/R_2(\lambda,r)$. In this case, $S_2(\lambda)$ is the PDS voltage signal proportional to the laser beam intensity passing through the sample channel that contains now RC and $R_2(\lambda,r)$ is the PDR voltage signal proportional to the laser beam intensity passing through the reference channel that contains now SC. In this way, the procedure cancels out any difference in the two optical paths but at the expense to double the measurement time. The final result of these two LTS measurements is the transmission coefficient related to the presence of the particles in SC that is obtained by the ratio between the two transmission coefficients $T_1(\lambda,r)$ and $T_2(\lambda,r)$:

$$T(\lambda,r) = \sqrt{\frac{T_1(\lambda,r)}{T_2(\lambda,r)}} = \sqrt{\frac{S_1(\lambda,r)R_2(\lambda,r)}{R_1(\lambda)S_2(\lambda)}} \quad (2)$$

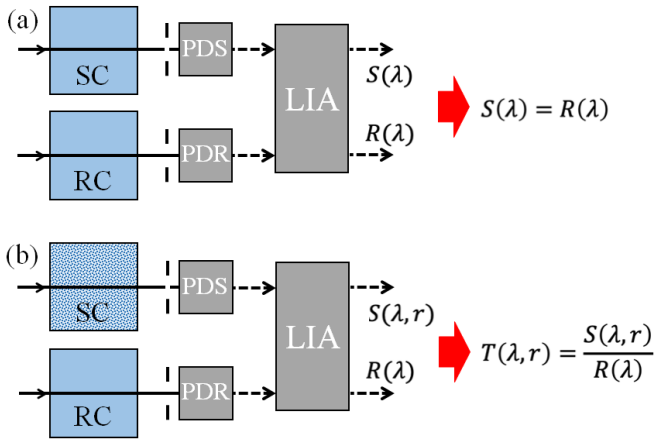

Figure 2E - Panel: (a) the experimental conditions used for the calibration of the signal S (□) and the reference R (□) amplitudes by varying the gain of each channel of the LIA; (b) the experimental conditions used for the LTS measurements of the sample transmission coefficient T(□,r): in this last case the sample cuvette SC contains the suspension of nanoparticles and the signal depends also on their radius.

This result makes clear that, even if the double ratio method does not need an initial calibration procedure of the LTS setup, a larger value of the measurement propagation of uncertainty is expected for $T(\lambda, r)$ if compared to that one of a single ratio $S(\lambda, r)/R(\lambda)$. To overcome this problem that can strongly limit the LTS measurement sensitivity and resolution, we demonstrate that it is possible to perform the characterization of the nanoparticle contained in SC by a single LTS measurement after a proper calibration of the experimental apparatus. By acting on the gain of each one of the two channels of the LIA, the sample and reference signals are balanced for each wavelength by using the liquid solution inside both the SC an RC cuvettes (i.e., a blank sample in the two cuvettes). This method considerably reduces the total measurement time and increases the detection sensitivity and resolution of the apparatus. To illustrate in detail the method used for the LTS calibration, we refer to Figure 2E. As before outlined, in the first step (see panel (a)) both the sample SC and reference RC cuvettes are filled with the aqueous suspending medium (i.e., without the suspended particles) and, for every wavelength of the probing laser beam, the LIA gains $G_1(\lambda)$ and $G_2(\lambda)$ of each one of the two LIA input channels are varied until the ratio of the LIA output voltages $S(\lambda)/R(\lambda)$ is equal to 1 within a value of the standard deviation of 0.5%.

II. Tunable-Gain Dual-Channel Dual-Phase Lock-In Amplifier (LIA)

The block scheme of the designed dual channel ad-hoc tunable gain LIA is reported in Figure 3E.

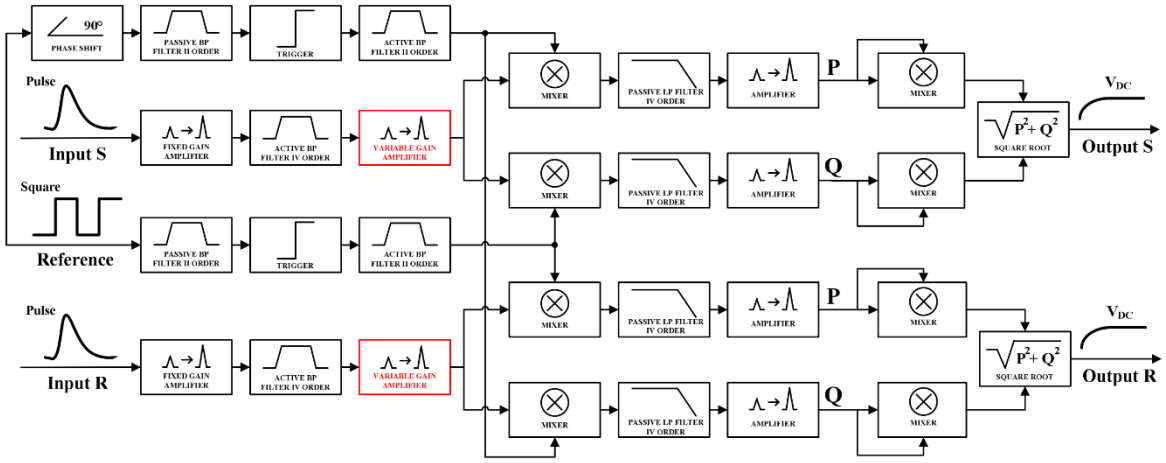

Figure 3E - Implemented block scheme of the implemented LIA.

Considering the laser source characteristics used for the experiments, the LIA internal blocks have been suitably designed and optimized in terms of the detection sensitivity and resolution, considering 5 ns pulsed voltage input signals at a repetition rate f_0=10 Hz with a mean value different from zero. Its main stages have been designed employing standard circuit topologies and configurations for filters, triggers, phase-shifters and amplifiers [9,10]. The other functions, namely the mixers and the square root operations, have been directly implemented by commercial active devices. More in detail, at each one of the LIA input stages (i.e., for the Input S and Input R pulsed signals) the first block is a tunable gain amplifier based on an Operational Amplifier (OA) operating in a non-inverting configuration, as shown in the schematic circuit reported in Figure 4E. It provides a variable gain, ranging from 2 up to 271, achieved by changing the value of the equivalent floating resistor R_{EQ}. The gain tuning is performed by properly acting on the control voltage V_{CTRL}, through LabVIEW environment and the DAQ board, that suitably regulates the R_{EQ} value according to the relationship reported in Figure 4E. The tunable gain amplifier is combined with the fourth-order active band-pass filter employed in order to: i) reduce the harmonic content of the input signal and the associated noise bandwidth; ii) eliminate the input disturbs and/or interferences; iii) achieve and amplify the main harmonic components of the input signals. The schematic circuit of this stage is reported in Figure 5E. It has been implemented by a cascade of two active second-order multiple negative feedback inverting filter topology centered at f_0 = 10 Hz with a maximum gain of about 550 and a quality factor Q = 12.5 corresponding to a bandwidth BW = 0.8 Hz. Then, after the demodulation stage (i.e., the mixer block), the fourth-order passive low-pass filter allows to extract the DC component of the resulting signal and, at the same time, to regulate the overall system response time.

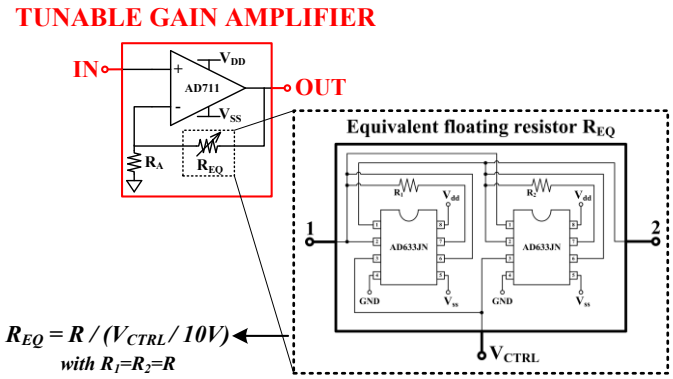

Figure 4E - Schematic circuit of the tunable gain amplifier and the voltage controlled floating resistor REQ.

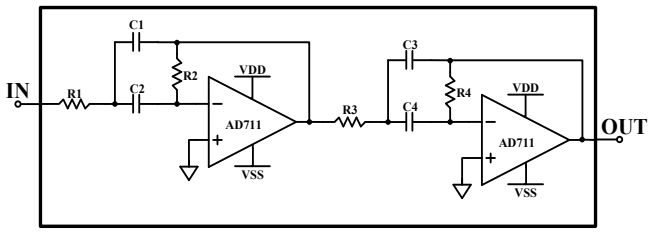

Figure 5E - Schematic circuit of the fourth-order active band-pass filter.

This filter is based on a simple passive topology composed by a cascade of four RC-cells, as shown in Figure 6E, with a resulting cut-off frequency $f_t \approx 10$ mHz, much smaller than $f_0 = 10$ Hz (i.e., the LIA reference operating frequency that corresponds to the laser repetition rate f0) and its main harmonics. Moreover, an additional amplifier has been also included to further increase the instrument total gain and to enhance the LIA detection sensitivity and resolution. This stage makes use of an OA in a non-inverting configuration with a fixed gain equal to 10. Finally, the resulting Phase (P) and Quadrature (Q) signals are squared through further mixer blocks and, by means of a square root operation of the sum P^2+Q^2, the final VDC output signal, proportional to the amplitude of the input pulses, is provided. Referring to the square wave reference signal, a phase shifter block has been included so to add a 90° phase shift between the P and Q paths. The schematic circuit implementation, including a trimmer for a phase shift fine tuning, is reported in Figure 7E. In addition, trigger blocks are also employed, implemented through OAs in an open-loop comparator configuration, so to provide square wave signals with fixed and constant values (i.e., low level = VSS, high level = VDD). Finally, a second-order active band-pass filter has been included to extract the main harmonic component of the reference signal employed for the demodulation operation. It has been implemented by an active second-order multiple negative feedback inverting filter topology ($f_0 = 10$ Hz, maximum gain = 22 and quality factor Q = 5).

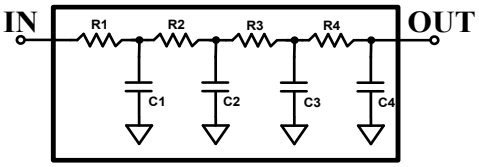

Figure 6E - Schematic circuit of the fourth-order passive low-pass filter.

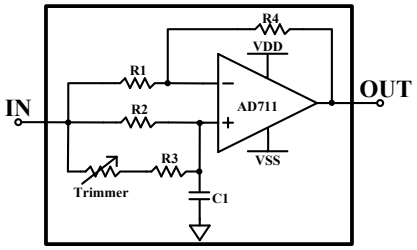

Figure 7E - Schematic circuit of the phase shifter block.

Figure 8E - Photo of the fabricated PCB implementing the developed LIA mounted inside an instrumental box for fast prototyping.

A PCB prototype of LIA, whose photo is reported in Figure 8E, has been developed by using commercial discrete devices. In particular, the active components employed for the implementation of the different blocks composing LIA are AD711 BiFET high speed OA (by Analog Devices). The mixers are AD633 analog multipliers (by Analog Devices) while the square root has been implemented through AD734 high speed four-quadrant analog multiplier (by Analog Devices). All the OA and the other active components are powered

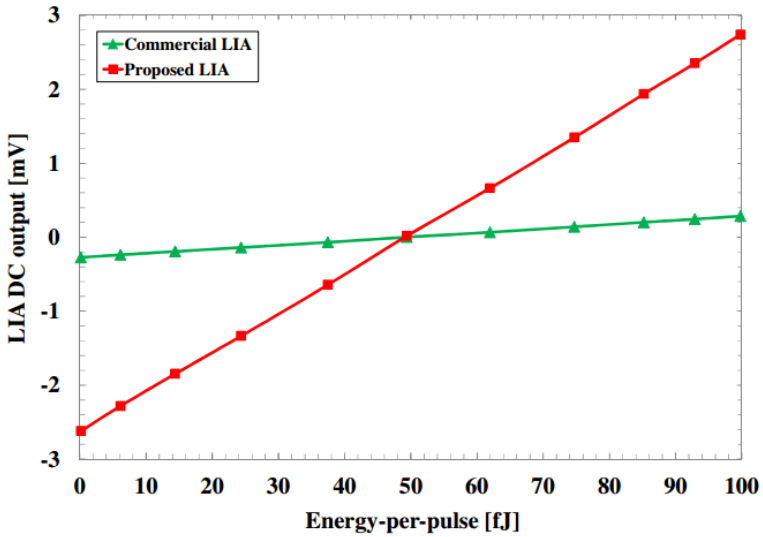

Figure 9E - Experimental characterization of the designed and the commercial LIAs.

at a dual DC voltage equal to ±15 V. The LIA optoelectronic characterization has been conducted by varying the laser energy-per-pulse in the signal path from 0 to 100 fJ, considering the starting value of about 49.5 fJ (i.e., for ϑ = 45°). Figure 9E reports the measured DC output voltages of the implemented ranging in ±2.7 mV compared with that one achieved by using a commercial LIA (SRS830DSP by Stanford Research Systems) ranging in ±0.28 mV. The resulting sensitivities are equal to 54 µV/fJ and 5.6 µV/fJ for the designed and commercial LIAs, respectively.

III. Experimental Measurements with the Overall System

The experimental validation of the employed variable gain calibration method has been first performed by LTS measurements of the size and concentration of a suspension of NIST standard polystyrene nanoparticles (Duke Standard by Thermo Scientific - Waltham, MA - USA). The spherical nanoparticle nominal average radius and concentration were equal to r=254±4 nm and C=1.0x10^9 particles/ml, respectively. In Figure 10E are reported the LTS measurement of the extinction coefficients by using the double ratio method (upper panel), and the variable gain calibration procedure (lower panel). As a first qualitative remark, the error bars associated to the experimental data are significantly smaller for the variable gain calibration procedure.

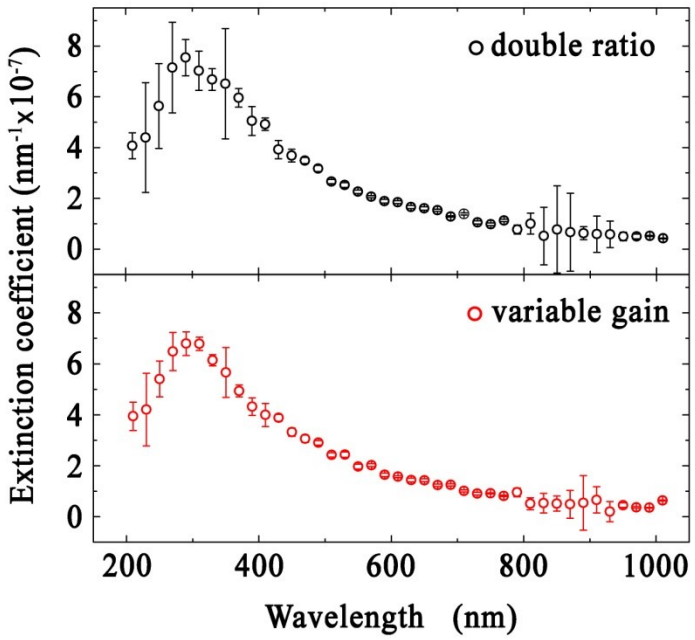

Figure 10E - Extinction coefficient as a function of wavelength of a NIST standard polystyrene particles suspension obtained by the balanced LTS method (black) and the double ratio LTS method (red). In the inset is shown the comparison of the corresponding relative errors.

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PUBBLICATIONS

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